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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	125MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	150
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpxd2020vlt125

— 208 LQFP, 0.5 mm pitch, 28 mm × 28 mm outline
— 416 TEPBGA, 1mm ball pitch, 27 mm × 27 mm outline

1.4 Feature details

1.4.1 Low-power operation

The PXD20 is designed for optimized low-power operation and dynamic power management of the CPU and peripherals. Power management features include software-controlled clock gating of peripherals and multiple power domains to minimize leakage in low-power modes.

There are three low-power modes:

- STANDBY
- STOP
- HALT

and five dynamic power modes — RUN[0..3] and DRUN. All low-power modes use clock gating to halt the clock for all or part of the device.

STANDBY mode turns off the power to the majority of the chip to offer the lowest power consumption mode.

The device can be awakened from STANDBY mode via from any of up to 23 I/O pins, a reset or from a periodic wake-up using a low power oscillator. If required, it is possible to enable the internal 16 MHz oscillator, the external 4–16 MHz oscillator and the external 32 KHz oscillator.

In STANDBY mode the contents of the CPU, on-chip peripheral registers and potentially some of the volatile memory are lost. The two possible configurations in STANDBY mode are:

- The device retains 64 KB of the on-chip SRAM, but the content of the graphics SRAM is lost.
- The device retains 8 KB of the on-chip SRAM, but the content of the graphics SRAM is lost.

STOP mode maintains power to the entire device allowing the retention of all on-chip registers and memory, and providing a faster recovery low power mode than the lowest-power STANDBY mode. There is no need to reconfigure the device before executing code. The clocks to the CPU and peripherals are halted and can be optionally stopped to the oscillator or PLL at the expense of a slower start-up time.

STOP is entered from RUN mode only. Wake-up from STOP mode is triggered by an external event or by the internal periodic wake-up, if enabled.

RUN modes are the main operating modes where the entire device can be powered and clocked and from which most processing activity is done. Four dynamic RUN modes are supported—RUN0 - RUN3. The ability to configure and select different RUN modes enables different clocks and power configurations to be supported with respect to each other and to allow switching between different operating conditions. The necessary peripherals, clock sources, clock speed and system clock prescalers can be independently configured for each of the four RUN modes of the device.

HALT mode is a reduced activity, low power mode intended for moderate periods of lower processing activity. In this mode the CPU system clocks are stopped but user-selected peripheral tasks can continue to run. It can be configured to provide more efficient power management features (switch-off PLL, flash memory, main regulator, etc.) at the cost of longer wake up latency. The system returns to RUN mode as soon as an event or interrupt is pending.

Table 2 summarizes the operating modes of the PXD20.

- Direct readback of the pin value supported on all digital output pins through the SIU
- Configurable digital input filter that can be applied to up to 24 general purpose input pins for noise elimination on external interrupts
- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset.

1.4.8 On-chip flash memory with ECC

The PXD20 microcontroller has the following flash memory features:

- 2 MB of flash memory
  - Typical flash memory access time: 0 wait-state for buffer hits, 3 wait-states for page buffer miss at 125 MHz
  - Two 4 × 128-bit page buffers with programmable prefetch control
    - One set of page buffers can be allocated for code-only, fixed partitions of code and data, all available for any access
    - One set of page buffers allocated to Display Controller Units, Graphics Accelerator and the eDMA
  - 64-bit ECC with single-bit correction, double-bit detection for data integrity
- Small block flash arrangement to support features such as boot block, EEPROM Emulation, operating system block.
  - 8×16 KB
  - 2×64 KB
  - 2×128 KB
  - 6×256 KB
- Hardware managed Flash writes, erase and verify sequence
- Censorship protection scheme to prevent Flash content visibility

1.4.9 Static random-access memory (SRAM)

The PXD20 microcontroller has 64 KB general-purpose on-chip SRAM with the following features:

- Typical SRAM access time: 1 wait-state for reads and 32-bit writes
- 32-bit ECC with single-bit correction, double bit detection for data integrity
- Supports byte (8-bit), half word (16-bit), word (32-bit) and double-word (64-bit) writes for optimal use of memory
- User transparent ECC encoding and decoding for byte, half word, and word accesses
- Separate internal power domains applied to 56 KB and 8 KB SRAM blocks during STANDBY modes to retain contents during low power mode.

1.4.10 On-chip graphics SRAM

The PXD20 microcontroller has 1 MB on-chip graphics SRAM with the following features:

- Two crossbar slave ports:
  - One dedicated to the 2D Graphics Accelerator (GFX2D) access
  - One dedicated to all other crossbar masters
- Usable as general purpose SRAM
- Supports byte (8-bit), half word (16-bit), word (32-bit) and double-word (64-bit) writes for optimal use of memory
- RAM controller with hardware RAM fill function supporting all-zeroes or all-ones SRAM initialization
- Independent data buffers (one per AHB port) for maximum system performance
  - Optimized for burst transfers (read + write)
  - Programmable read prefetch capabilities

To secure the content of all critical information to be displayed, a safety mode can be activated to check the integrity of critical data along the whole system data path from the memory to the TFT pads.

The DCU3 features the following:

- Display color depth: up to 24 bpp
- Generation of all RGB and control signals for TFT
- Four-plane blending
- Maximum number of Input Layers: 16 (fixed priority)
- Dynamic Look-Up-Table (Color and Gamma Look-Up)
- α–blending range: up to 256 levels
- Transparency Mode
- Gamma Correction
- Tiled mode on all the layers
- Hardware Cursor
- Supports YCrCb 4:2:2 input data format
- RLE decode inline supporting direct read of RLE compressed images from system memory
- Critical display content integrity monitoring for Functional Safety support
- Internal Direct Memory Access (DMA) module to transfer data from internal and / or external memory.

The DCU3 also features a Parallel Data Interface (PDI) to receive external digital video or graphic content into the DCU3. The PDI input is directly injected into the DCU3 background plane FIFO. When the PDI is activated, all the DCU3 synchronization is extracted from the external video stream to guarantee the synchronization of the two video sources.

The PDI can be used to:

- Connect a video camera output directly to the PDI
- Connect a secondary display driver as slave with a minimum of extra cost
- Connect a device gathering various Video sources
- Provide flexibility to allow the DCU to be used in slave mode (external synchronization)

The PDI features the following:

- Supported color modes:
  - 8-bit mono
  - 8-bit color multiplexed
  - RGB565
  - 16-bit/18-bit RAW color
- Supported synchronization modes:
  - embedded ITU-R BT.656-4 (RGB565 mode 2)
  - HSYNC, VSYNC
  - Data Enable
- Direct interface with DCU3 background plane FIFO
- Synchronization generation for the DCU3

1.4.14 Display Control Unit Lite (DCULite)

The DCULite is a display controller designed to enable the PXD20 to drive a second TFT LCD display up to XGA resolution using direct blit graphics and video. The DCULite includes all features of the DCU3, including the PDI with the following exceptions:

- Reduced from 4-plane to 2-plane blending
- Reduced from 16 layers to 4 layers
- Reduced CLUT size

  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
    - Parity, noise and framing errors
  - Interrupt driven operation with 4 interrupts sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods
- LIN features:
  - Autonomous LIN frame handling
  - Message buffer to store identifier and up to eight data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors
  - Sync field; Delimiter; ID parity; Bit, Framing; Checksum and Timeout errors
  - Classic or extended checksum calculation
  - Configurable Break duration of up to 36-bit times
  - Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features
    - Loop back
    - Self Test
    - LIN bus stuck dominant detection
  - Interrupt driven operation with 16 interrupt sources
  - LIN slave mode features
    - Autonomous LIN header handling
    - Autonomous LIN response handling
    - Discarding of irrelevant LIN responses using up to 16 ID filters

1.4.25 Inter-Integrated Circuit (I^2C) controller modules

The PXD20 includes four I^2C modules. Each module features the following:

- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I^2C bus standard
- Multi-master operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

2.3 416 TEPBGA package pinout–40 to 105°C

Figure 4 shows the pinout for the 416 TEPBGA package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	ddr_dq[26]	ddr_dq[27]	ddr_dq[28]	ddr_dq[29]	30]	31]	ddr_ba[0]	ddr_ba[1]	ddr_ba[2]	ddr_address[0]	ddr_address[4]	ddr_address[6]	ddr_address[8]	ddr_address[12]	PG12	PF14	PF10	PF8	PF5	PF3	PK0	PB3	PJ12	PL11	PG7	PG6	A
B	ddr_dq[25]	VSS	ddr_dqs[3]	ddr_dm[3]	VSS	ddr_cas	ddr_ras	VSS	ddr_web	ddr_address[1]	VSS	ddr_address[7]	ddr_address[9]	VSS	ddr_address[15]	PF13	VDDE	PF15	VSS	PF1	VDDE	PJ15	PL13	VDDE	VSS	PG5	B
C	ddr_dq[23]]	VDDE_DDR	VSS	ddr_dq[24]	VDDE_DDR	VSS	ddr_dram_clk	VDDE_DDR	VSS	ddr_address[2]	VDDE_DDR	VSS	ddr_address[10]	VDDE_DDR	VSS	PF12	VSS	PF7	VDDE	PF0	VSS	PJ14	PL12	PL10	PG3	PG4	C
D	ddr_dq[19]	ddr_dq[20]	ddr_dq[21]	ddr_dq[22]	ddr_odt	VDD33_DDR	ddr_dram_clkb	ddr_cke	ddr_cs	ddr_address[3]	ddr_address[5]	VDD33_DDR	ddr_address[11]	ddr_address[13]	ddr_address[14]	PF11	PF9	PF6	PF4	PK1	PB2	PJ13	PM2	**VREF_RSDS2**	PG2	PG1	D
E	ddr_dq[17]	VSS	VDDE_DDR	ddr_dq[18]																			PG11	VSS	VDDE	PG0	E
F	ddr_dq[16]	**MVTT3**	VSS	VDD33_DDR																			PA15	PA14	PA13	PA12	F
G	ddr_dq[15]	ddr_dqs[2]	ddr_dm[2]	ddr_dq[14]																			PA11	PA9	PA8	PA7	G
H	ddr_dq[13]	VSS	VDDE_DDR	ddr_dq[12]																			PA10	VDDE	VSS	VA6	H
J	ddr_dq[11]	**MVTT2**	VSS	MVREF																			PA3	**VREF_RSDS1**	PA5	PA4	J
K	ddr_dq[9]	ddr_dqs[1]	ddr_dm[1]	ddr_dq[10]						VDD12	VSS	VDD12	VSS	VDD12	VSS	VDD12	VSS						PA2	VSS	PA1	PA0	K
L	ddr_dq[8]	VSS	VDDE_DDR	ddr_dq[7]						VSS	VDD12	VSS	VDD12	VSS	VDD12	VSS	VDD12						PM13	PM12	VDDE	PJ0	L
M	ddr_dq[5]	**MVTT1**	VSS	ddr_dq[6]						VDD12	VSS	VSS	VSS	VSS	VSS	VDD12	VSS						PO7	PO6	PO5	PO4	M
N	ddr_dq[3]	ddr_dqs[0]	VDDE_DDR	ddr_dq[4]						VSS	VDD12	VSS	VSS	VSS	VSS	VSS	VDD12						PO3	VDDE	PO2	PO1	N
P	ddr_dq[1]	VSS	ddr_dm[0]	ddr_dq[2]						VDD12	VSS	VSS	VSS	VSS	VSS	VDD12	VSS						PO0	PN15	VSS	PN14	P
R	ddr_dq[0]	**MVTT0**	VSS	VDD33_DDR						VSS	VDD12	VSS	VSS	VSS	VSS	VSS	VDD12						PE7	PE6	PN13	PN12	R
T	PG10	PG9	VDDE_DDR	PG8						VDD12	VSS	VDD12	VSS	VDD12	VSS	VDD12	VSS						PE5	PE4	PE3	PE2	T
U	PJ9	PJ8	PJ2	PJ1						VSS	VDD12	VSS	VDD12	VSS	VDD12	VSS	VDD12						PE1	VSSM	VDDM	PE0	U
V	PB1	VSS	PJ11	PJ10																			PD15	PD14	PD13	PD12	V
W	**RESET**	PB10	VDDE	PB0																			PD11	VDDM	VSSM	PD10	W
Y	VSS	PM4	PM3	PB11																			PD9	PD8	PD7	PD6	Y
AA	**XTAL**	**VREG_BYPASS**	**VRC_CTRL**	**VDDREG**																			PD5	VSSM	VDDM	PD4	AA
AB	**EXTAL**	PL4	VSS	**VDDPLL**																			PD3	PD2	PD1	PD0	AB
AC	**VSUP_TEST**	PL5	**PN0**	**PK4**	**PK6**	**PH0**	PF2	PB13	PK11	PN2	PN4	PN8	PB9	PB7	PJ7	PB5	MCKO	MDO6	MDO10	MVO0	PC0	VDDA	VSSEH_ADC	PC3	PC1	PC2	AC
AD	**PL6**	VDDE	**PN1**	VSS	**PK7**	PH1	VDDE	EVTI	MSEO	VSS	PN5	PN9	VDDE	PJ4	PJ3	VSS	MSEO2	MDO7	VDDE	MDO1	PC6	VSSA	VDDEH_ADC	PC4	PC7	PC5	AD
AE	**PL7**	VSS	**PK2**	VDDE	**PK8**	PH2	VSS	EVTO	PM0	VDDE	PN6	PN10	VSS	PJ5	PH4	VDDE	MDO4	MDO8	VSS	MDO2	PL1	PL0	PC10	PC11	PC9	PC8	AE
AF	**PL8**	**PL9**	**PK3**	**PK5**	**PK9**	**PH3**	PB12	PK10	PM1	PN3	PN7	PN11	PB8	PJ6	PB4	PB6	MDO5	MDO9	MDO11	MDO3	PL3	PL2	**PC15**	**PC14**	PC13	PC12	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 4. 416 TEPBGA pinout

Table 6. DRAM interface pin summary (continued)

Port pin[1]	Function	I/O direction	Pad type	PCR	RESET config[2]	Pin number
						416 TEPBGA
DDR_CLKB	DRAM Clock bar	Output	DDR	NA	Output, None	D7
DDR_CK	DRAM Clock Enable	Output	DDR	PCR[222]	Output, Pull Down	D8
DDR_CS	DRAM Chip Select	Output	DDR	PCR[223]	Output, None	D9
MVREF	DDR Reference Voltage	Input	—	NA	—	J4
MVTT	DRAM Termination Voltage	Input	—	NA	—	F2,J2,M2,R2

1 These port pins are disabled and unpowered on packages where the DRAM interface is not bonded out.

2 Reset configuration is given as I/O direction and pull direction (for example, “Input, pullup”).

2.4.7 VIU muxing

The DCU3, DCULite and VIU2 modules share the same pins for input video. It is, however, possibile to feed independent video streams to VIU2 and DCU3 (operating in narrow mode). Figure 5 explains the pin sharing arrangement.

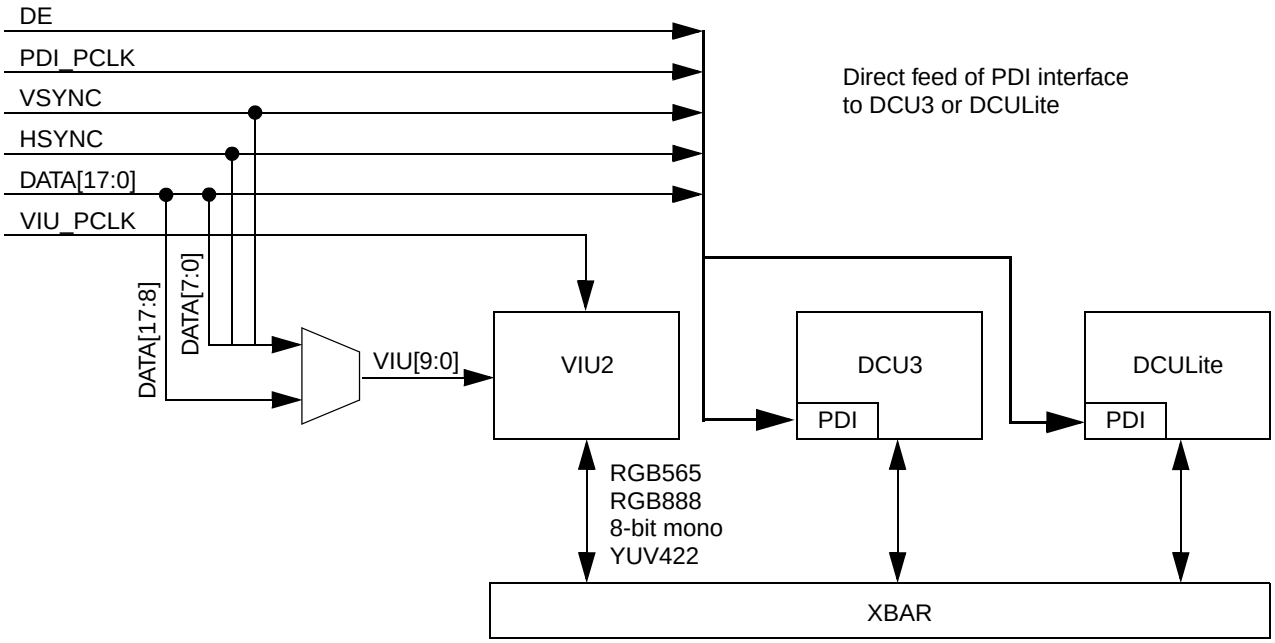

Figure 5. VIU2, DCU3, and DCULite pin sharing

VIU input data selection is done based on select bit (bit 0) of Miscellaneous control register (0xC3FE0340).

- VIU pix data: VIU[9:0]
- Select bit 1’b0: PDI[7:0],HSYNC,VSYNC
- Select bit 1’b1: PDI[17:8]

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PD[11]	PCR[57]	Option 0 Option 1 Option 2 Option 3	GPIO[57] M2C1P SSD2_3 eMIOS0[11]	—	SIUL SMD SSD PWM/Timer	I/O	SMD	None, None	103	119	W23
PD[12]	PCR[58]	Option 0 Option 1 Option 2 Option 3	GPIO[58] M3C0M SSD3_0 eMIOS0[12]	—	SIUL SMD SSD PWM/Timer	I/O	SMD	None, None	106	122	V26
PD[13]	PCR[59]	Option 0 Option 1 Option 2 Option 3	GPIO[59] M3C0P SSD3_1 eMIOS0[13]	—	SIUL SMD SSD PWM/Timer	I/O	SMD	None, None	107	123	V25
PD[14]	PCR[60]	Option 0 Option 1 Option 2 Option 3	GPIO[60] M3C1M SSD3_2 eMIOS0[14]	—	SIUL SMD SSD PWM/Timer	I/O	SMD	None, None	108	124	V24
PD[15]	PCR[61]	Option 0 Option 1 Option 2 Option 3	GPIO[61] M3C1P SSD3_3 eMIOS0[15]	—	SIUL SMD SSD PWM/Timer	I/O	SMD	None, None	109	125	V23
PORT E											
PE[0]	PCR[62]	Option 0 Option 1 Option 2 Option 3	GPIO[62] M4C0M SSD4_0 —	—	SIUL SMD SSD —	I/O	SMD	None, None	—	126	U26
PE[1]	PCR[63]	Option 0 Option 1 Option 2 Option 3	GPIO[63] M4C0P SSD4_1 —	—	SIUL SMD SSD —	I/O	SMD	None, None	—	127	U23
PE[2]	PCR[64]	Option 0 Option 1 Option 2 Option 3	GPIO[64] M4C1M SSD4_2 —	—	SIUL SMD SSD —	I/O	SMD	None, None	—	128	T26

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PE[3]	PCR[65]	Option 0 Option 1 Option 2 Option 3	GPIO[65] M4C1P SSD4_3 —	—	SIUL SMD SSD —	I/O	SMD	None, None	—	129	T25
PE[4]	PCR[66]	Option 0 Option 1 Option 2 Option 3	GPIO[66] M5C0M SSD5_0 —	—	SIUL SMD SSD —	I/O	SMD	None, None	—	132	T24
PE[5]	PCR[67]	Option 0 Option 1 Option 2 Option 3	GPIO[67] M5C0P SSD5_1 —	—	SIUL SMD SSD —	I/O	SMD	None, None	—	133	T23
PE[6]	PCR[68]	Option 0 Option 1 Option 2 Option 3	GPIO[68] M5C1M SSD5_2 —	—	SIUL SMD SSD —	I/O	SMD	None, None	—	134	R24
PE[7]	PCR[69]	Option 0 Option 1 Option 2 Option 3	GPIO[69] M5C1P SSD5_3 —	—	SIUL SMD SSD —	I/O	SMD	None, None	—	135	R23
PORT F											
PF[0]	PCR[70]	Option 0 Option 1 Option 2 Option 3	GPIO[70] eMIOS1[19] EVTO DCULITE_B2	—	SIUL PWM/Timer NEXUS DCULite	I/O	M	None, None	157	189	C20
PF[1]	PCR[71]	Option 0 Option 1 Option 2 Option 3	GPIO[71] eMIOS1[20] MSEO DCULITE_B3	—	SIUL PWM/Timer NEXUS DCULite	I/O	M	None, None	158	190	B20
PF[2]	PCR[72]	Option 0 Option 1 Option 2 Option 3	GPIO[72] NMI — —	—	SIUL NMI — —	I/O	S	None, None	45	53	AC7

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PF[3]	PCR[73]	Option 0 Option 1 Option 2 Option 3	GPIO[73] eMIOS1[21] MSEO DCULITE_B4	—	SIUL PWM/Timer NEXUS DCULite	I/O	M	None, None	159	191	A20
PF[4]	PCR[74]	Option 0 Option 1 Option 2 Option 3	GPIO[74] eMIOS1[14] SDA_1 DCULITE_B5	—	SIUL PWM/Timer I^2C_1 DCULite	I/O	M	None, None	160	192	D19
PF[5]	PCR[75]	Option 0 Option 1 Option 2 Option 3	GPIO[75] QUADSPI_IO1_B eMIOS1[15] VIU8_PDI16	—	SIUL QuadSPI PWM/Timer VIU2/PDI	I/O	M	None, None	161	193	A19
PF[6]	PCR[76]	Option 0 Option 1 Option 2 Option 3	GPIO[76] QUADSPI_IO0_B eMIOS1[16] VIU9_PDI17	—	SIUL QuadSPI PWM/Timer VIU2/PDI	I/O	M	None, None	162	194	D18
PF[7]	PCR[77]	Option 0 Option 1 Option 2 Option 3	GPIO[77] eMIOS1[15] SCL_1 DCULITE_B6	—	SIUL PWM/Timer I^2C_1 DCULite	I/O	M	None, None	163	195	C18
PF[8]	PCR[78]	Option 0 Option 1 Option 2 Option 3	GPIO[78] SDA_0 CS2_1 RXD_1	—	SIUL I^2C_0 DSPI_1 LINFlex_1	I/O	S	None, None	164	196	A18
PF[9]	PCR[79]	Option 0 Option 1 Option 2 Option 3	GPIO[79] SCL_0 CS1_1 TXD_1	—	SIUL I^2C_0 DSPI_1 LINFlex_1	I/O	S	None, None	165	197	D17
PF[10]	PCR[80]	Option 0 Option 1 Option 2 Option 3	GPIO[80] QUADSPI_PCS_A — EVTI	—	SIUL QuadSPI — NEXUS	I/O	M	None, None	169	201	A17
PF[11]	PCR[81]	Option 0 Option 1 Option 2 Option 3	GPIO[81] QUADSPI_IO2_A — MDO0	—	SIUL QuadSPI — NEXUS	I/O	M	None, None	170	202	D16

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PH[11]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[12]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PORT J											
PJ[0]	PCR[105]	Option 0 Option 1 Option 2 Option 3	GPIO[105] DCULITE_B6 — I2S_DO / PWMO	—	SIUL DCULite — SGM	I/O	M	None, None	—	—	L26
PJ[1]	PCR[106]	Option 0 Option 1 Option 2 Option 3	GPIO[106] VIU1_PDI_HSYNC eMIOS1[9] eMIOS0[8]	—	SIUL VIU2/PDI PWM/Timer PWM/Timer	I/O	S	None, None	4	4	U4
PJ[2]	PCR[107]	Option 0 Option 1 Option 2 Option 3	GPIO[107] VIU0_PDI_VSYNC eMIOS1[14] eMIOS0[9]	—	SIUL VIU2/PDI PWM/Timer PWM/Timer	I/O	S	None, None	5	5	U3
PJ[3]	PCR[108]	Option 0 Option 1 Option 2 Option 3	GPIO[108] VIU_PCLK eMIOS0[22] PDI_DE	—	SIUL VIU2 PWM/Timer PDI	I/O	S	None, None	60	72	AD15
PJ[4]	PCR[109]	Option 0 Option 1 Option 2 Option 3	GPIO[109] VIU2_PDI0 eMIOS0[21] eMIOS0[23]	—	SIUL VIU2/PDI PWM/Timer PWM/Timer	I/O	S	None, None	56	68	AD14
PJ[5]	PCR[110]	Option 0 Option 1 Option 2 Option 3	GPIO[110] VIU3_PDI1 eMIOS0[20] eMIOS0[16]	—	SIUL VIU2/PDI PWM/Timer PWM/Timer	I/O	M	None, None	57	69	AE14
PJ[6]	PCR[111]	Option 0 Option 1 Option 2 Option 3	GPIO[111] VIU4_PDI2 eMIOS0[19] eMIOS0[15]	—	SIUL VIU2/PDI PWM/Timer PWM/Timer	I/O	S	None, None	58	70	AF14

Table 11. Recommended operating conditions (5.0 V) (continued)

Symbol		C	Parameter	Conditions	Value		Unit	SpecID
					Min	Max		
V_{DDM}	SR	P	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})		+4.5	+5.5	V	D2.30
V_{DD_DR}[11]		P	Voltage on V_{DD_DR} with respect to V_{SS}		+1.62	+3.6	V	D2.31
V_{SS_DR}		D	Voltage on V_{SSRSDS} with respect to V_{SS}		+1.62	+3.6	V	D2.32
V_{RSDS}		P	Voltage on V_{DD_DR} with respect to V_{SS}		+3.0	+3.6	V	D2.33
TV_{DD}	SR	D	V_{DD} slope to ensure correct power up[12]			12	V/ms	D2.34
T_A	SR	P	Ambient temperature under bias		–40	105	°C	D2.35
					–40	105		
T_J	SR	D	Junction temperature under bias		–40	140		D2.36

1 100 nF capacitance needs to be provided between V_{DDA}/V_{SSA} pair.

2 Full functionality cannot be guaranteed when voltage drops below 4.5 V. In particular, I/O DC and ADC electrical characteristics may not be guaranteed below 4.5 V during the voltage drop sequence.

3 10 µF capacitance must be connected between V_{DDR} and V_{SS12}. It is recommended that this cap should be placed, as close as possible to the DUT pin on board.

4 V_{DD12} cannot be used to drive any external component.

5 Each V_{DD12}/V_{SS12} supply pair should have a 10 µF capacitor. Absolute combined maximum capacitance is 40 µF. Preferably, all the VDD12 supply pads should be shorted and then connected to a 4×10 µF capacitance. This is to ensure the ESR of external capacitance does not exceed 0.2 Ω. A 100 nF capacitor must be placed close to the pin.

6 V_{DD} refers collectively to I/O voltage supplies, i.e., V_{DDE_A}, V_{DDE_B}, V_{DDE_DR}, V_{DDMA}, V_{DDMB} and V_{DDMC}. VDDmin value for is 4.5 V for VDDE_A & VDDM, 3 V VDDE_B, while it is 1.62 V for VDD_DR. VDD max value is 5.5 V for VDDE_A & VDDM and 3.6 V for VDDE_B & VDD_DR.

7 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

8 V_{SS} refers collectively to I/O voltage supply grounds, i.e., V_{SSE_A}, V_{SSE_B}, V_{SSE_A}, V_{SSE_E}, V_{SSMA}, V_{SSMB} and V_{SSMC}) unless otherwise noted.

9 V_{DDE_A} should not be less than V_{DDA}.

10 VDDE_B cannot go beyond 3.6V under any operating condition.

11 VDD_DR can be 1.8, 2.5 and 3.3V (typical) based on type of SDR memory.

12 Guaranteed by device validation

4.5 Thermal characteristics

Table 12. Thermal characteristics for 176-pin LQFP[1]

Symbol		C	Parameter	Conditions	Value	Unit	SpecID
$R_{\theta JA}$	CC	D	Junction to Ambient Natural Convection[2]	Single layer board –1s	36	°C/W	D3.1
$R_{\theta JA}$	CC	D	Junction to Ambient Natural Convection[2]	Four layer board –2s2p	29	°C/W	D3.2
$R_{\theta JMA}$	CC	D	Junction to Ambient[2]	@200 ft./min., single layer board –1s	28	°C/W	D3.3
$R_{\theta JMA}$	CC	D	Junction to Ambient[2]	@200 ft./min., Four layer board –2s2p	23	°C/W	D3.4
$R_{\theta JB}$	CC	D	Junction to Board[3]		18	°C/W	D3.5
$R_{\theta JCtop}$	CC	D	Junction to Case (Top)[4]		5	°C/W	D3.6

[6] Flash in Low Power. RCOSC 128 kHz and RCOSC 16 MHz ON. 10 MHz XTAL clock. FlexCAN: instances: 0, 1ON (clocked but no reception or transmission), LINFLEX: instances 0, 1, 2 ON (clocked but no reception or transmission). eMIOS: instance: 0, 1 ON - 16 channels on with PWM20K Hz. DSPI: instance: 0 (clocked but no communication). DCUs, TCON, VIU, GPU clock gated, RTC/API ON.PIT ON. STM ON. ADC ON but not converting.

[7] No clock, RC 16MHz off, RCI 128 kHz on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

[8] ULPreg ON, HP/LPVreg off, 64 KB RAM on, device configured for minimum consumption, all possible modules switched off.

[9] 32 KHz oscillator operates at 32,768 Hz.

[10] ULPreg ON, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

4.8 DC electrical specifications

4.8.1 DC specification for CMOS090LP2 library @ VDDE = 3.3 V

NOTE

These pad specifications are applicable for pads in the Digital segment Only. See the "GPIO power bank supplies and functionality" table in the "Voltage Regulators and Power Supplies" chapter of the reference manual for details.

Table 21. DC electrical specifications

Symbol		C	Parameter	Condition	Value		Unit	SpecID
					Min	Max		
Vdd	SR	P	Core supply voltage	—	1.08	1.47	V	D9.1
Vdde	SR	P	I/O supply voltage	—	3.0	3.6	V	D9.2
Vdd33	SR	P	I/O pre-driver supply voltage	—	3.0	3.6	V	D9.3
Vih_c	SR	P	CMOS input buffer high voltage	With hysteresis enabled	0.65 × Vdde	Vdde + 0.3	V	D9.4
				With hysteresis disabled	0.55 × Vdde	Vdde + 0.3		
Vil_c	SR	P	CMOS input buffer low voltage	With hysteresis enabled	Vss – 0.3	0.35 × Vdde	V	D9.5
				With hysteresis disabled	Vss – 0.3	0.40 × Vdde		
Vhys_c	SR	T	CMOS input buffer hysteresis	—	0.1 × Vdde	—	V	D9.6
Vih_fod_h	SR	P	5 V tolerant CMOS input buffer high voltage	With hysteresis enabled	0.65 × Vdd33	Vdd33 + 0.3	V	D9.7
Vil_fod_h	SR	P	5 V tolerant CMOS input buffer low voltage	With hysteresis enabled	Vss – 0.3	0.35 × Vdd33	V	D9.8
Iact_s	SR	T	Selectable weak pullup/pulldown current	—	25	150	µA	D9.9
Iinact_d	SR	P	Digital pad input leakage current	Weak pull inactive	–2.5	2.5	µA	D9.10
Iinact_a	SR	P	Analog pad input leakage current	Weak pull inactive	–150	150	µA	D9.11
Voh	SR	P	Output high voltage	—	0.8 × Vdde	—	V	D9.12

Table 26. Supply leakage (continued)

Pad	VDD		VDDE		VDD33	
	Typ	Max	Typ	Max	Typ	Max
pad_esdspacer_hv	—	—	—	—	—	—
pad_tgate_hv	—	—	—	—	—	—
pad_vdd33_hv	—	—	—	—	—	—
pad_vdde_hv	0	0	—	—	0	0
pad_vddint3v_hv	0	0	—	—	0	0
pad_vddint_hv	0	0	—	—	—	—
pad_vss_hv	0	0	—	—	—	—
pad_vsse_hv	0	0	—	—	—	—
pad_vssint3v_hv	0	0	—	—	—	—
pad_vssint_hv	0	0	—	—	—	—
spcr_17_82_hv	—	—	—	—	—	—
spcr_35_84_hv	—	—	—	—	—	—
spcr_71_88_hv	—	—	—	—	—	—
spcr_143_38_hv	—	—	—	—	—	—
spcr_vdde_lvl_hv	—	—	—	—	—	—

Table 27. AVG IDDE specifications

Cell	Period (ns)	Load (pF)[1]	VDDE (V)	Drive/slew select	IDDE (mA)
pad_msr_hv[2]	24	50	5.5	11	14
	62	50	5.5	01	5.3
	317	50	5.5	00	1.1
	425	200	5.5	00	3
pad_ssr_hv[2]	37	50	5.5	11	9
	130	50	5.5	01	2.5
	650	50	5.5	00	0.5
	840	200	5.5	00	1.5

1 All loads are lumped loads.

2 Average current is for pad configured as output only. Use pad_i current for input.

Table 36. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit	SpecID
					Min	Typ	Max		
V_{IH}	SR	P	Input High Level CMOS Schmitt Trigger	—	0.65 V_{DD}	—	V_{DD} + 0.4	V	D8.1
V_{IL}	SR	P	Input low Level CMOS Schmitt Trigger	—	–0.4	—	0.35 V_{DD}	V	D8.2
V_{HYS}	CC[3]	D	Input hysteresis CMOS Schmitt Trigger	—	0.1 V_{DD}	—	—	V	D8.3
V_{OL}	CC[4]	P	Output low level	Push Pull, I_{OL} = 2mA, V_{DD} = 5.0V ± 10%, ipp_hve = 0 (recommended)	—	—	0.1 V_{DD}	V	D8.4
		D		Push Pull, I_{OL} = 1mA, V_{DD} = 5.0V ± 10%, ipp_hve = 1[5]	—	—	0.1 V_{DD}		
		C		Push Pull, I_{OL} = 1mA, V_{DD} = 3.3V ± 10%, ipp_hve = 1 (recommended)	—	—	0.5		
T_{tr}	CC[4]	T	Output transition time output pin[6] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0V ± 10%, ipp_hve = 0	—	—	10	ns	D8.5
				C_L = 50pF, V_{DD} = 5.0V ± 10%, ipp_hve = 0	—	—	20		
				C_L = 100pF, V_{DD} = 5.0V ± 10%, ipp_hve = 0	—	—	40		
				C_L = 25pF, V_{DD} = 3.3V ± 10%, ipp_hve = 1	—	—	12		
				C_L = 50pF, V_{DD} = 3.3V ± 10%, ipp_hve = 1	—	—	25		
				C_L = 100pF, V_{DD} = 3.3V ± 10%, ipp_hve = 1	—	—	40		
W_{FRST}	SR	P	$\overline{\text{RESET}}$ Input Filtered Pulse	—	—	—	70	ns	D8.6
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ Input Not Filtered Pulse	—	400	—	—	ns	D8.7
$\lvert I_{WPU} \rvert$	CC[4]	P	Weak pullup current absolute value	—	10	—	—	µA	D8.8

1 V_{DD} = 3.3V ±10% / 5.0V ±10%, T_A = –40 to +105°C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Data based on characterization results, not tested in production

4 Guaranteed by design simulation.

5 This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of the reference manual).

6 C_L calculation should include device and package capacitance (C_{PKG} < 5pF).

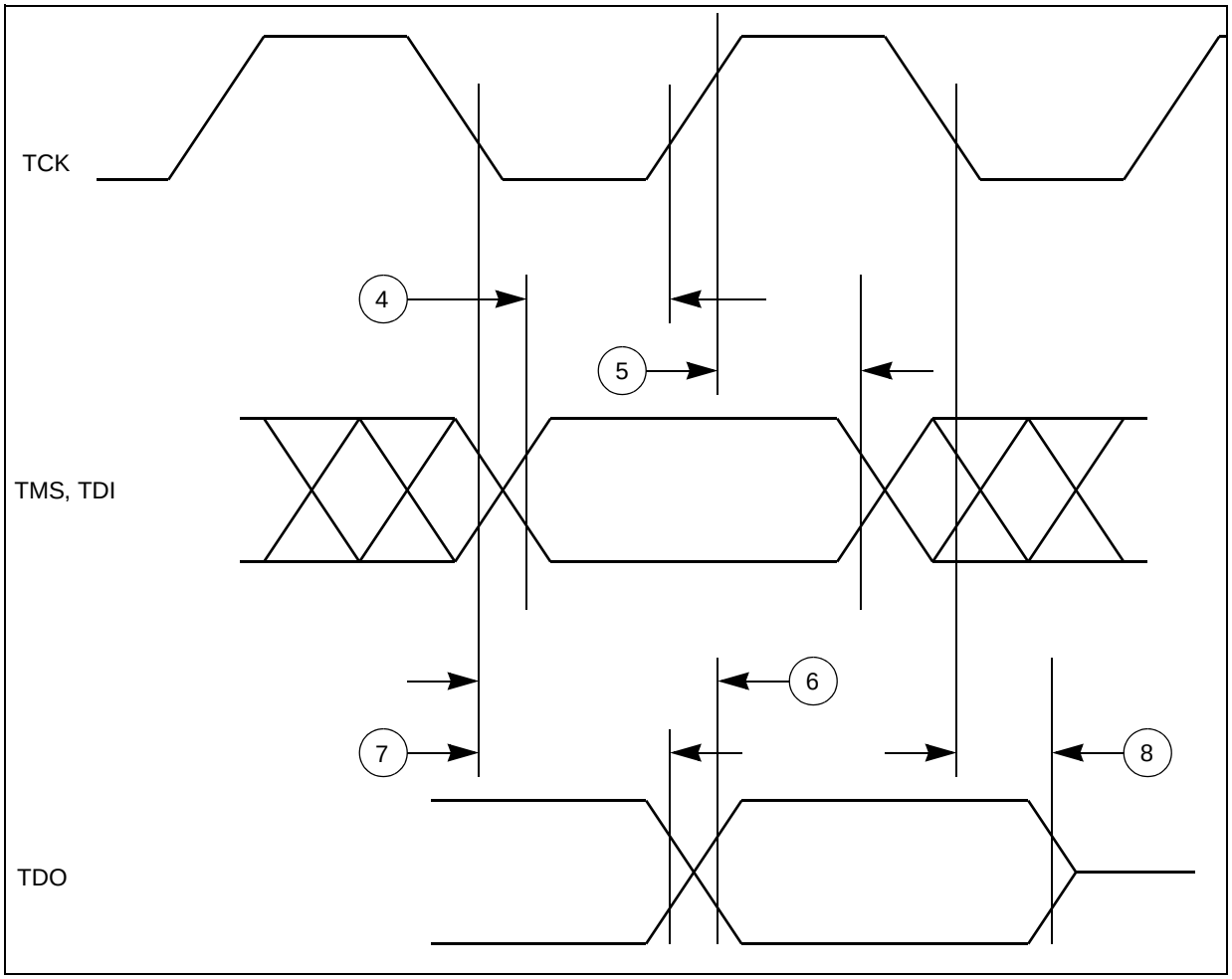

Figure 19. JTAG test access port timing

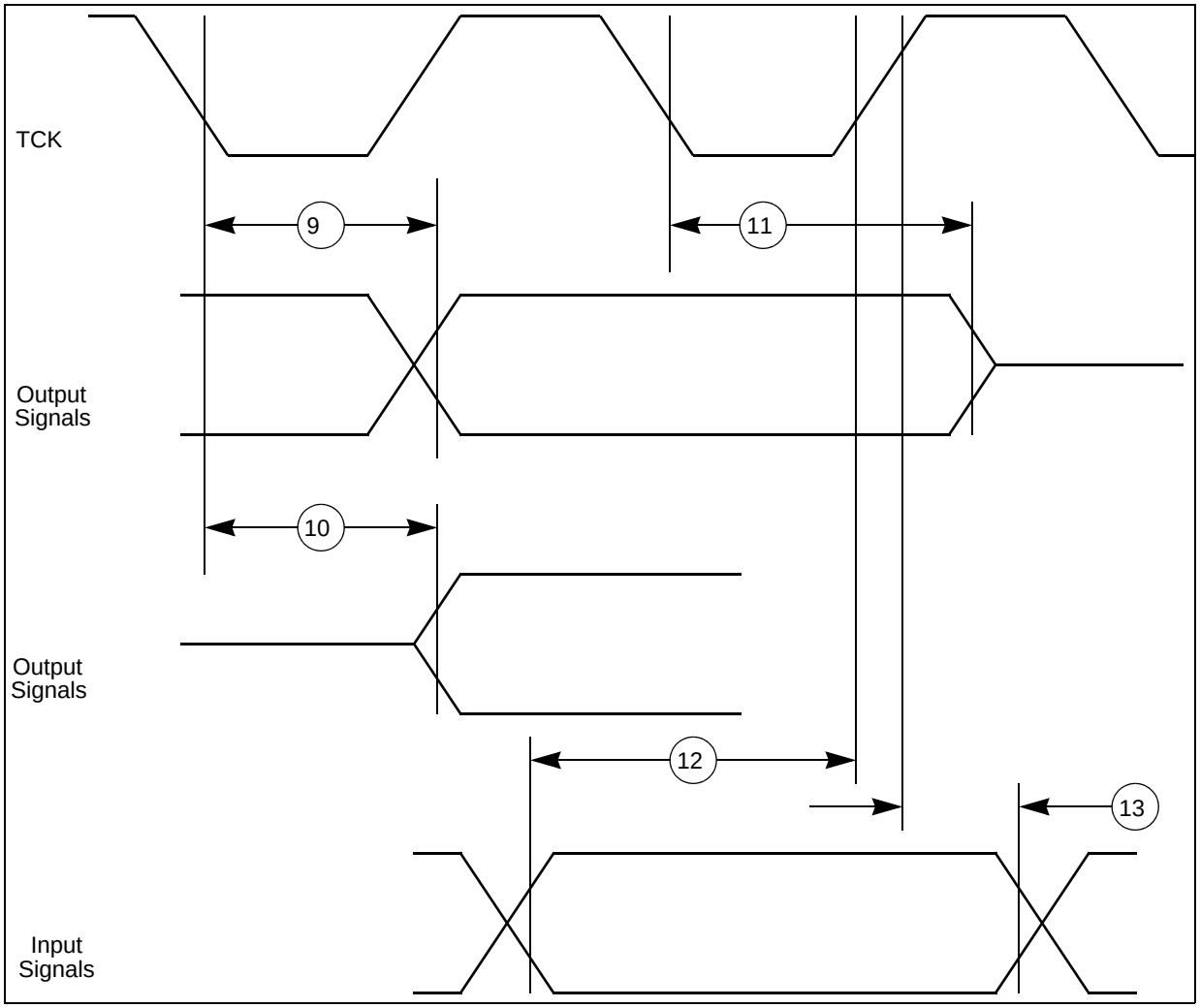

Figure 20. JTAG boundary scan timing

- PCLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, PCLK runs continuously. This signal frequency could be from 5 to 66 MHz depending on the panel type.
- HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

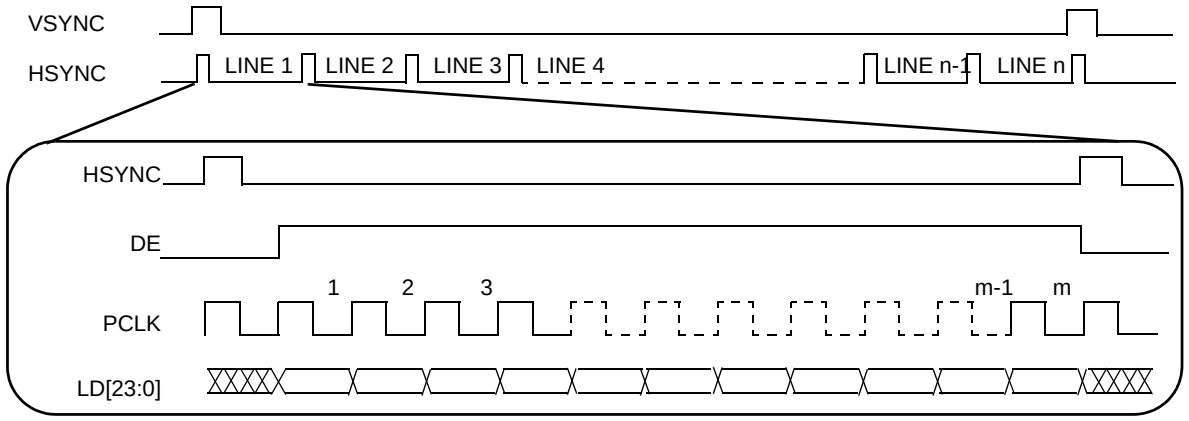

Figure 24. TFT LCD interface timing overview[1]

4.18.3.1 Interface to TFT LCD panels—pixel level timings

Figure 25 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high.

Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the DCU Clock Confide Register (DCCR) in the system clock module.

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

1. In Figure 24, the “LD[23:0]” signal is “line data,” an aggregation of the DCU’s RGB signals—R[0:7], G[0:7] and B[0:7].

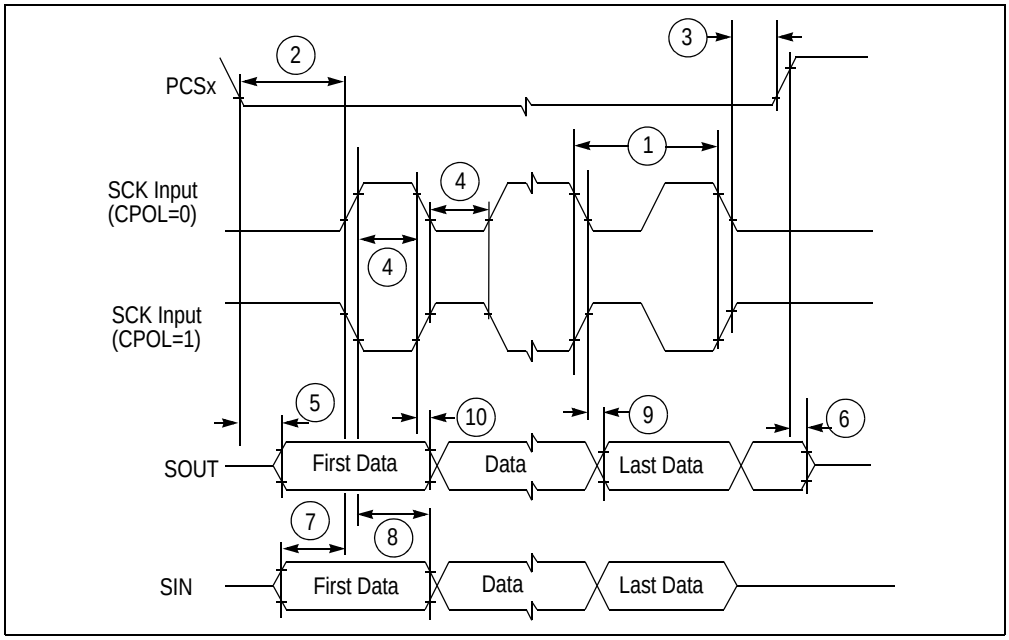

Figure 35. DSPI classic SPI timing — Slave, CPHA = 0

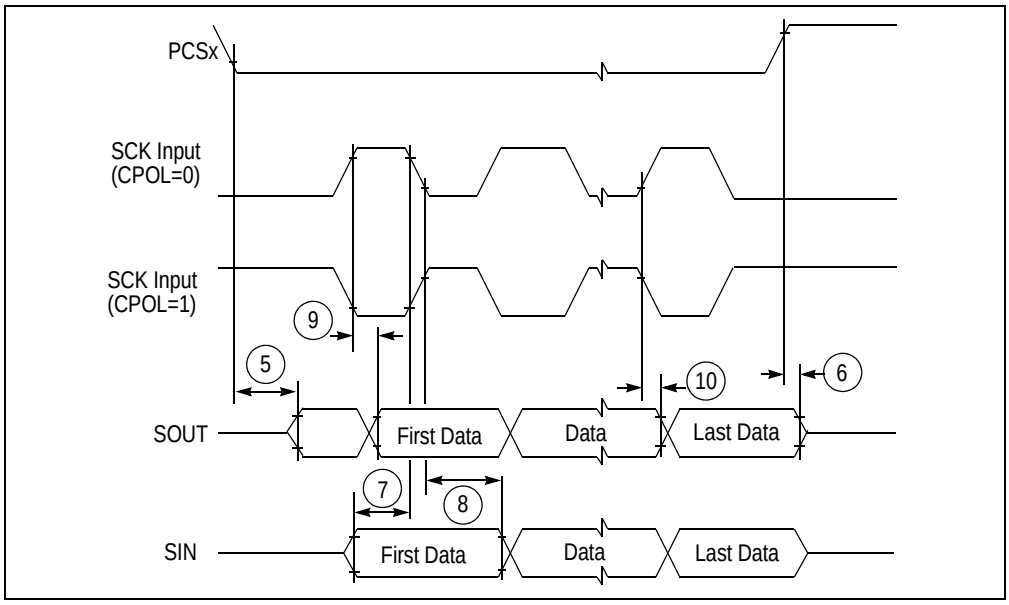

Figure 36. DSPI classic SPI timing — Slave, CPHA = 1

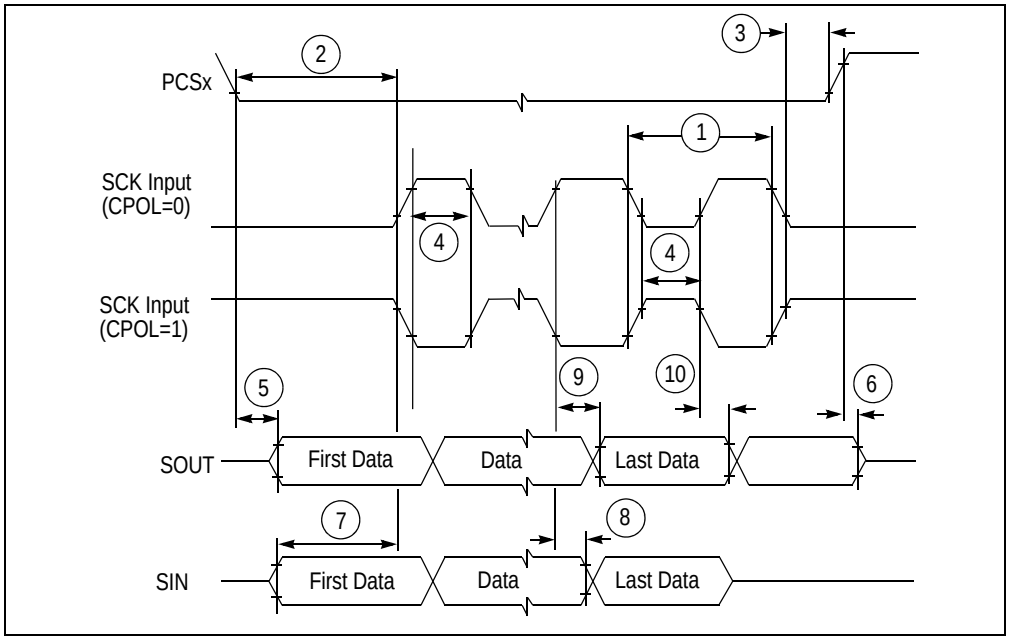

Figure 39. DSPI modified transfer format timing — Slave, CPHA = 0

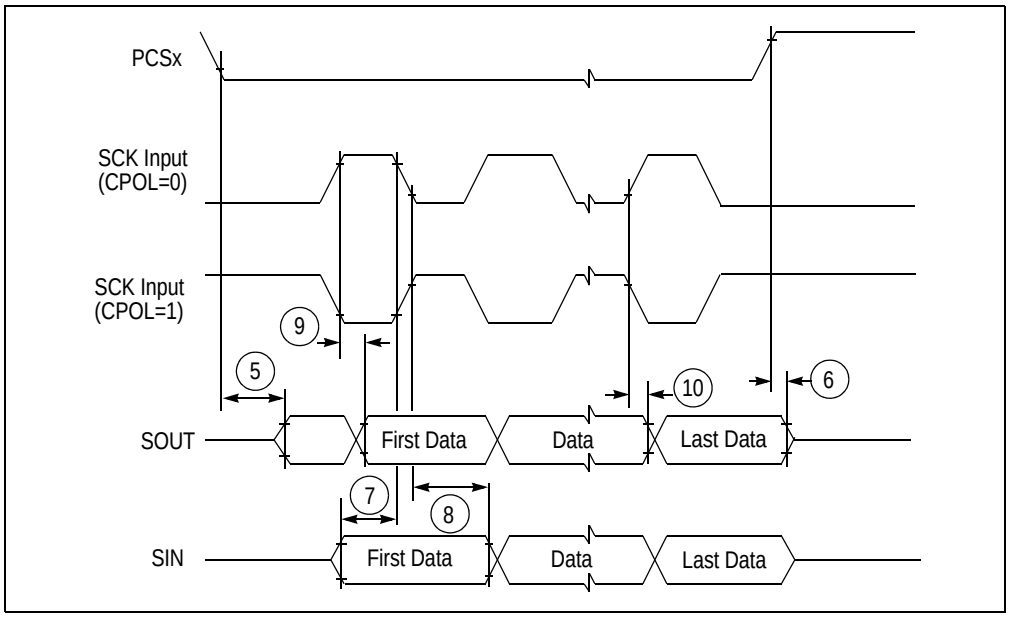

Figure 40. DSPI modified transfer format timing — Slave, CPHA = 1

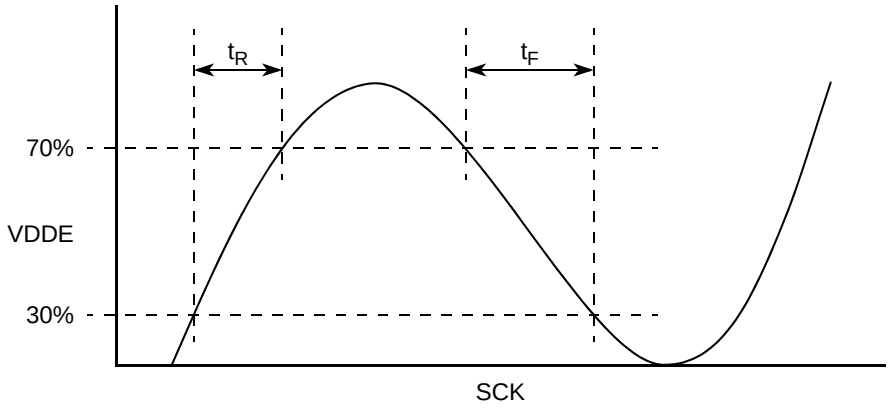

Figure 44. QuadSPI clock profile

4.18.13 TCON/RSDS timing

The following notes apply to Table 71:

- Measurement condition: Vdde/Vdd33 = 3.3 V ± 10%, Vdd = 1.2 V ± 10%, Vss/Vsse = 0 V, T = –40 to 105°C
- Termination: 100 Ω ± 5%
- VREFH_RSDS terminations of 47 µF

Table 71. TCON/RSDS timing

Symbol		C	Parameter	Condition	Value			Unit	SpecID
					Min	Typ	Max		
V_{OD}	CC	C	Differential output voltage	RSDS mode	391	—	471	mV	A14.1
V_{OS}	CC	C	Common mode voltage	100 Ω termination between Pad_p and Pad_n	1.17	—	1.4	V	A14.2
tr	CC	C	Rise time	Transition from 20% to 80%	606	—	844	ps	A14.3
tf	CC	C	Fall time	Transition from 20% to 80%	607	—	842	ps	A14.4
tplh	CC	D	Propagation delay, low to high	—	—	2.65	—	ns	A14.5
tphl	CC	D	Propagation delay, high to low	—	—	2.47	—	ns	A14.6
tdz	CC	D	Start-up time	—	—	200	—	µs	A14.7
tskew[1 2 3]	CC	C	Skew between different RSDS lines	Max and min skew between clock and data pads	—	—	—	ps	A14.8

1 There are eight programmable bits to provide 256 different skew numbers with various combinations of these bits.

2 Default value of all the eight skew options are all “1”.

3 All “0” combination of eight bits is not valid.