Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	125MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	128
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpxd2020vlu125

  - Interfaces to external, memory-mapped serial flash memories
  - Supports simultaneous addressing of 2 external serial flashes to achieve up 80 MB/s read bandwidth
- RLE decoder supporting memory to memory decoding of RLE data in conjunction with eDMA
- Four local interconnect network (LINFlex) controller modules
  - Capable of autonomous message handling (master), autonomous header handling (slave mode), and UART support
  - Compliant with LIN protocol rev 2.1
- Three controller-area network (FlexCAN) modules
  - Compliant with the CAN protocol version 2.0 C
  - 64 configurable buffers
  - Programmable bit rate of up to 1 Mb/s
- Four Inter-Integrated Circuit (I^2C) internal bus controllers with master/slave bus interface
- Low-power loop controlled pierce crystal oscillator supporting 4–16MHz external crystal or resonator
- Real Time Counter (RTC) with clock source from internal 128 kHz or 16 MHz oscillator supporting autonomous wake-up with 1 ms resolution with maximum timeout of 2 seconds
  - Support for real time counter (RTC) with clock source from external 32 KHz crystal oscillator, supporting wake-up with 1 s resolution and maximum timeout of one hour
  - RTC optionally clocked by fast 4–16 MHz external oscillator
- System timers:
  - Four-channel 32-bit System Timer Module (STM)
  - Eight-channel 32-bit Periodic Interrupt Timer (PIT) module (including ADC trigger)
  - Software Watchdog Timer (SWT)
- System Integration Unit Lite (SIUL) module to manage external interrupts, GPIO and pad control
- System Status and Configuration Module (SSCM)
  - Provides information for identification of the device, last boot mode, or debug status
  - Provides an entry point for the censorship password mechanism
- Clock Generation Module (MC_CGM) to generate system clock sources and provide a unified register interface, enabling access to all clock sources
- Clock Monitor Unit (CMU)
  - Monitors the integrity of the fast (4–16 MHz) external crystal oscillator and the primary FMPLL (FMPLL0)
  - Acts as a frequency meter, measuring the frequency of one clock source and comparing it to a reference clock
- Mode Entry Module (MC_ME)
  - Controls the device power mode, i.e., RUN, HALT, STOP, or STANDBY
  - Controls mode transition sequences
  - Manages the power control, voltage regulator, clock generation and clock management modules
- Power Control Unit (MC_PCU) to implement standby mode entry/exit and control connections to power domains
- Reset Generation Module (MC_RGM) to manage reset assertion and release to the device at initial power-up
- Nexus Development Interface (NDI) per IEEE-ISTO 5001-2008 Class 3 standard with additional Class 4 features:
  - Watchpoint Triggering
  - Processor Overrun Control
- Device/board boundary-scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator controller for regulating the 3.3–5 V supply voltage down to 1.2 V for core logic (requires external ballast transistor)
- Package:[1]
  - 176 LQFP, 0.5 mm pitch, 24 mm × 24 mm outline

1. See the device comparison table for package offerings for each device in the family.

— 208 LQFP, 0.5 mm pitch, 28 mm × 28 mm outline
— 416 TEPBGA, 1mm ball pitch, 27 mm × 27 mm outline

1.4 Feature details

1.4.1 Low-power operation

The PXD20 is designed for optimized low-power operation and dynamic power management of the CPU and peripherals. Power management features include software-controlled clock gating of peripherals and multiple power domains to minimize leakage in low-power modes.

There are three low-power modes:

- STANDBY
- STOP
- HALT

and five dynamic power modes — RUN[0..3] and DRUN. All low-power modes use clock gating to halt the clock for all or part of the device.

STANDBY mode turns off the power to the majority of the chip to offer the lowest power consumption mode.

The device can be awakened from STANDBY mode via from any of up to 23 I/O pins, a reset or from a periodic wake-up using a low power oscillator. If required, it is possible to enable the internal 16 MHz oscillator, the external 4–16 MHz oscillator and the external 32 KHz oscillator.

In STANDBY mode the contents of the CPU, on-chip peripheral registers and potentially some of the volatile memory are lost. The two possible configurations in STANDBY mode are:

- The device retains 64 KB of the on-chip SRAM, but the content of the graphics SRAM is lost.
- The device retains 8 KB of the on-chip SRAM, but the content of the graphics SRAM is lost.

STOP mode maintains power to the entire device allowing the retention of all on-chip registers and memory, and providing a faster recovery low power mode than the lowest-power STANDBY mode. There is no need to reconfigure the device before executing code. The clocks to the CPU and peripherals are halted and can be optionally stopped to the oscillator or PLL at the expense of a slower start-up time.

STOP is entered from RUN mode only. Wake-up from STOP mode is triggered by an external event or by the internal periodic wake-up, if enabled.

RUN modes are the main operating modes where the entire device can be powered and clocked and from which most processing activity is done. Four dynamic RUN modes are supported—RUN0 - RUN3. The ability to configure and select different RUN modes enables different clocks and power configurations to be supported with respect to each other and to allow switching between different operating conditions. The necessary peripherals, clock sources, clock speed and system clock prescalers can be independently configured for each of the four RUN modes of the device.

HALT mode is a reduced activity, low power mode intended for moderate periods of lower processing activity. In this mode the CPU system clocks are stopped but user-selected peripheral tasks can continue to run. It can be configured to provide more efficient power management features (switch-off PLL, flash memory, main regulator, etc.) at the cost of longer wake up latency. The system returns to RUN mode as soon as an event or interrupt is pending.

Table 2 summarizes the operating modes of the PXD20.

Table 2. Operating mode summary[1]

Operating mode	SoC features					Clock sources						Periodic Wake-up	Wake-up input	VREG mode	Wake-up time[2]						
	CPU GFX accelerator DRAM controller	Peripherals	Flash	RAM	Graphics RAM	Primary PLL	Auxiliary PLL	16 MHz IRC	4–16 MHz OSC	128 kHz IRC	32 KHz X OSC				VREG start-up	IRC Wake-up	Flash Recovery	OSC Stabilization	PLL Lock	S/W Reconfig	Mode switch over
RUN	On	OP	OP	OP[3]	On	OP	OP	On	OP	On	OP	—	—	FP	—	—	—	—	—	—	—
HALT	CG	OP	OP	OP[3]	On	OP	OP	On	OP	On	OP	OP	OP	FP	—	—	—	—	—	—	TBD
STOP	CG	CG	CG	OP[3]	On	CG	CG	OP	OP	On	OP	OP	OP	LP	350 µs	4 µs	20 µs	1 ms	200 µs	—	24 µs
STANDBY	Off	Off	Off	64 KB[4]	Off	Off	Off	OP	OP	OP	OP	OP	OP	LP	350 µs	8 µs	100 µs	1 ms	200 µs	Var	28 µs
	Off	Off	Off	8 KB[5]	Off	Off	Off	OP	OP	OP	OP	OP	OP	LP	200 µs	8 µs	100 µs	1 ms	200 µs	Var	28 µs
POR															500 µs	8 µs	100 µs	1 ms	200 µs		BAM[6]

1 Table Key:

On—Powered and clocked

OP—Optionally configurable to be enabled or disabled (clock gated)

CG—Clock Gated, Powered but clock stopped

Off-—Powered off and clock gated

FP—VREG Full Performance mode

LP—VREG Low Power mode, reduced output capability of VREG but lower power consumption

Var—Variable duration, based on the required reconfiguration and execution clock speed

BAM—Boot Assist Module Software and Hardware used for device start-up and configuration

2 A high level summary of some key durations that need to be considered when recovering from low power modes. This does not account for all durations at wake up. Other delays will be necessary to consider including, but not limited to the external supply start-up time.
IRC Wake-up time must not be added to the overall wake-up time as it starts in parallel with the VREG.
All other wake-up times must be added to determine the total start-up time.

3 Either 64 KB or 8 KB available.

4 64 KB of the RAM contents is retained, but not accessible in STANDBY mode.

5 8 KB of the RAM contents is retained, but not accessible in STANDBY mode.

6 Dependent on boot option after reset.

Additional notes on low power operation:

- Fast wake-up using the on-chip 16 MHz internal RC oscillator allows rapid execution from RAM on exit from low power modes
- The 16 MHz internal RC oscillator supports low speed code execution and clocking of peripherals when it is selected as the system clock and can also be used as the PLL input clock source to provide fast start-up without the external oscillator delay
- The device includes an internal voltage regulator that includes the following features:

  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
    - Parity, noise and framing errors
  - Interrupt driven operation with 4 interrupts sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods
- LIN features:
  - Autonomous LIN frame handling
  - Message buffer to store identifier and up to eight data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors
  - Sync field; Delimiter; ID parity; Bit, Framing; Checksum and Timeout errors
  - Classic or extended checksum calculation
  - Configurable Break duration of up to 36-bit times
  - Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features
    - Loop back
    - Self Test
    - LIN bus stuck dominant detection
  - Interrupt driven operation with 16 interrupt sources
  - LIN slave mode features
    - Autonomous LIN header handling
    - Autonomous LIN response handling
    - Discarding of irrelevant LIN responses using up to 16 ID filters

1.4.25 Inter-Integrated Circuit (I^2C) controller modules

The PXD20 includes four I^2C modules. Each module features the following:

- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I^2C bus standard
- Multi-master operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

- Data Trace via Data Write Messaging (DWM) and Data Read Messaging (DRM). This provides the capability for the development tool to trace reads and/or writes to selected internal memory resources.
- Ownership Trace via Ownership Trace Messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An Ownership Trace Message is transmitted when a new process/task is activated, allowing the development tool to trace ownership flow.
- Run-time access to embedded processor memory map via the JTAG port. This allows for enhanced download/upload capabilities.
- Watchpoint Messaging via the auxiliary pins
- Watchpoint Trigger enable of Program and/or Data Trace Messaging
- Data Acquisition Messaging (DQM) allows code to be instrumented to export customized information to the Nexus Auxiliary Output Port.
- Address Translation Messaging via program correlation messages displays updates to the TLB for use by the debugger in correlating virtual and physical address information
- Auxiliary interface for higher data input/output
- Registers for Program Trace, Data Trace, Ownership Trace and Watchpoint Trigger.
- All features controllable and configurable via the JTAG port

Table 3. Voltage supply pin descriptions (continued)

Supply pin	Function	Pin number		
		176 LQFP	208 LQFP	416 TEPBGA
V_{SS}	1.2 V ground	7, 18, 36, 49, 66, 68, 111, 123, 133, 139, 154, 167, 176	7, 18, 38, 47, 57, 64, 78, 80, 137, 147, 157, 163, 185, 199, 208	AB3,AD10,AD16,AD4,AE13,AE19,AE2,AE7,B11,B14,B19,B2,B25,B5,B8,C12,C15,C17,C21,C3,C6,C9,E2,E24,F3,H2,H25,J3,K11,K13,K15,K17,K24,L10,L12,L14,L16,L2,M11,M12,M13,M14,M15,M17,M3,N10,N12,N13,N14,N15,N16,P11,P12,P13,P14,P15,P17,P2,P25,R10,R12,R13,R14,R15,R16,R3,T11,T13,T15,T17,U10,U12,U14,U16,V2,Y1
	VDD12 ground and VDDPLL ground (VSSPLL)	24	24	—
V_{DDE_B}	3.3 V I/O supply. This supply is shared with internal flash, 16 MHz IRC oscillator and 4–16MHz crystal oscillator.	6, 19, 37, 48, 65, 89, 112, 122, 132, 140, 166	6, 19, 37, 48, 56, 63, 77, 105, 138, 146, 156, 164, 184, 198	AD13,AD19,AD2,AD7,AE10,AE16,AE4,B17,B21,B24,C19,E25,H24,L25,N24,W3
V_{DDA}[2]	3.3 V/5 V reference voltage and analog supply for A/D converter. This supply is shared with the SXOSC.	79	95	AC22
V_{SSA}	Reference ground and analog ground for A/D converter	80	96	AD22
V_{DDR}	Voltage regulator VREG supply	20	20	AA4
V_{SSR}	Voltage regulator ground	21	21	—
V_{DDE_A}[2]	3.3 V/5 V I/O supply. This supply is shared with the SXOSC.	77	93	AD23
V_{SSE_A}	3.3 V/5 V I/O supply ground	78	94	AC23
V_{DDM}	Stepper motor 3.3 V/5 V pad supply. SSD shares this supply.	94, 104	110, 120, 130	U25,W24,AA25
V_{SSM}	Stepper motor ground	95, 105	111, 121, 131	U24,W24,AA24
V_{DDPLL}	1.2 V PLL supply	25	25	AB4
V_{SUP_TEST}[3]	9 V - 12 V flash test analog write signal	22	22	AC1
V_{DD_DR}	1.8V, 2.5V, and 3.3V DDR SDRAM supply	—	—	C2,C5,C8,C11,C14,E3,H3,L3,N3,T3
V_{DD33_DR}	Functional supply for SDRAM pads (where available must be >= VDD_DR)	—	—	D6, D12, F4, R4

Table 6. DRAM interface pin summary (continued)

Port pin[1]	Function	I/O direction	Pad type	PCR	RESET config[2]	Pin number
						416 TEPBGA
DDR_DQ[11]	DRAM Data Bus [11]	I/O	DDR	PCR[257]	None, None	J1
DDR_DQ[10]	DRAM Data Bus [10]	I/O	DDR	PCR[258]	None, None	K4
DDR_DQ[9]	DRAM Data Bus [9]	I/O	DDR	PCR[259]	None, None	K1
DDR_DQ[8]	DRAM Data Bus [8]	I/O	DDR	PCR[260]	None, None	L1
DDR_DQ[7]	DRAM Data Bus [7]	I/O	DDR	PCR[261]	None, None	L4
DDR_DQ[6]	DRAM Data Bus [6]	I/O	DDR	PCR[262]	None, None	M4
DDR_DQ[5]	DRAM Data Bus [5]	I/O	DDR	PCR[263]	None, None	M1
DDR_DQ[4]	DRAM Data Bus [4]	I/O	DDR	PCR[264]	None, None	N4
DDR_DQ[3]	DRAM Data Bus [3]	I/O	DDR	PCR[265]	None, None	N1
DDR_DQ[2]	DRAM Data Bus [2]	I/O	DDR	PCR[266]	None, None	P4
DDR_DQ[1]	DRAM Data Bus [1]	I/O	DDR	PCR[267]	None, None	P1
DDR_DQ[0]	DRAM Data Bus [0]	I/O	DDR	PCR[268]	None, None	R1
DRAM Data Strobes						
DDR_DQS[3]	DRAM Data Strobe [3]	I/O	DDR	PCR[232]	None, None	B3
DDR_DQS[2]	DRAM Data Strobe [2]	I/O	DDR	PCR[231]	None, None	G2
DDR_DQS[1]	DRAM Data Strobe [1]	I/O	DDR	PCR[230]	None, None	K2
DDR_DQS[0]	DRAM Data Strobe [0]	I/O	DDR	PCR[229]	None, None	N2
DRAM Data Enables						
DDR_DM[3]	DRAM Data Enable [3]	Output	DDR	PCR[236]	Output, None	B4
DDR_DM[2]	DRAM Data Enable [2]	Output	DDR	PCR[235]	Output, None	G3
DDR_DM[1]	DRAM Data Enable [1]	Output	DDR	PCR[234]	Output, None	K3
DDR_DM[0]	DRAM Data Enable [0]	Output	DDR	PCR[233]	Output, None	P3
DRAM Address						
DDR_A[15]	DRAM address [15]	Output	DDR	PCR[217]	Output, None	B15
DDR_A[14]	DRAM address [14]	Output	DDR	PCR[216]	Output, None	D15
DDR_A[13]	DRAM address [13]	Output	DDR	PCR[215]	Output, None	D14
DDR_A[12]	DRAM address [12]	Output	DDR	PCR[214]	Output, None	A14
DDR_A[11]	DRAM address [11]	Output	DDR	PCR[213]	Output, None	D13

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PA[14]	PCR[14]	Option 0 Option 1 Option 2 Option 3	GPIO[14] DCU_G6 — —	RSDS7P	SIUL DCU3 — —	I/O	M / RSDS	None, none	134	158	F24
PA[15]	PCR[15]	Option 0 Option 1 Option 2 Option 3	GPIO[15] DCU_G7 — —	RSDS7M	SIUL DCU3 — —	I/O	M / RSDS	None, none	135	159	F23
PORT B											
PB[0]	PCR[16]	Option 0 Option 1 Option 2 Option 3	GPIO[16] CANTX_0 TXD_0 —	—	SIUL FlexCAN_0 LINFlex_0 —	I/O	S	None, none	13	13	W4
PB[1]	PCR[17]	Option 0 Option 1 Option 2 Option 3	GPIO[17] CANRX_0 RXD_0 —	—	SIUL FlexCAN_0 LINFlex_0 —	I/O	S	None, none	12	12	V1
PB[2]	PCR[18]	Option 0 Option 1 Option 2 Option 3	GPIO[18] TXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, none	153	183	D21
PB[3]	PCR[19]	Option 0 Option 1 Option 2 Option 3	GPIO[19] RXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, none	152	182	A22
PB[4]	PCR[20]	Option 0 Option 1 Option 2 Option 3	GPIO[20] SCK_1 MA0 —	—	SIUL DSPI_1 ADC —	I/O	S	None, none	62	74	AF15
PB[5]	PCR[21]	Option 0 Option 1 Option 2 Option 3	GPIO[21] SOUT_1 MA1 FABM	—	SIUL DSPI_1 ADC Control	I/O	S	Input, pull-down	63	75	AC16

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PB[6]	PCR[22]	Option 0 Option 1 Option 2 Option 3	GPIO[22] SIN_1 MA2 ABS[0]	—	SIUL DSPI_1 ADC Control	I/O	S	Input, pull-up	64	76	AF16
PB[7]	PCR[23]	Option 0 Option 1 Option 2 Option 3	GPIO[23] SIN_0 eMIOS1[20] I2S_SCK/PWMOA	—	SIUL DSPI_0 PWM/Timer SGM	I/O	S	None, none	55	67	AC14
PB[8]	PCR[24]	Option 0 Option 1 Option 2 Option 3	GPIO[24] SOUT_0 eMIOS1[19] I2S_DO/PWMO	—	SIUL DSPI_0 PWM/Timer SGM	I/O	S	None, none	54	66	AF13
PB[9]	PCR[25]	Option 0 Option 1 Option 2 Option 3	GPIO[25] SCK_0 eMIOS1[18] I2S_FS	—	SIUL DSPI_0 PWM/Timer SGM	I/O	M	None, none	53	65	AC13
PB[10]	PCR[26]	Option 0 Option 1 Option 2 Option 3	GPIO[26] CANRX_1 I2S_DO/PWMO —	—	SIUL FlexCAN_1 SGM —	I/O	S	None, none	14	14	W2
PB[11]	PCR[27]	Option 0 Option 1 Option 2 Option 3	GPIO[27] CANTX_1 SGM_MCLK —	—	SIUL FlexCAN_1 SGM —	I/O	S	None, none	15	15	Y4
PB[12]	PCR[28]	Option 0 Option 1 Option 2 Option 3	GPIO[28] RXD_1 eMIOS1[10] CS2_0	—	SIUL LINFlex_1 PWM/Timer DSPI_0	I/O	S	None, none	46	54	AF7
PB[13]	PCR[29]	Option 0 Option 1 Option 2 Option 3	GPIO[29] TXD_1 eMIOS1[11] CS1_0	—	SIUL LINFlex_1 PWM/Timer DSPI_0	I/O	S	None, none	47	55	AC8
PB[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PB[15]	—	—	Reserved	—	—	—	—	—	—	—	—

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PN[8]	PCR[169]	Option 0 Option 1 Option 2 Option 3	GPIO[169] DCULITE_R6 — TCON[10]	—	SIUL DCULite — TCON	I/O	M	None, None	—	—	AC12
PN[9]	PCR[170]	Option 0 Option 1 Option 2 Option 3	GPIO[170] DCULITE_R7 — TCON[11]	—	SIUL DCULite — TCON	I/O	M	None, None	—	—	AD12
PN[10]	PCR[171]	Option 0 Option 1 Option 2 Option 3	GPIO[171] DCULITE_G0 RXD_3 VIU2_PDI10	—	SIUL DCULite LINFlex_3 VIU2/PDI	I/O	M	None, None	—	—	AE12
PN[11]	PCR[172]	Option 0 Option 1 Option 2 Option 3	GPIO[172] DCULITE_G1 TXD_3 VIU3_PDI11	—	SIUL DCULite LINFlex_3 VIU2/PDI	I/O	M	None, None	—	—	AF12
PN[12]	PCR[173]	Option 0 Option 1 Option 2 Option 3	GPIO[173] DCULITE_G2 — eMIOS0[17]	—	SIUL DCULite — PWM/Timer	I/O	M	None, None	—	—	R26
PN[13]	PCR[174]	Option 0 Option 1 Option 2 Option 3	GPIO[174] DCULITE_G3 — eMIOS0[18]	—	SIUL DCULite — PWM/Timer	I/O	M	None, None	—	—	R25
PN[14]	PCR[175]	Option 0 Option 1 Option 2 Option 3	GPIO[175] DCULITE_G4 — eMIOS0[19]	—	SIUL DCULite — PWM/Timer	I/O	M	None, None	—	—	P26
PN[15]	PCR[176]	Option 0 Option 1 Option 2 Option 3	GPIO[176] DCULITE_G5 — eMIOS0[20]	—	SIUL DCULite — PWM/Timer	I/O	M	None, None	—	—	P24
PORT P											
PP[0]	PCR[177]	Option 0 Option 1 Option 2 Option 3	GPIO[177] DCULITE_G6 — eMIOS0[21]	—	SIUL DCULite — PWM/Timer	I/O	M	None, None	—	—	P23

Table 30. DC electrical specifications at 2.5 V VDDE (continued)

Symbol		C	Parameter	Value		Unit	SpecID
				Min	Max		
Vih	SR	P	Input high voltage	Vref + 0.15	—	V	D9.85
Vil	SR	P	Input low voltage	—	Vref – 0.15	V	D9.86
Voh	SR	P	Output high voltage	Vtt + 0.81	—	V	D9.87
Vol	SR	P	Output low voltage	—	Vtt – 0.81	V	D9.88

Table 31. Output drive current @ VDDE = 2.5 V (±200mV)

Pad	C	Drive mode	Minimum Ioh (mA)	Minimum Iol (mA)	Libraries
pad_st_acc	P	011	–16.2	16.2	6MDDR
pad_st_dq	P	011	–16.2	16.2	6MDDR
pad_st_ck	P	011	–16.2	16.2	6MDDR

4.8.5 DC specification for CMOS090_ddr library @ VDDE = 1.8 V

Table 32. DC electrical specifications for 1.8 V VDDE

Symbol		C	Parameter	Value		Unit	SpecID
				Min	Max		
Vdd	SR	P	Core supply voltage	1.08	1.32	V	D9.89
				1.08	1.47		
Vdde	SR	P	I/O supply voltage	1.7	1.9	V	D9.90
Vdd33	SR	P	I/O pre-driver supply voltage	3.0	3.6	V	D9.91
Vref	SR	P	Input reference voltage	0.49 × Vdde	0.51 × Vdde	V	D9.92
Vtt	SR	P	Termination voltage	Vref – 0.04	Vref + 0.04	V	D9.93
Vih	SR	P	Input high voltage	Vref + 0.125	—	V	D9.94
Vil	SR	P	Input low voltage	—	Vref – 0.125	V	D9.95
Voh	SR	P	Output high voltage	Vtt + 0.81	—	V	D9.96
Vol	SR	P	Output low voltage	—	Vtt – 0.81	V	D9.97

Table 33. Output drive current @ VDDE = 1.8 V (±100mV)

Pad		Drive mode	Minimum Ioh (mA)	Minimum Iol (mA)	Libraries
pad_st_acc	P	000	–3.57	3.57	6MDDR
		001	–7.84	7.84	
		010	–5.36	5.36	
		110	–13.4	13.4	

Table 33. Output drive current @ VDDE = 1.8 V (±100mV) (continued)

Pad		Drive mode	Minimum Ioh (mA)	Minimum Iol (mA)	Libraries
pad_st_dq	P	000	–3.57	3.57	6MDDR
		001	–7.84	7.84	
		010	–5.36	5.36	
		110	–13.4	13.4	
pad_st_clk	P	000	–3.57	3.57	6MDDR
		001	–7.84	7.84	
		010	–5.36	5.36	
		110	–13.4	13.4	

Table 34. ODT DC electrical characteristics

Symbol		C	Parameter	Condition	Value			Unit	SpecID
					Min	Typ	Max		
Rtt	SR	C	Effective impedance value	PXD20 supports only 150 ohm termination and that can be enabled by enabling any bit of the termination control register (all of them are OR'ed).	120	150	180	Ω	D9.98

Table 35. core_v_det_odt and core_v_det33_odt specifications

VDDE	C	VDD	Vtrip max (V)	Vtrip min	Hysteresis min (V)
3.5	C	Rising	0.79	0.44	0.07
	C	Falling	0.56	0	
1.62	C	Rising	0.65	0.3	0.16
	C	Falling	0.33	0	
Rising	C	0.0	1.40	0.3	—

Table 36. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit	SpecID
					Min	Typ	Max		
V_{IH}	SR	P	Input High Level CMOS Schmitt Trigger	—	0.65 V_{DD}	—	V_{DD} + 0.4	V	D8.1
V_{IL}	SR	P	Input low Level CMOS Schmitt Trigger	—	–0.4	—	0.35 V_{DD}	V	D8.2
V_{HYS}	CC[3]	D	Input hysteresis CMOS Schmitt Trigger	—	0.1 V_{DD}	—	—	V	D8.3
V_{OL}	CC[4]	P	Output low level	Push Pull, I_{OL} = 2mA, V_{DD} = 5.0V ± 10%, ipp_hve = 0 (recommended)	—	—	0.1 V_{DD}	V	D8.4
		D		Push Pull, I_{OL} = 1mA, V_{DD} = 5.0V ± 10%, ipp_hve = 1[5]	—	—	0.1 V_{DD}		
		C		Push Pull, I_{OL} = 1mA, V_{DD} = 3.3V ± 10%, ipp_hve = 1 (recommended)	—	—	0.5		
T_{tr}	CC[4]	T	Output transition time output pin[6] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0V ± 10%, ipp_hve = 0	—	—	10	ns	D8.5
				C_L = 50pF, V_{DD} = 5.0V ± 10%, ipp_hve = 0	—	—	20		
				C_L = 100pF, V_{DD} = 5.0V ± 10%, ipp_hve = 0	—	—	40		
				C_L = 25pF, V_{DD} = 3.3V ± 10%, ipp_hve = 1	—	—	12		
				C_L = 50pF, V_{DD} = 3.3V ± 10%, ipp_hve = 1	—	—	25		
				C_L = 100pF, V_{DD} = 3.3V ± 10%, ipp_hve = 1	—	—	40		
W_{FRST}	SR	P	$\overline{\text{RESET}}$ Input Filtered Pulse	—	—	—	70	ns	D8.6
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ Input Not Filtered Pulse	—	400	—	—	ns	D8.7
$\lvert I_{WPU} \rvert$	CC[4]	P	Weak pullup current absolute value	—	10	—	—	µA	D8.8

1 V_{DD} = 3.3V ±10% / 5.0V ±10%, T_A = –40 to +105°C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Data based on characterization results, not tested in production

4 Guaranteed by design simulation.

5 This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of the reference manual).

6 C_L calculation should include device and package capacitance (C_{PKG} < 5pF).

4.16 ADC parameters

The device provides a 10-bit Successive Approximation Register (SAR) Analog to Digital Converter.

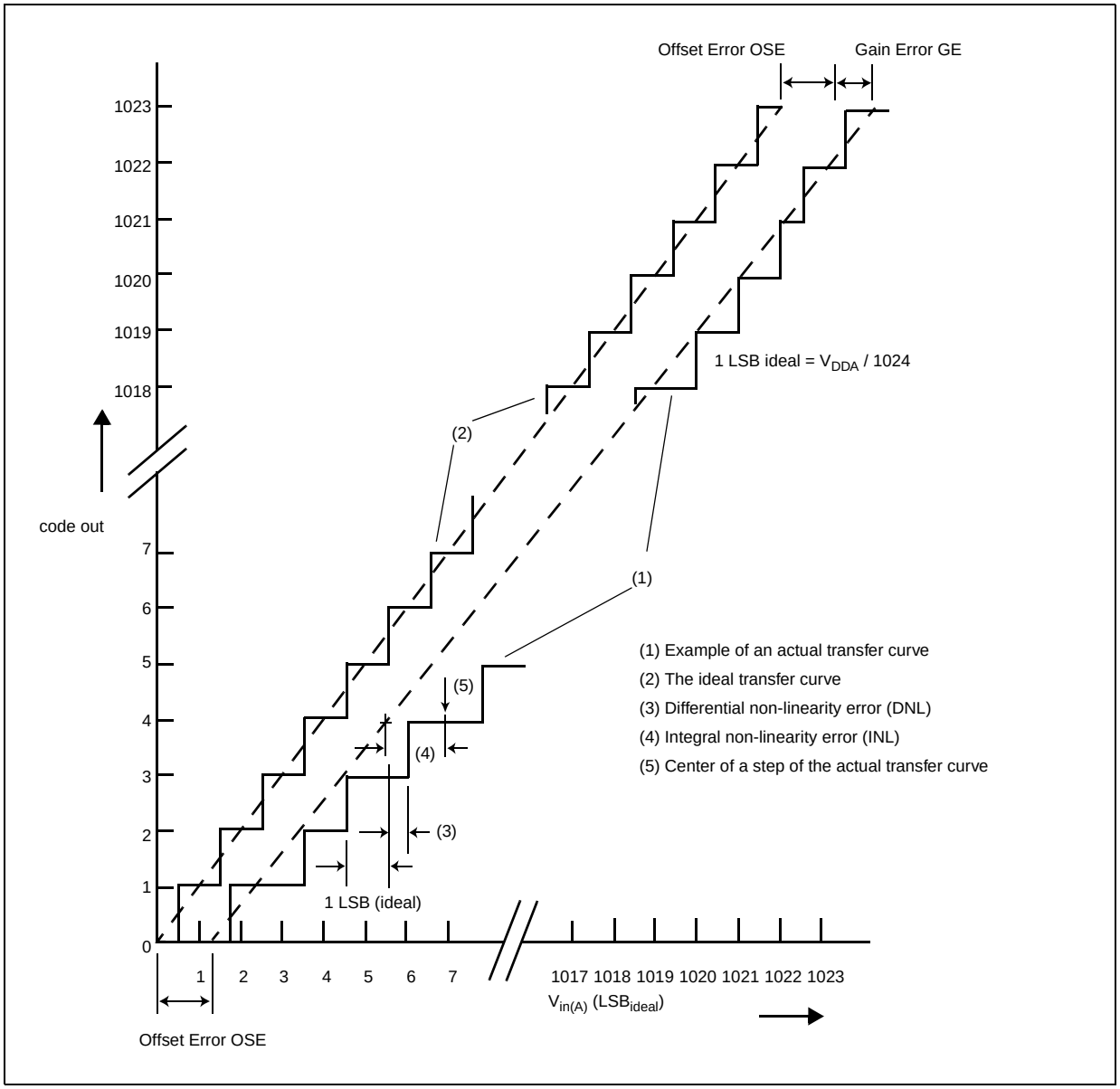

Figure 13. ADC characteristics and error definitions

4.16.1 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

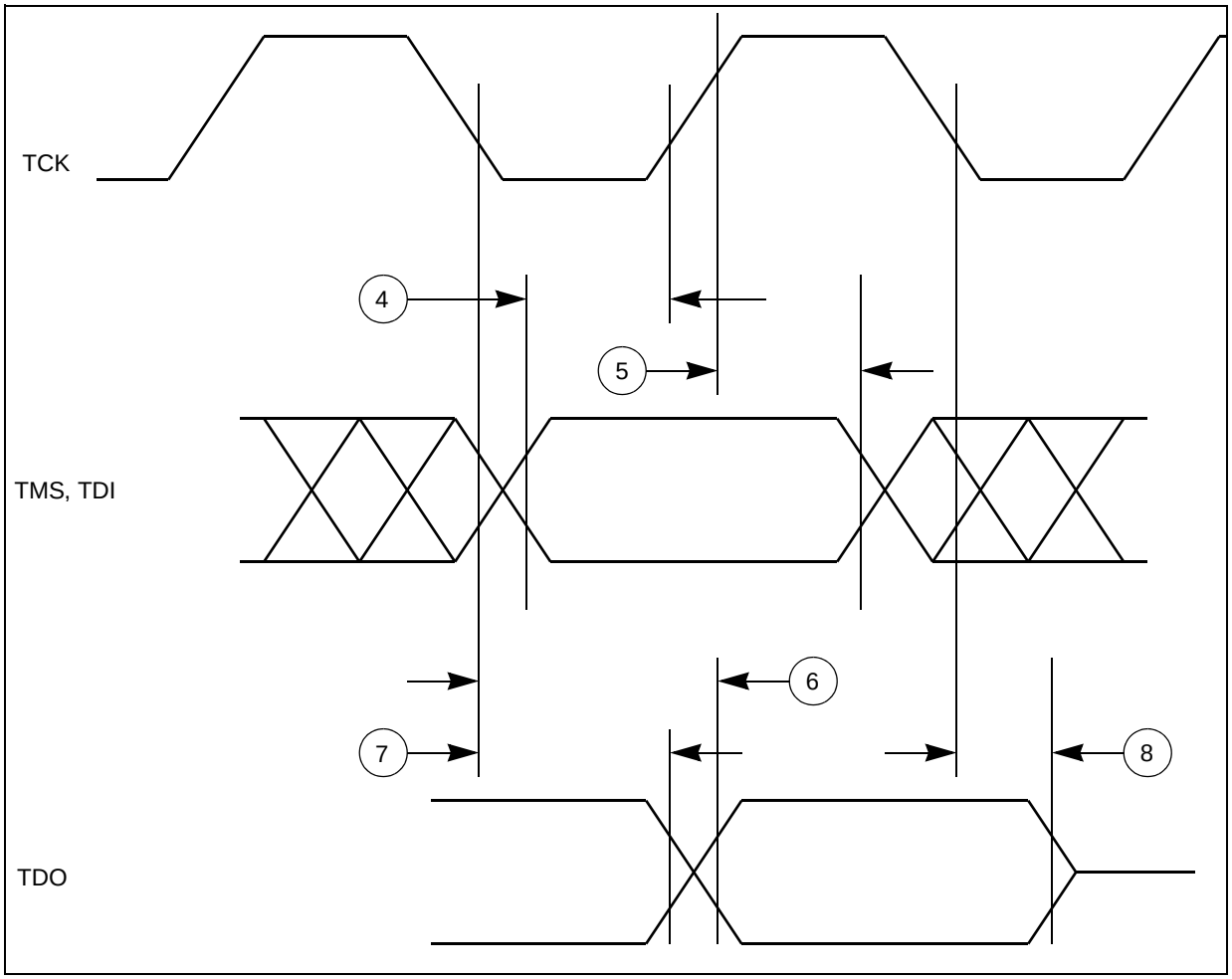

Figure 19. JTAG test access port timing

Table 66. DSPI timing[1] (continued)

Num	Symbol		C	Characteristic	Min	Max	Unit	SpecID
7	t_{SUI}	CC[2]	D	Data Setup Time for Inputs				A11.7
				Master (MTFE = 0)	20	—	ns	
				Slave	10	—	ns	
				Master (MTFE = 1, CPHA = 0)[8]	5	—	ns	
				Master (MTFE = 1, CPHA = 1)	35	—	ns	
8	t_{HI}	CC[2]	D	Data Hold Time for Inputs				A11.8
				Master (MTFE = 0)	–4	—	ns	
				Slave	10	—	ns	
				Master (MTFE = 1, CPHA = 0)[8]	26	—	ns	
				Master (MTFE = 1, CPHA = 1)	–4	—	ns	
9	t_{SUO}	CC[2]	D	Data Valid (after SCK edge)				A11.9
				Master (MTFE = 0)	—	15	ns	
				Slave	—	20	ns	
				Master (MTFE = 1, CPHA=0)	—	30	ns	
				Master (MTFE = 1, CPHA=1)	—	15	ns	
10	t_{HO}	CC[2]	D	Data Hold Time for Outputs				A11.10
				Master (MTFE = 0)	–15	—	ns	
				Slave	5.5	—	ns	
				Master (MTFE = 1, CPHA = 0)	0	—	ns	
				Master (MTFE = 1, CPHA = 1)	–15	—	ns	

1 DSPI timing specified at VDDE_x = 3.0 V to 3.6 V, T_A = –40 to 105 °C, and CL = 50 pF with SRC = 0b10.

2 Parameter values guaranteed by design.

3 The minimum SCK Cycle Time restricts the baud rate selection for given system clock rate.

4 The actual minimum SCK Cycle Time is limited by pad performance.

5 Maximum clock possible is System clock/2.

6 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK], program PSSCK=2 & CSSCK = 2

7 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC]

8 This delay value is corresponding to SMPL_PT=00b which is bit field 9 and 8 of DSPI_MCR register.

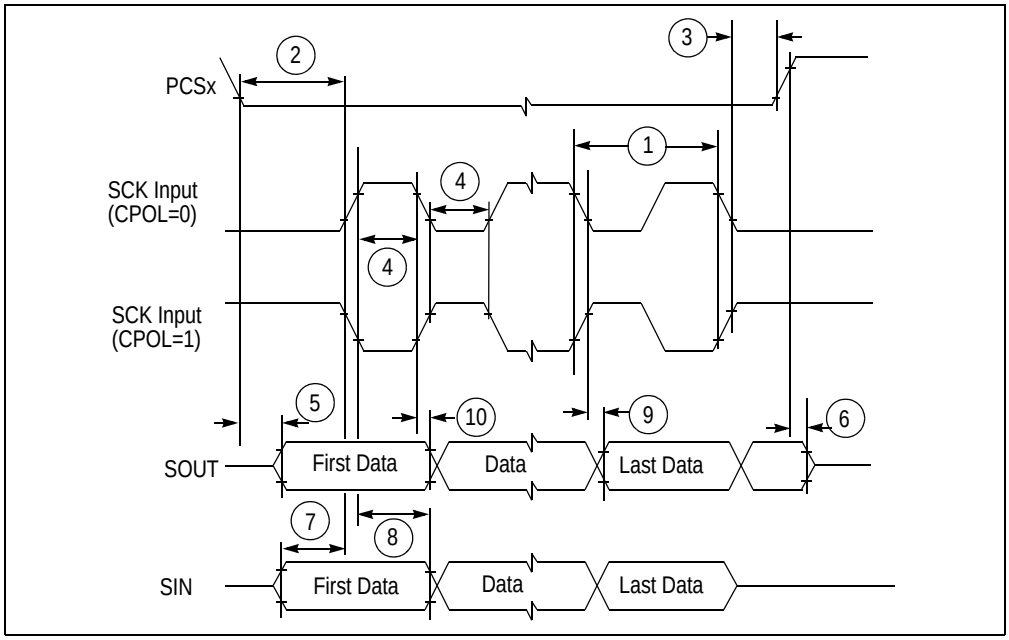

Figure 35. DSPI classic SPI timing — Slave, CPHA = 0

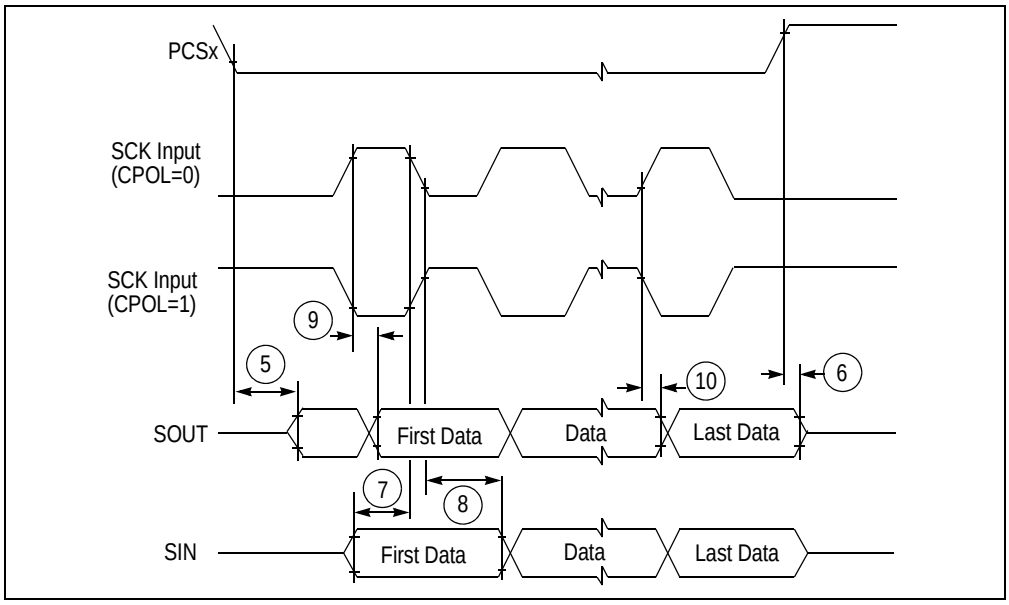

Figure 36. DSPI classic SPI timing — Slave, CPHA = 1

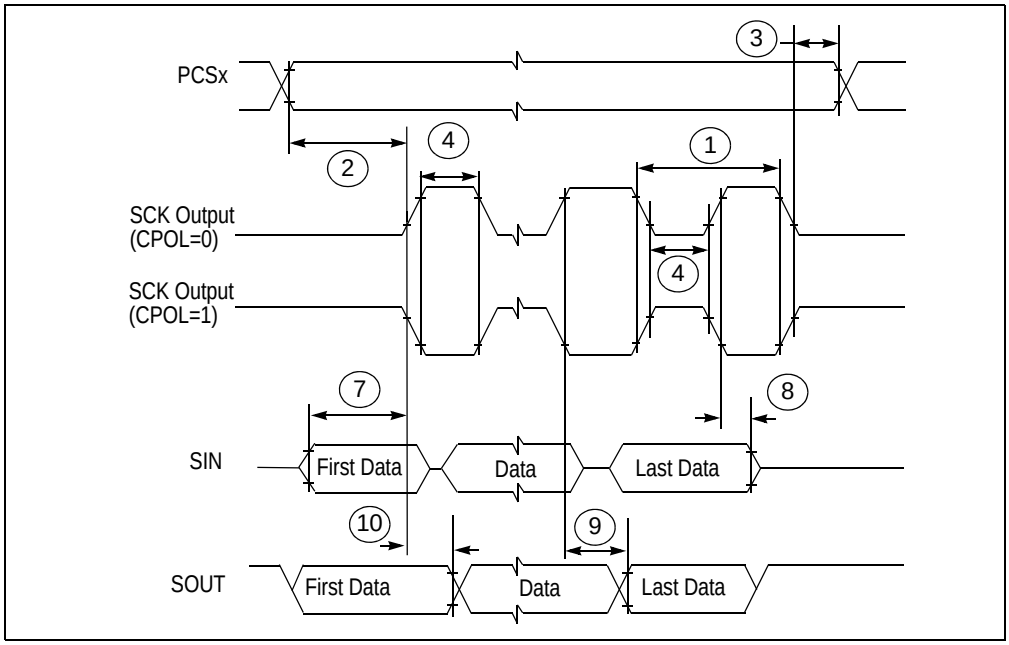

Figure 37. DSPI modified transfer format timing — Master, CPHA = 0

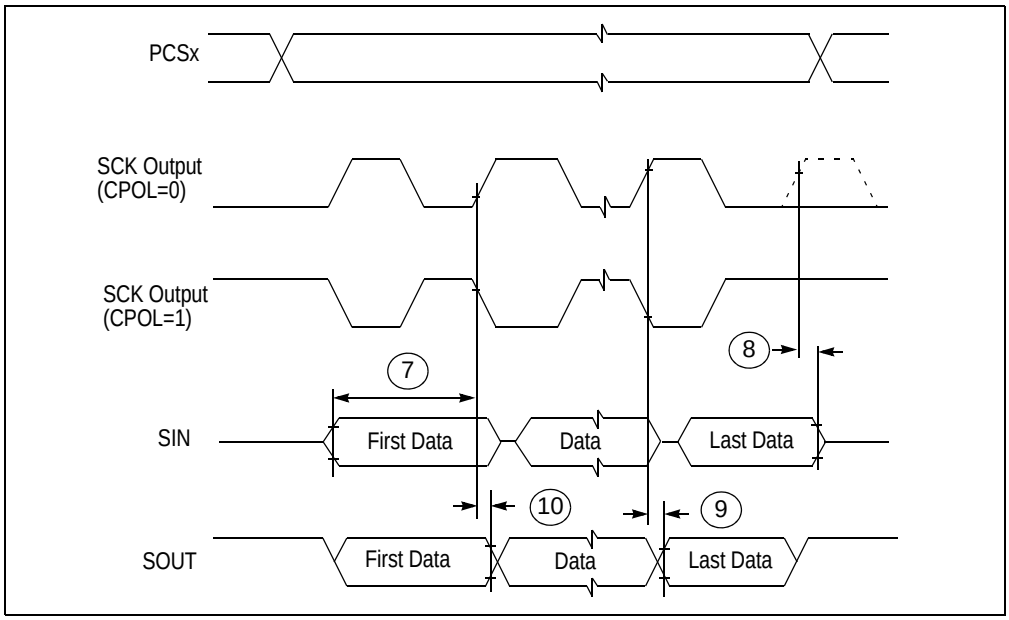

Figure 38. DSPI modified transfer format timing — Master, CPHA = 1

4.18.11 I²C timing

Table 67. I²C input timing specifications—SCL and SDA

Num	Symbol		C	Characteristic	Min. Value	Max. Value	Unit	SpecID
1	—	CC[1]	D	Start condition hold time	2	—	IP-Bus Cycle[2]	A12.1
2	—	CC[1]	D	Clock low time	8	—	IP-Bus Cycle[2]	A12.2
4	—	CC[1]	D	Data hold time	0.0	—	ns	A12.3
6	—	CC[1]	D	Clock high time	4	—	IP-Bus Cycle[2]	A12.4
7	—	CC[1]	D	Data setup time	0.0	—	ns	A12.5
8	—	CC[1]	D	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[2]	A12.6
9	—	CC[1]	D	Stop condition setup time	2	—	IP-Bus Cycle[2]	A12.7

1 Parameter values guaranteed by design.

2 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device

Table 68. I²C Output timing specifications—SCL and SDA

Num	Symbol		C	Characteristic	Min. Value	Max. Value	Unit	SpecID
1[1]	—	CC[2]	D	Start condition hold time	6	—	IP-Bus Cycle[3]	A12.8
2[1]	—	CC[2]	D	Clock low time	10	—	IP-Bus Cycle[2]	A12.9
3[4]	—	CC[2]	D	SCL/SDA rise time	—	99.6	ns	A12.10
4[1]	—	CC[2]	D	Data hold time	7	—	IP-Bus Cycle[2]	A12.11
5[1]	—	CC[2]	D	SCL/SDA fall time	—	99.5	ns	A12.12
6[1]	—	CC[2]	D	Clock high time	10	—	IP-Bus Cycle[2]	A12.13
7[1]	—	CC[2]	D	Data setup time	2	—	IP-Bus Cycle[2]	A12.14
8[1]	—	CC[2]	D	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[2]	A12.15
9[1]	—	CC[2]	D	Stop condition setup time	10	—	IP-Bus Cycle[2]	A12.16

1 Programming IBFD (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Parameter values guaranteed by design.

3 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device

4 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pullup resistor values.

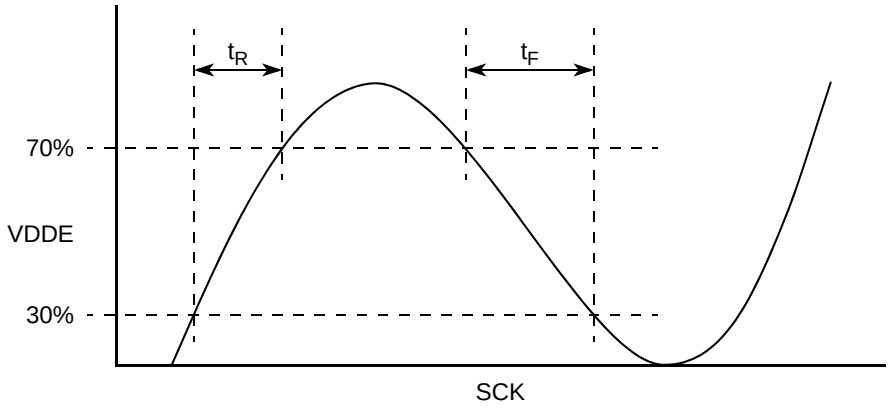

Figure 44. QuadSPI clock profile

4.18.13 TCON/RSDS timing

The following notes apply to Table 71:

- Measurement condition: Vdde/Vdd33 = 3.3 V ± 10%, Vdd = 1.2 V ± 10%, Vss/Vsse = 0 V, T = –40 to 105°C
- Termination: 100 Ω ± 5%
- VREFH_RSDS terminations of 47 µF

Table 71. TCON/RSDS timing

Symbol		C	Parameter	Condition	Value			Unit	SpecID
					Min	Typ	Max		
V_{OD}	CC	C	Differential output voltage	RSDS mode	391	—	471	mV	A14.1
V_{OS}	CC	C	Common mode voltage	100 Ω termination between Pad_p and Pad_n	1.17	—	1.4	V	A14.2
tr	CC	C	Rise time	Transition from 20% to 80%	606	—	844	ps	A14.3
tf	CC	C	Fall time	Transition from 20% to 80%	607	—	842	ps	A14.4
tplh	CC	D	Propagation delay, low to high	—	—	2.65	—	ns	A14.5
tphl	CC	D	Propagation delay, high to low	—	—	2.47	—	ns	A14.6
tdz	CC	D	Start-up time	—	—	200	—	µs	A14.7
tskew[1 2 3]	CC	C	Skew between different RSDS lines	Max and min skew between clock and data pads	—	—	—	ps	A14.8

1 There are eight programmable bits to provide 256 different skew numbers with various combinations of these bits.

2 Default value of all the eight skew options are all “1”.

3 All “0” combination of eight bits is not valid.