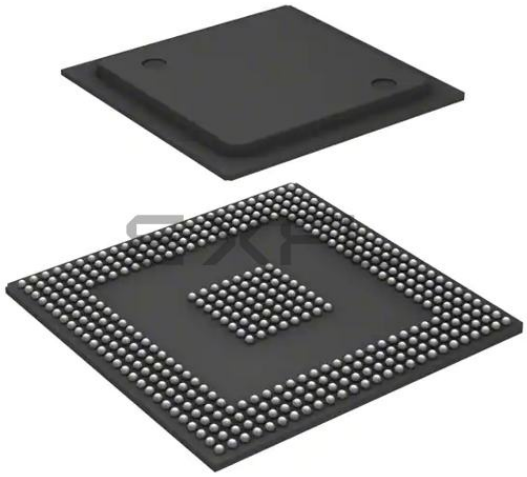

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	125MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	177
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpxd2020vvu125

1.3 Feature list

- Dual-issue, 32-bit Power Architecture Book E compliant CPU core complex (e200z4d)
  - Memory Management Unit (MMU)
  - 4 KB, 2/4-way instruction cache
- 2 MB on-chip ECC flash memory with:
  - Flash memory controller
  - Prefetch buffers
- 64 KB on-chip ECC SRAM
- 1 MB on-chip non-ECC graphics SRAM with two-port graphics SRAM controller
- Memory Protection Unit (MPU) with up to 16 region descriptors and 32-byte region granularity to provide basic memory access permission and ensure separation between different codes and data
- Interrupt Controller (INTC) with 181 peripheral interrupt sources and eight software interrupts
- Two Frequency-Modulated Phase-Locked Loops (FMPLLs)
  - Primary FMPLL (FMPLL0) provides a system clock up to 125 MHz
  - Auxiliary FMPLL (FMPLL1) is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules, QuadSPI and as alternate clock to the DCU and DCU-Lite for pixel clock generation
- Crossbar switch architecture enables concurrent access of peripherals, flash memory or RAM from multiple bus masters
- 16-channel Enhanced Direct Memory Access controller (eDMA) with multiple transfer request sources using a DMA channel multiplexer
- Boot Assist Module (BAM) with 8 KB dedicated ROM for embedded boot code supports boot options including download of boot code via a serial link (CAN or SCI)
- Two Display Control Units (DCU3 and DCULite) for direct drive of up to two TFT LCD displays up to XGA resolution
- Timing Controller (TCON) and RSDS interface for the DCU3 module
- 2D OpenVG 1.1 and raster graphics accelerator (GFX2D)
- Video Input Unit (VIU2) supporting 8/10-bit ITU656 video input, YUV to RGB conversion, video down-scaling, de-interlacing, contrast adjustment and brightness adjustment.
- DRAM controller supporting DDR1, DDR2, LPDDR1 and SDR DRAMs
- Stepper Motor Controller (SMC)
  - High-current drivers for as many as six stepper motors driven in full dual H-bridge configuration
  - Stepper motor return-to-zero and stall detection module
  - Stepper motor short circuit detection
- Sound Generator Module (SGM)
  - 4-channel mixer
  - Supports PCM wave playback and synthesized tones
  - Optional PWM or I^2S outputs
- Two 16-channel Enhanced Modular Input Output System (eMIOS) modules
  - Support a range of 16-bit Input Capture, Output Compare, Pulse Width Modulation and Quadrature Decode functions
- 10-bit Analog-to-Digital Converter (ADC) with a maximum conversion time of 1 µs
  - Up to 20 internal channels
  - Up to 8 external channels
- Three Deserial Serial Peripheral Interface (DSPI) modules for full-duplex, synchronous, communications with external devices
- QuadSPI serial flash memory controller
  - Supports single, dual and quad IO serial flash memory

— 208 LQFP, 0.5 mm pitch, 28 mm × 28 mm outline
— 416 TEPBGA, 1mm ball pitch, 27 mm × 27 mm outline

1.4 Feature details

1.4.1 Low-power operation

The PXD20 is designed for optimized low-power operation and dynamic power management of the CPU and peripherals. Power management features include software-controlled clock gating of peripherals and multiple power domains to minimize leakage in low-power modes.

There are three low-power modes:

- STANDBY
- STOP
- HALT

and five dynamic power modes — RUN[0..3] and DRUN. All low-power modes use clock gating to halt the clock for all or part of the device.

STANDBY mode turns off the power to the majority of the chip to offer the lowest power consumption mode.

The device can be awakened from STANDBY mode via from any of up to 23 I/O pins, a reset or from a periodic wake-up using a low power oscillator. If required, it is possible to enable the internal 16 MHz oscillator, the external 4–16 MHz oscillator and the external 32 KHz oscillator.

In STANDBY mode the contents of the CPU, on-chip peripheral registers and potentially some of the volatile memory are lost. The two possible configurations in STANDBY mode are:

- The device retains 64 KB of the on-chip SRAM, but the content of the graphics SRAM is lost.
- The device retains 8 KB of the on-chip SRAM, but the content of the graphics SRAM is lost.

STOP mode maintains power to the entire device allowing the retention of all on-chip registers and memory, and providing a faster recovery low power mode than the lowest-power STANDBY mode. There is no need to reconfigure the device before executing code. The clocks to the CPU and peripherals are halted and can be optionally stopped to the oscillator or PLL at the expense of a slower start-up time.

STOP is entered from RUN mode only. Wake-up from STOP mode is triggered by an external event or by the internal periodic wake-up, if enabled.

RUN modes are the main operating modes where the entire device can be powered and clocked and from which most processing activity is done. Four dynamic RUN modes are supported—RUN0 - RUN3. The ability to configure and select different RUN modes enables different clocks and power configurations to be supported with respect to each other and to allow switching between different operating conditions. The necessary peripherals, clock sources, clock speed and system clock prescalers can be independently configured for each of the four RUN modes of the device.

HALT mode is a reduced activity, low power mode intended for moderate periods of lower processing activity. In this mode the CPU system clocks are stopped but user-selected peripheral tasks can continue to run. It can be configured to provide more efficient power management features (switch-off PLL, flash memory, main regulator, etc.) at the cost of longer wake up latency. The system returns to RUN mode as soon as an event or interrupt is pending.

Table 2 summarizes the operating modes of the PXD20.

Table 2. Operating mode summary[1]

Operating mode	SoC features					Clock sources						Periodic Wake-up	Wake-up input	VREG mode	Wake-up time[2]						
	CPU GFX accelerator DRAM controller	Peripherals	Flash	RAM	Graphics RAM	Primary PLL	Auxiliary PLL	16 MHz IRC	4–16 MHz OSC	128 kHz IRC	32 KHz X OSC				VREG start-up	IRC Wake-up	Flash Recovery	OSC Stabilization	PLL Lock	S/W Reconfig	Mode switch over
RUN	On	OP	OP	OP[3]	On	OP	OP	On	OP	On	OP	—	—	FP	—	—	—	—	—	—	—
HALT	CG	OP	OP	OP[3]	On	OP	OP	On	OP	On	OP	OP	OP	FP	—	—	—	—	—	—	TBD
STOP	CG	CG	CG	OP[3]	On	CG	CG	OP	OP	On	OP	OP	OP	LP	350 µs	4 µs	20 µs	1 ms	200 µs	—	24 µs
STANDBY	Off	Off	Off	64 KB[4]	Off	Off	Off	OP	OP	OP	OP	OP	OP	LP	350 µs	8 µs	100 µs	1 ms	200 µs	Var	28 µs
	Off	Off	Off	8 KB[5]	Off	Off	Off	OP	OP	OP	OP	OP	OP	LP	200 µs	8 µs	100 µs	1 ms	200 µs	Var	28 µs
POR															500 µs	8 µs	100 µs	1 ms	200 µs		BAM[6]

1 Table Key:

On—Powered and clocked

OP—Optionally configurable to be enabled or disabled (clock gated)

CG—Clock Gated, Powered but clock stopped

Off-—Powered off and clock gated

FP—VREG Full Performance mode

LP—VREG Low Power mode, reduced output capability of VREG but lower power consumption

Var—Variable duration, based on the required reconfiguration and execution clock speed

BAM—Boot Assist Module Software and Hardware used for device start-up and configuration

2 A high level summary of some key durations that need to be considered when recovering from low power modes. This does not account for all durations at wake up. Other delays will be necessary to consider including, but not limited to the external supply start-up time.
IRC Wake-up time must not be added to the overall wake-up time as it starts in parallel with the VREG.
All other wake-up times must be added to determine the total start-up time.

3 Either 64 KB or 8 KB available.

4 64 KB of the RAM contents is retained, but not accessible in STANDBY mode.

5 8 KB of the RAM contents is retained, but not accessible in STANDBY mode.

6 Dependent on boot option after reset.

Additional notes on low power operation:

- Fast wake-up using the on-chip 16 MHz internal RC oscillator allows rapid execution from RAM on exit from low power modes
- The 16 MHz internal RC oscillator supports low speed code execution and clocking of peripherals when it is selected as the system clock and can also be used as the PLL input clock source to provide fast start-up without the external oscillator delay
- The device includes an internal voltage regulator that includes the following features:

- Direct readback of the pin value supported on all digital output pins through the SIU
- Configurable digital input filter that can be applied to up to 24 general purpose input pins for noise elimination on external interrupts
- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset.

1.4.8 On-chip flash memory with ECC

The PXD20 microcontroller has the following flash memory features:

- 2 MB of flash memory
  - Typical flash memory access time: 0 wait-state for buffer hits, 3 wait-states for page buffer miss at 125 MHz
  - Two 4 × 128-bit page buffers with programmable prefetch control
    - One set of page buffers can be allocated for code-only, fixed partitions of code and data, all available for any access
    - One set of page buffers allocated to Display Controller Units, Graphics Accelerator and the eDMA
  - 64-bit ECC with single-bit correction, double-bit detection for data integrity
- Small block flash arrangement to support features such as boot block, EEPROM Emulation, operating system block.
  - 8×16 KB
  - 2×64 KB
  - 2×128 KB
  - 6×256 KB
- Hardware managed Flash writes, erase and verify sequence
- Censorship protection scheme to prevent Flash content visibility

1.4.9 Static random-access memory (SRAM)

The PXD20 microcontroller has 64 KB general-purpose on-chip SRAM with the following features:

- Typical SRAM access time: 1 wait-state for reads and 32-bit writes
- 32-bit ECC with single-bit correction, double bit detection for data integrity
- Supports byte (8-bit), half word (16-bit), word (32-bit) and double-word (64-bit) writes for optimal use of memory
- User transparent ECC encoding and decoding for byte, half word, and word accesses
- Separate internal power domains applied to 56 KB and 8 KB SRAM blocks during STANDBY modes to retain contents during low power mode.

1.4.10 On-chip graphics SRAM

The PXD20 microcontroller has 1 MB on-chip graphics SRAM with the following features:

- Two crossbar slave ports:
  - One dedicated to the 2D Graphics Accelerator (GFX2D) access
  - One dedicated to all other crossbar masters
- Usable as general purpose SRAM
- Supports byte (8-bit), half word (16-bit), word (32-bit) and double-word (64-bit) writes for optimal use of memory
- RAM controller with hardware RAM fill function supporting all-zeroes or all-ones SRAM initialization
- Independent data buffers (one per AHB port) for maximum system performance
  - Optimized for burst transfers (read + write)
  - Programmable read prefetch capabilities

1.4.11 Memory Protection Unit (MPU)

The MPU features the following:

- Sixteen region descriptors for per master protection
- Start and end address defined with 32-byte granularity
- Overlapping regions supported
- Protection attributes can optionally include process ID
- Protection offered for 4 concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters

1.4.12 2D graphics accelerator (GFX2D)

- Native vector graphics rendering
  - Compatible with OpenVG1.1
  - Complete hardware OpenVG 1.1 rendering pipeline
  - Both geometry and pixel processing
  - Adaptive processing of Bezier curves and strokes
- 16-sample edge anti-aliasing
  - High image quality, font scalability, etc.
  - 4× Rotated Grid Supersampling (RGSS) AA for Flash
- 3D perspective texturing, reflections, and shadowing
- Shading (linear or radial gradient)
- Separate 2D engine for BitBlt, fill and ROP operations
- Significant performance improvement when compared to software or 3D GPU-based OpenVG implementations

1.4.13 Display Control Unit (DCU3)

The DCU3 is a display controller designed to drive TFT LCD displays up to WVGA resolution using direct blit graphics and video.

The DCU3 generates all the necessary signals required to drive the TFT LCD displays: up to 24-bit RGB data bus, Pixel Clock, Data Enable, Horizontal-Sync and Vertical-Sync.

The flexible architecture of the DCU3 enables the display of OpenVG-rendered frame buffer content and direct blit rendered graphics simultaneously.

An optional Timing Controller (TCON) and RSDS interface is available to directly drive the row and column drivers of a display panel.

Internal memory resource of the device allows to easily handle complex graphics contents (pictures, icons, languages, fonts).

The DCU3 supports 4-plane blending and 16 graphics layers. Control Descriptors (CDs) associated with each of the 16 layers enable effective merging of different resolutions into one plane to optimize use of internal memory buffers. A layer may be constructed from graphic content of various resolutions including indexed colors of 1, 2, 4 and 8 bpp, direct colors of 16, 24 and 32 bpp, and a YUV 4:2:2 color space. The ability of the DCU3 to handle input data in resolutions as low as 1bpp, 2bpp and 4bpp enables a highly efficient use of internal memory resources of the PXD20. A special tiled mode can be enabled on any of the 16 layers to repeat a pattern optimizing graphic memory usage.

A hardware cursor can be managed independently of the layers at blending level increasing the efficient use of the internal DCU3 resources.

1.4.28 Real time counter (RTC)

The Real Timer Counter supports wake-up from Low Power modes or Real Time Clock generation

- Configurable resolution for different timeout periods
  - 1 s resolution for >1 hour period
  - 1 ms resolution for 2 second period
- Selectable clock sources from external 32 KHz crystal, external 4–16 MHz crystal, internal 128 kHz RC oscillator or divided internal 16 MHz RC oscillator

1.4.29 System timer module (STM)

The STM is a 32-bit timer designed to support commonly required system and application software timing functions. The STM includes a 32-bit up counter and four 32-bit compare channels with a separate interrupt source for each channel. The counter is driven by the system clock divided by an 8-bit prescale value (1 to 256).

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.4.30 Software watchdog timer (SWT)

The SWT features the following:

- Watchdog supporting software activation or enabled out of Reset
- Supports normal or windowed mode
- Watchdog timer value writable once after reset
- Watchdog supports optional halting during low power modes
- Configurable response on timeout: reset, interrupt, or interrupt followed by reset
- Clock source: 128 kHz RC oscillator

1.4.31 Stepper motor controller (SMC)

The SMC module is a PWM motor controller suitable to drive instruments in a cluster configuration or any other loads requiring a PWM signal. The motor controller has twelve PWM channels associated with two pins each (24 pins in total) driving up to 6 stepper motors.

The SMC module includes the following features:

- 10/11-bit PWM counter
- 11-bit resolution with selectable PWM dithering function
- Left, right, or center aligned PWM
- Output slew rate control
- Output Short Circuit Detection

This module is suited for, but not limited to, driving small stepper and air core motors used in instrumentation applications. This module can be used for other motor control or PWM applications that match the frequency, resolution, and output drive capabilities of the module.

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PA[14]	PCR[14]	Option 0 Option 1 Option 2 Option 3	GPIO[14] DCU_G6 — —	RSDS7P	SIUL DCU3 — —	I/O	M / RSDS	None, none	134	158	F24
PA[15]	PCR[15]	Option 0 Option 1 Option 2 Option 3	GPIO[15] DCU_G7 — —	RSDS7M	SIUL DCU3 — —	I/O	M / RSDS	None, none	135	159	F23
PORT B											
PB[0]	PCR[16]	Option 0 Option 1 Option 2 Option 3	GPIO[16] CANTX_0 TXD_0 —	—	SIUL FlexCAN_0 LINFlex_0 —	I/O	S	None, none	13	13	W4
PB[1]	PCR[17]	Option 0 Option 1 Option 2 Option 3	GPIO[17] CANRX_0 RXD_0 —	—	SIUL FlexCAN_0 LINFlex_0 —	I/O	S	None, none	12	12	V1
PB[2]	PCR[18]	Option 0 Option 1 Option 2 Option 3	GPIO[18] TXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, none	153	183	D21
PB[3]	PCR[19]	Option 0 Option 1 Option 2 Option 3	GPIO[19] RXD_0 — —	—	SIUL LINFlex_0 — —	I/O	S	None, none	152	182	A22
PB[4]	PCR[20]	Option 0 Option 1 Option 2 Option 3	GPIO[20] SCK_1 MA0 —	—	SIUL DSPI_1 ADC —	I/O	S	None, none	62	74	AF15
PB[5]	PCR[21]	Option 0 Option 1 Option 2 Option 3	GPIO[21] SOUT_1 MA1 FABM	—	SIUL DSPI_1 ADC Control	I/O	S	Input, pull-down	63	75	AC16

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PG[4]	PCR[90]	Option 0 Option 1 Option 2 Option 3	GPIO[90] DCU_B4 — —	RSDS10P	SIUL DCU3 — —	I/O	M	None, None	143	168	C26
PG[5]	PCR[91]	Option 0 Option 1 Option 2 Option 3	GPIO[91] DCU_B5 — —	RSDS10M	SIUL DCU3 — —	I/O	M	None, None	144	169	B26
PG[6]	PCR[92]	Option 0 Option 1 Option 2 Option 3	GPIO[92] DCU_B6 — —	RSDS11P	SIUL DCU3 — —	I/O	M	None, None	145	170	A26
PG[7]	PCR[93]	Option 0 Option 1 Option 2 Option 3	GPIO[93] DCU_B7 — —	RSDS11M	SIUL DCU3 — —	I/O	M	None, None	146	171	A25
PG[8]	PCR[94]	Option 0 Option 1 Option 2 Option 3	GPIO[94] DCU_VSYNC — —	—	SIUL DCU3 — —	I/O	M	None, None	1	1	T4
PG[9]	PCR[95]	Option 0 Option 1 Option 2 Option 3	GPIO[95] DCU_HSYNC — —	—	SIUL DCU3 — —	I/O	M	None, None	2	2	T2
PG[10]	PCR[96]	Option 0 Option 1 Option 2 Option 3	GPIO[96] DCU_DE — —	—	SIUL DCU3 — —	I/O	M	None, None	3	3	T1
PG[11]	PCR[97]	Option 0 Option 1 Option 2 Option 3	GPIO[97] DCU_PCLK — —	RSDSCLKP	SIUL DCU3 — —	I/O	F	None, None	147	172	E23
PG[12]	PCR[98]	Option 0 Option 1 Option 2 Option 3	GPIO[98] CS0_1 PDI_DE DCULITE_B7	—	SIUL DSPI_1 PDI DCULite	I/O	M	None, None	168	200	A15

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PG[13]	—	—	Reserved	—	—	—	—	—	—	—	—
PG[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PG[15]	—	—	Reserved	—	—	—	—	—	—	—	—
PORT H											
PH[0][6]	PCR[99]	Option 0 Option 1 Option 2 Option 3	GPIO[99] TCK — —	—	SIUL JTAG — —	I/O	S	Input, Pull Up	41	49	AC6
PH[1][6]	PCR[100]	Option 0 Option 1 Option 2 Option 3	GPIO[100] TDI — —	—	SIUL JTAG — —	I/O	S	Input, Pull Up	42	50	AD6
PH[2][6]	PCR[101]	Option 0 Option 1 Option 2 Option 3	GPIO[101] TDO — —	—	SIUL JTAG — —	I/O	M	Output, None	43	51	AE6
PH[3][6]	PCR[102]	Option 0 Option 1 Option 2 Option 3	GPIO[102] TMS — —	—	SIUL JTAG — —	I/O	S	Input, Pull Up	44	52	AF6
PH[4]	PCR[103]	Option 0 Option 1 Option 2 Option 3	GPIO[103] CS0_0 eMIOS1[21] DCULITE_G6	—	SIUL DSPI_0 PWM/Timer DCULite	I/O	M	None, None	61	73	AE15
PH[5]	PCR[104]	Option 0 Option 1 Option 2 Option 3	GPIO[104] VIU7_PDI15 I2S_FS eMIOS1[8]	—	SIUL VIU2/PDI SGM PWM/Timer	I/O	S	None, None	38	—	—
PH[6]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[7]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[8]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[9]	—	—	Reserved	—	—	—	—	—	—	—	—
PH[10]	—	—	Reserved	—	—	—	—	—	—	—	—

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PM[6]	PCR[153]	Option 0 Option 1 Option 2 Option 3	GPIO[153] VIU6_PDI14 eMIOS1[23] DCULITE_TAG	—	SIUL VIU2/PDI PWM/Timer DCULite	I/O	M	None, None	17	—	—
PM[7]	PCR[154]	Option 0 Option 1 Option 2 Option 3	GPIO[154] VIU8_PDI16 I2S_DO / PWMO eMIOS1[16]	—	SIUL VIU2/PDI SGM PWM/Timer	I/O	S	None, None	39	—	—
PM[8]	PCR[155]	Option 0 Option 1 Option 2 Option 3	GPIO[155] VIU9_PDI17 I2S_SCK / PWMOA eMIOS1[23]	—	SIUL VIU2/PDI SGM PWM/Timer	I/O	S	None, None	40	—	—
PM[9]	PCR[156]	Option 0 Option 1 Option 2 Option 3	GPIO[156] PDI_PCLK SGM_MCLK eMIOS0[8]	—	SIUL PDI SGM PWM/Timer	I/O	M	None, None	113	—	—
PM[10]	PCR[157]	Option 0 Option 1 Option 2 Option 3	GPIO[157] RXD_2 CANRX_2 eMIOS0[16]	—	SIUL LINFlex_2 FlexCAN_2 PWM/Timer	I/O	S	None, None	114	—	—
PM[11]	PCR[158]	Option 0 Option 1 Option 2 Option 3	GPIO[158] TXD_2 CANTX_2 eMIOS0[23]	—	SIUL LINFlex_2 FlexCAN_2 PWM/Timer	I/O	S	None, None	115	—	—
PM[12]	PCR[159]	Option 0 Option 1 Option 2 Option 3	GPIO[159] DCULITE_B7 — I2S_SCK / PWMOA	—	SIUL DCULite — SGM	I/O	M	None, None	—	—	L24
PM[13]	PCR[160]	Option 0 Option 1 Option 2 Option 3	GPIO[160] DCULITE_PCLK — SGM_MCLK	—	SIUL DCULite — SGM	I/O	F	None, None	—	—	L23
PM[14]	—	—	Reserved	—	—	—	—	—	—	—	—
PM[15]	—	—	Reserved	—	—	—	—	—	—	—	—

Table 7. Port pin summary (continued)

Port pin	PCR	Alternate function[1]	Function	Special function[2]	Peripheral[3]	I/O direction	Pad Type[4]	RESET config[5]	Pin number		
									176 LQFP	208 LQFP	416 TEPBGA
PN[8]	PCR[169]	Option 0 Option 1 Option 2 Option 3	GPIO[169] DCULITE_R6 — TCON[10]	—	SIUL DCULite — TCON	I/O	M	None, None	—	—	AC12
PN[9]	PCR[170]	Option 0 Option 1 Option 2 Option 3	GPIO[170] DCULITE_R7 — TCON[11]	—	SIUL DCULite — TCON	I/O	M	None, None	—	—	AD12
PN[10]	PCR[171]	Option 0 Option 1 Option 2 Option 3	GPIO[171] DCULITE_G0 RXD_3 VIU2_PDI10	—	SIUL DCULite LINFlex_3 VIU2/PDI	I/O	M	None, None	—	—	AE12
PN[11]	PCR[172]	Option 0 Option 1 Option 2 Option 3	GPIO[172] DCULITE_G1 TXD_3 VIU3_PDI11	—	SIUL DCULite LINFlex_3 VIU2/PDI	I/O	M	None, None	—	—	AF12
PN[12]	PCR[173]	Option 0 Option 1 Option 2 Option 3	GPIO[173] DCULITE_G2 — eMIOS0[17]	—	SIUL DCULite — PWM/Timer	I/O	M	None, None	—	—	R26
PN[13]	PCR[174]	Option 0 Option 1 Option 2 Option 3	GPIO[174] DCULITE_G3 — eMIOS0[18]	—	SIUL DCULite — PWM/Timer	I/O	M	None, None	—	—	R25
PN[14]	PCR[175]	Option 0 Option 1 Option 2 Option 3	GPIO[175] DCULITE_G4 — eMIOS0[19]	—	SIUL DCULite — PWM/Timer	I/O	M	None, None	—	—	P26
PN[15]	PCR[176]	Option 0 Option 1 Option 2 Option 3	GPIO[176] DCULITE_G5 — eMIOS0[20]	—	SIUL DCULite — PWM/Timer	I/O	M	None, None	—	—	P24
PORT P											
PP[0]	PCR[177]	Option 0 Option 1 Option 2 Option 3	GPIO[177] DCULITE_G6 — eMIOS0[21]	—	SIUL DCULite — PWM/Timer	I/O	M	None, None	—	—	P23

3 System design information

3.1 Power-up sequencing

The preferred power-up sequence for PXD20 is as follows:

1. Generic IO supplies or noise-free supplies, consisting of:
   - VDDA
   - VDDE_A
   - VDDE_B
   - VDDM
   - VDD_DR
   - VDD33_DR
   - VDDPLL

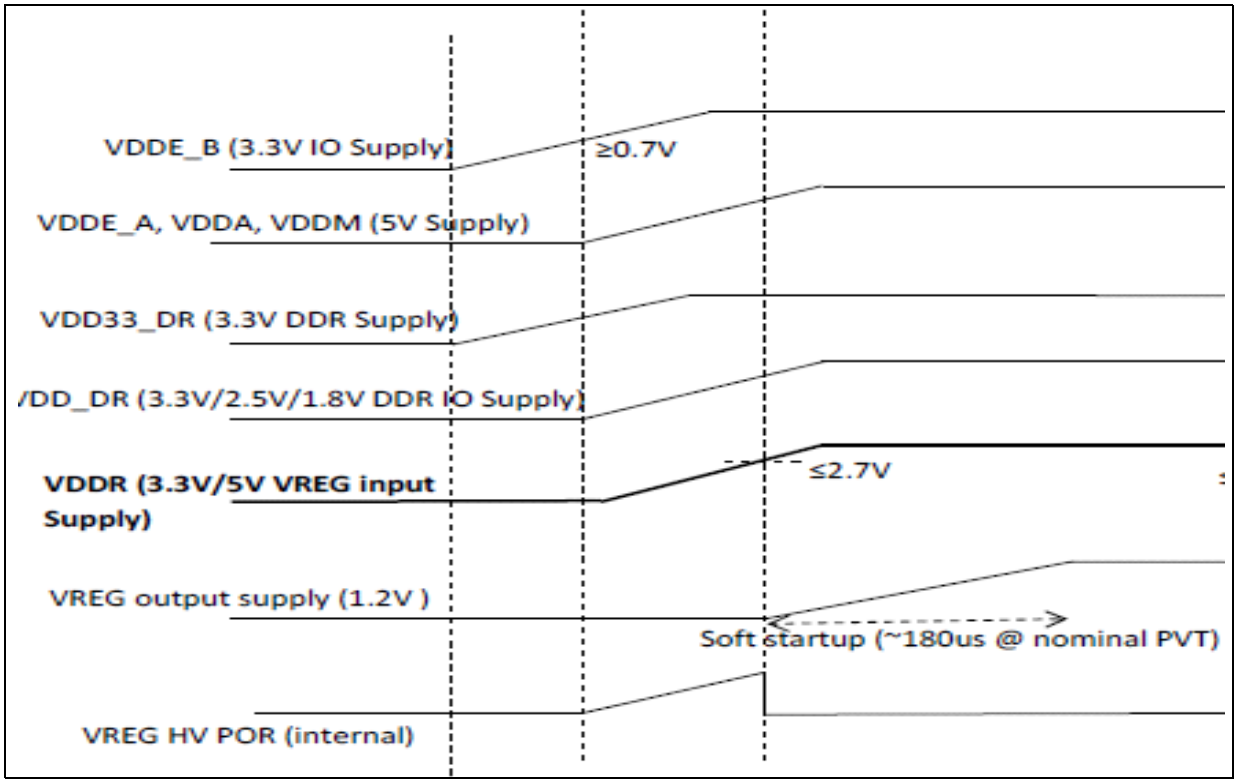

Figure 6. Power-up sequencing

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

4.4 Recommended operating conditions

Table 10. Recommended operating conditions (3.3 V)

Symbol		C	Parameter	Conditions	Value		Unit	SpecID
					Min	Max		
V_{DDA}[1]	SR	P	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})		+3.0	+3.6	V	D2.1
		D		Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1		
V_{SSA}	SR	P	Voltage on VSSA (ADC reference) pin with respect V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V	D2.2
V_{DDPLL}	CC	P	Voltage on VDDPLL (1.2 V PLL supply) pin with respect to ground (V_{SSPLL})		1.08	1.32	V	D2.3
V_{DDR}[2]	SR	P	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})		+3.0	+3.6	V	D2.4
		D		Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1		
V_{SSR}	SR	D	Voltage on VSSR (regulator ground) pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V	D2.5
V_{DD12}[3,4]	CC	P	Voltage on VDD12 pin with respect to ground (V_{SS12})		1.08	1.4	V	D2.6
V_{SS12}	CC	D	Voltage on VSS12 pin with respect to V_{SS}		V_{SS} – 0.1	V_{SS} + 0.1	V	D2.7
V_{DD}[5,6,7]	SR	P	Voltage on V_{DD} pins (V_{DDE_A}, V_{DDE_B}, V_{DD_DR}, V_{DDM}) with respect to ground (V_{SS})		V_{DDmin}[5]	V_{DDmax}[5]	V	D2.8
V_{SS}[8]	SR	D	I/O supply ground		0	0	V	D2.9
V_{DDE_A}[9]	SR	P	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})		+3.0	+3.6	V	D2.10
V_{DDE_B}	SR	P	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})		+3.0	+3.6	V	D2.11
V_{DDM}	SR	P	Voltage on VDDM (stepper motor supply) pin with respect to ground (V_{SSM})		+3.0	+3.6	V	D2.12
V_{DD_DR}		P	Voltage on V_{DDDDR} with respect to V_{SS}		+1.62	+3.6	V	D2.13
V_{SS_DR}		D	Voltage on V_{SSRSDS} with respect to V_{SS}		+1.62	+3.6	V	D2.14
V_{RSDS}		P	Voltage on V_{DDDDR} with respect to V_{SS}		+3.0	+3.6	V	D2.15
TV_{DD}	SR	D	V_{DD} slope to ensure correct power up[10]			12	V/ms	D2.16
T_A	SR	P	Ambient temperature under bias		–40	105	°C	D2.17
T_J	SR	D	Junction temperature under bias		–40	140		D2.18

[1] Time after the input supply to the voltage regulator has ramped up (VDDR) and the voltage regulator has asserted the Power OK signal.

Table 17. Low-power voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions	Min	Max	Unit	SpecID
T_J	SR	D	Junction temperature	—	–40	140	°C	D5.2
I_{REG}	CC	T	Current consumption	Reference included, @ 55 °C No load @ Full load	—	 5 600	µA	D5.3
I_L	CC	T	Output current capacity	DC load current	—	15	mA	D5.4
V_{DD12}	CC	D	Output voltage	Pre-trimming sigma < 7 mV	—	1.33	V	D5.5
		P		Post-trimming	1.14	1.32		

Table 18. Ultra low-power voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions	Min	Max	Unit	SpecID
T_J	SR	D	Junction temperature	—	–40	140	°C	D5.2
I_{REG}	CC	T	Current consumption	Reference included, @ 55 °C No load @ Full load	—	 2 100	µA	D5.3
I_L	CC	T	Output current capacity	DC load current	—	5	mA	D5.4
V_{DD12}	CC	D	Output voltage (value @ I_L = 0 @ 27°C)	Pre-trimming sigma < 7 mV	—	1.33	V	D5.5
		P		Post-trimming	1.14	1.32		

4.7.2 Voltage monitor electrical characteristics

The device implements a Power On Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the V_{DD} and the V_{DD12} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0V ±10% range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

Table 24. DC electrical specifications (continued)

Symbol		C	Parameter	Condition	Value		Unit	SpecID
					Min	Max		
Rtgate	SR	D	Pad_tgate_hv input resistance	—	250	800	Ω	D9.39
pupd_rm	SR	D	pad_pupd_hv resistance mismatch	—	—	5	%	D9.40
pupd_leak	SR	D	pad_pupd_hv leakage current	—	0.1	75000	pA	D9.41
pupd200k	SR	D	pad_pupd_hv 200 kΩ resistance	—	130	280	kΩ	D9.42
pupd100k	SR	D	pad_pupd_hv 100 kΩ resistance	—	65	140	kΩ	D9.43
pupd5k	SR	D	pad_pupd_hv 5 kΩ resistance	—	1.4	5.2	kΩ	D9.44

Table 25. DC electrical specifications

Symbol		Parameter	Condition	Value		Unit	SpecID
				Min	Max		
Vdd	SR	Core supply voltage	—	1.08	1.32	V	D9.45
Vdde	SR	I/O supply voltage	—	3.0	3.6	V	D9.46
Vdd33	SR	I/O pre-driver supply voltage	—	3.0	3.6	V	D9.47
Vih_hys	SR	CMOS input buffer high voltage	With hysteresis enabled	0.65 × Vdde	Vdde + 0.3	V	D9.48
Vil_hys	SR	CMOS input buffer low voltage	With hysteresis enabled	Vss – 0.3	0.35 × Vdde	V	D9.49
Vih	SR	CMOS input buffer high voltage	With hysteresis disabled	0.55 × Vdde	Vdde + 0.3	V	D9.50
Vil	SR	CMOS input buffer low voltage	With hysteresis disabled	Vss – 0.3	0.40 × Vdde	V	D9.51
Vhys	SR	CMOS input buffer hysteresis	—	0.1 × Vdde	—	V	D9.52
Pull_Ioh	SR	Weak pullup current	—	15	70	µA	D9.53
Pull_Iol	SR	Weak pulldown current	—	15	95	µA	D9.54
Iinact_d	SR	Digital pad input leakage current	Weak pull inactive	–2.5	2.5	µA	D9.55
Iinact_a	SR	Analog pad input leakage current	Weak pull inactive	–150	150	µA	D9.56
Voh	SR	Slew rate controlled output high voltage	—	0.8 × Vdde	—	V	D9.57
Vol	SR	Slew rate controlled output low voltage	—	—	0.2 × Vdde	V	D9.58

Table 30. DC electrical specifications at 2.5 V VDDE (continued)

Symbol		C	Parameter	Value		Unit	SpecID
				Min	Max		
Vih	SR	P	Input high voltage	Vref + 0.15	—	V	D9.85
Vil	SR	P	Input low voltage	—	Vref – 0.15	V	D9.86
Voh	SR	P	Output high voltage	Vtt + 0.81	—	V	D9.87
Vol	SR	P	Output low voltage	—	Vtt – 0.81	V	D9.88

Table 31. Output drive current @ VDDE = 2.5 V (±200mV)

Pad	C	Drive mode	Minimum Ioh (mA)	Minimum Iol (mA)	Libraries
pad_st_acc	P	011	–16.2	16.2	6MDDR
pad_st_dq	P	011	–16.2	16.2	6MDDR
pad_st_ck	P	011	–16.2	16.2	6MDDR

4.8.5 DC specification for CMOS090_ddr library @ VDDE = 1.8 V

Table 32. DC electrical specifications for 1.8 V VDDE

Symbol		C	Parameter	Value		Unit	SpecID
				Min	Max		
Vdd	SR	P	Core supply voltage	1.08	1.32	V	D9.89
				1.08	1.47		
Vdde	SR	P	I/O supply voltage	1.7	1.9	V	D9.90
Vdd33	SR	P	I/O pre-driver supply voltage	3.0	3.6	V	D9.91
Vref	SR	P	Input reference voltage	0.49 × Vdde	0.51 × Vdde	V	D9.92
Vtt	SR	P	Termination voltage	Vref – 0.04	Vref + 0.04	V	D9.93
Vih	SR	P	Input high voltage	Vref + 0.125	—	V	D9.94
Vil	SR	P	Input low voltage	—	Vref – 0.125	V	D9.95
Voh	SR	P	Output high voltage	Vtt + 0.81	—	V	D9.96
Vol	SR	P	Output low voltage	—	Vtt – 0.81	V	D9.97

Table 33. Output drive current @ VDDE = 1.8 V (±100mV)

Pad		Drive mode	Minimum Ioh (mA)	Minimum Iol (mA)	Libraries
pad_st_acc	P	000	–3.57	3.57	6MDDR
		001	–7.84	7.84	
		010	–5.36	5.36	
		110	–13.4	13.4	

Table 33. Output drive current @ VDDE = 1.8 V (±100mV) (continued)

Pad		Drive mode	Minimum Ioh (mA)	Minimum Iol (mA)	Libraries
pad_st_dq	P	000	–3.57	3.57	6MDDR
		001	–7.84	7.84	
		010	–5.36	5.36	
		110	–13.4	13.4	
pad_st_clk	P	000	–3.57	3.57	6MDDR
		001	–7.84	7.84	
		010	–5.36	5.36	
		110	–13.4	13.4	

Table 34. ODT DC electrical characteristics

Symbol		C	Parameter	Condition	Value			Unit	SpecID
					Min	Typ	Max		
Rtt	SR	C	Effective impedance value	PXD20 supports only 150 ohm termination and that can be enabled by enabling any bit of the termination control register (all of them are OR'ed).	120	150	180	Ω	D9.98

Table 35. core_v_det_odt and core_v_det33_odt specifications

VDDE	C	VDD	Vtrip max (V)	Vtrip min	Hysteresis min (V)
3.5	C	Rising	0.79	0.44	0.07
	C	Falling	0.56	0	
1.62	C	Rising	0.65	0.3	0.16
	C	Falling	0.33	0	
Rising	C	0.0	1.40	0.3	—

4.11 Slow external crystal oscillator (32 KHz) electrical characteristics

The device provides a slow external oscillator/resonator driver (SXOSC). The 32 KHz oscillator operates at 32,768 Hz.

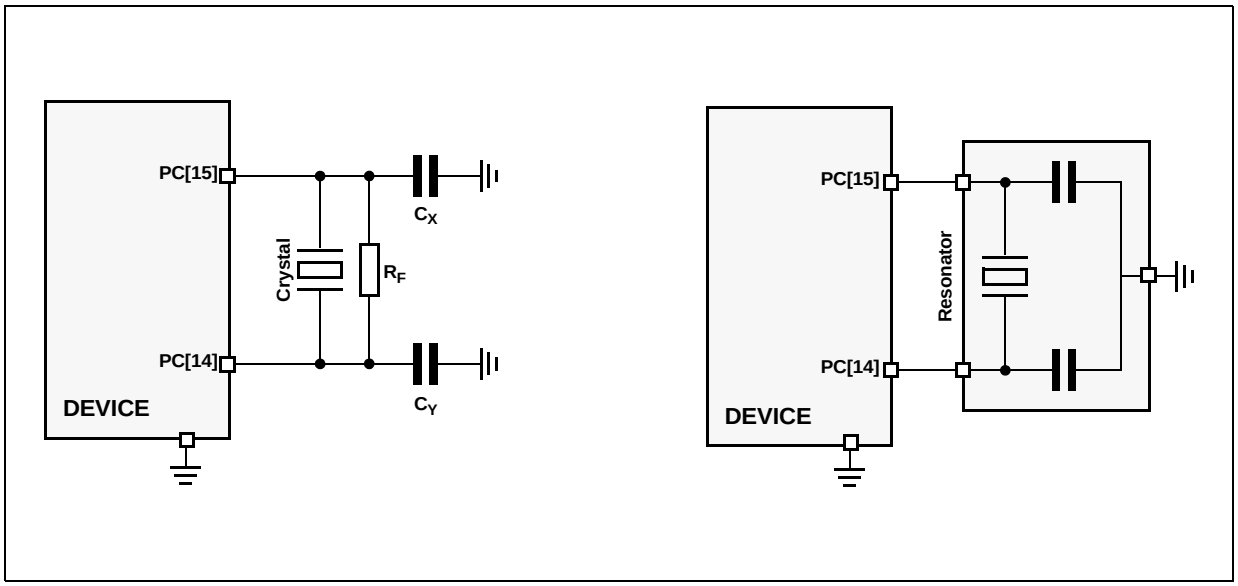

Figure 11. Crystal oscillator and resonator connection scheme

NOTE

PC[14]/PC[15] must not be directly used to drive external circuits.

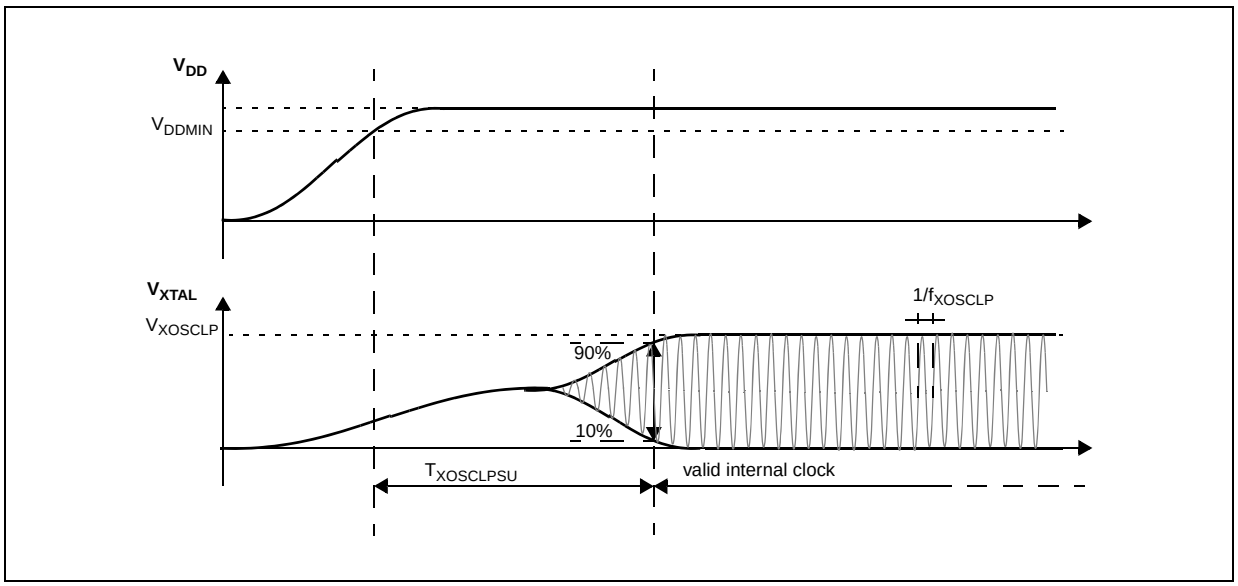

Figure 12. Slow external crystal oscillator electrical characteristics

Table 47. Functional pad AC type specifications (continued)

Name	Prop. delay (ns) L>H / H>L		Rise/fall edge (ns)		Drive load (pF)	Drive/slew rate select
	Min	Max	Min	Max		MSB, LSB
pad_ssr_hv	9.2 / 6.9	27 / 28	5.5 / 4.1	15 / 17	50	11
	30 / 23	81 / 87	21 / 16	57 / 63	200	
	N/A					10
	31 / 31	80 / 90	15.4 / 15.4	38 / 42	50	01
	58 / 52	144 / 155	32 / 26	82 / 85	200	
	162 / 168	415 / 415	80 / 82	190 / 190	50	00
	216 / 205	533 / 540	106 / 95	250 / 250	200	
pad_i_hv	0.5 / 0.5	3 / 3	0.4 / 0.4	1.5 / 1.5	0.5	N/A

4.17.4 Pad AC specifications (3.3 V, PAD3V5V = 1)

Table 48. Pad AC specifications (3.3 V, PAD3V5V = 1)[1]

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	3	—	40	4	—	40	—	—	4	0.01	—	2	25
		3	—	40	6	—	50	—	—	2	0.01	—	2	50
		3	—	40	10	—	75	—	—	2	0.01	—	2	100
		3	—	40	14	—	100	—	—	2	0.01	—	2	200
2	Medium	1	—	15	2	—	12	—	—	40	2.5	—	7	25
		1	—	15	4	—	25	—	—	20	2.5	—	7	50
		1	—	15	8	—	40	—	—	13	2.5	—	7	100
		1	—	15	14	—	70	—	—	7	2.5	—	7	200
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	3	—	40	50
		1	—	6	3	—	12	—	—	40	3	—	40	100
		1	—	6	5	—	18	—	—	25	3	—	40	200
4	Pull Up/Down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50
Parameter Classification		D			C			C			C			n/a

1 Propagation delay from $V_{DD}/2$ of internal signal to Pchannel/Nchannel on condition

2 Slope at rising/falling edge

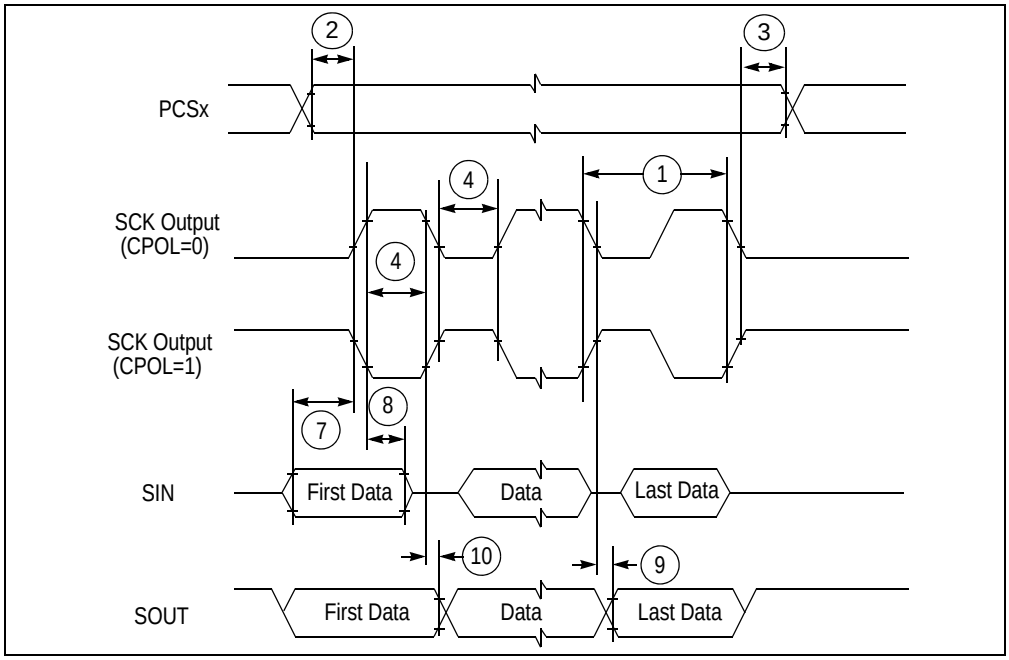

Figure 33. DSPI classic SPI timing — Master, CPHA = 0

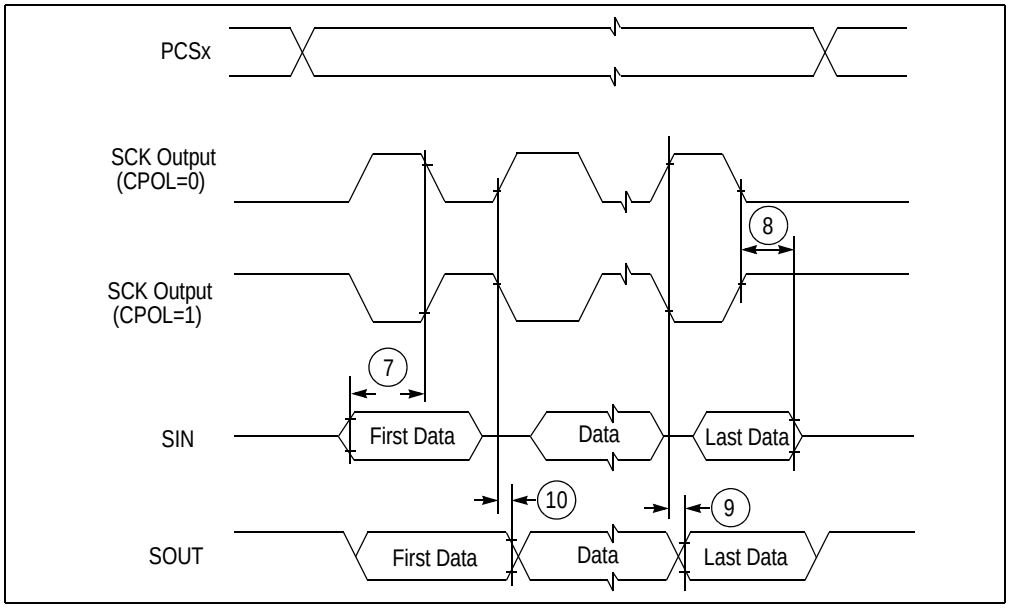

Figure 34. DSPI classic SPI timing — Master, CPHA = 1