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What is "Embedded - Microcontrollers"?

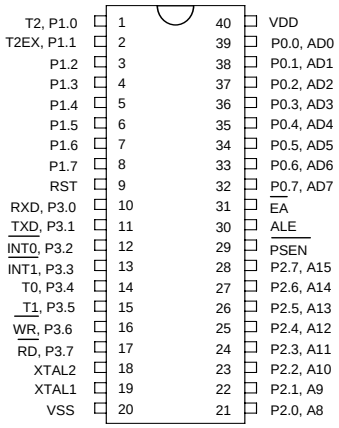
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

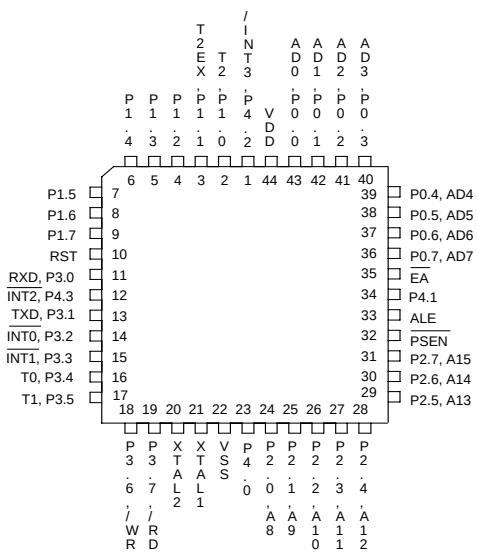
Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 60°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78l058a24fl

3. PIN CONFIGURATIONS

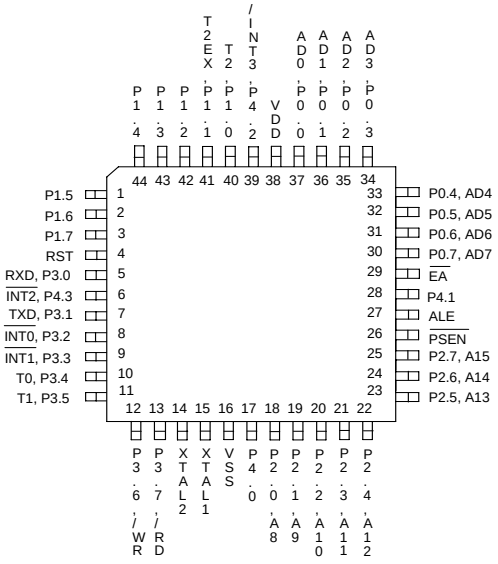
40-Pin DIP



44-Pin PLCC



44-Pin QFP



4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute the external ROM. The ROM address and data will not be presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency.
RST	I L	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	CRYSTAL 1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	CRYSTAL 2: This is the crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	I	GROUND: ground potential.
V_{DD}	I	POWER SUPPLY: Supply voltage for operation.
P0.0–P0.7	I/O D	PORT 0: Function is the same as that of standard 8052.
P1.0–P1.7	I/O H	PORT 1: Function is the same as that of standard 8052.
P2.0–P2.7	I/O H	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0–P3.7	I/O H	PORT 3: Function is the same as that of the standard 8052.
P4.0–P4.3	I/O H	PORT 4: A bi-directional I/O. See details below.

*** Note: TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

5. FUNCTIONAL DESCRIPTION

The W78L058A architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, one special purpose programmable 4-bits I/O port, 512 bytes of RAM, three timer/counters, a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

RAM

The internal data RAM in the W78L058A is 512 bytes. It is divided into two banks: 256 bytes of scratchpad RAM and 256 bytes of AUX-RAM. These RAMs are addressed by different ways.

- RAM 0H–7FH can be addressed directly and indirectly as the same as in 8051. Address pointers are R0 and R1 of the selected register bank.
- RAM 80H–FFH can only be addressed indirectly as the same as in 8051. Address pointers are R0, R1 of the selected registers bank.
- AUX-RAM 0H–FFH is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointer are R0 and R1 of the selected register bank and DPTR register. An access to external data memory locations higher than FFH will be performed with the MOVX instruction in the same way as in the 8051. The AUX-RAM is disable after a reset. Setting the bit 4 in CHPCON register will enable the access to AUX-RAM. When AUX-RAM is enabled the instructions of "MOVX @Ri" will always access to on-chip AUX-RAM. When executing from internal program memory, an access to AUX-RAM will not affect the Ports P0, P2, $\overline{WR}$ and $\overline{RD}$.

Example,

```
CHPENR    REG     F6H
CHPCON    REG     BFH
MOV       CHPENR,#87H
MOV       CHPENR,#59H
ORL       CHPCON,#00010000B   ; enable AUX-RAM
MOV       CHPENR,#00H
MOV       R0,#12H
MOV       A,#34H
MOVX      @R0,A               ; Write 34h data to 12h address.
```

Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2. The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

W78L058A Special Function Registers (SFRs) and Reset Values

F8									FF
F0	+B 00000000						**CHPENR** **00000000**		F7
E8									EF
E0	+ACC 00000000								E7
D8	**+P4** **xxxx1111**								DF
D0	+PSW 00000000								D7
C8	+T2CON 00000000		RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	XICON 00000000		**P4CONA** **00000000**	**P4CONB** **00000000**	**SFRAL** **00000000**	**SFRAH** **00000000**	**SFRFD** **00000000**	**SFRCN** **00000000**	C7
B8	+IP 00000000							**CHPCON** **0xx00000**	BF
B0	+P3 00000000				**P43AL** **00000000**	**P43AH** **00000000**			B7
A8	+IE 00000000				**P42AL** **00000000**	**P42AH** **00000000**	**P2ECON** **0000xx00**		AF
A0	+P2 11111111								A7
98	+SCON 00000000	SBUF xxxxxxxx							9F
90	+P1 11111111				**P41AL** **00000000**	**P41AH** **00000000**			97
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8F
80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000	**P40AL** **00000000**	**P40AH** **00000000**		PCON 00110000	87

Notes:

1.The SFRs marked with a plus sign(+) are both byte- and bit-addressable.

2. The text of SFR with bold type characters are extension function registers.

Port 4

Port 4, address D8H, is a 4-bit multipurpose programmable I/O port. Each bit can be configured individually by software. The Port 4 has four different operation modes.

Mode 0: P4.0–P4.3 is a bi-directional I/O port which is same as port 1. P4.2 and P4.3 also serve as external interrupt $\overline{PSEN}$ and $\overline{INT2}$ if enabled.

Mode 1: P4.0–P4.3 are read strobe signals that are synchronized with $\overline{RD}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

Mode 2: P4.0–P4.3 are write strobe signals that are synchronized with $\overline{WR}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

P4CONB (C3H)

BIT	NAME	FUNCTION
7, 6	P43FUN1 P43FUN0	00: Mode 0. P4.3 is a general purpose I/O port which is the same as Port1. 01: Mode 1. P4.3 is a Read Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 10: Mode 2. P4.3 is a Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 11: Mode 3. P4.3 is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1, and P43CMP0.
5, 4	P43CMP1 P43CMP0	Chip-select signals address comparison: 00: Compare the full address (16 bits length) with the base address register P43AH, P43AL. 01: Compare the 15 high bits (A15–A1) of address bus with the base address register P43AH, P43AL. 10: Compare the 14 high bits (A15–A2) of address bus with the base address register P43AH, P43AL. 11: Compare the 8 high bits (A15–A8) of address bus with the base address register P43AH, P43AL.
3, 2	P42FUN1 P42FUN0	The P4.2 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P42CMP1 P42CMP0	The P4.2 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

P4CONA (C2H)

BIT	NAME	FUNCTION
7, 6	P41FUN1 P41FUN0	The P4.1 function control bits which are the similar definition as P43FUN1, P43FUN0.
5, 4	P41CMP1 P41CMP0	The P4.1 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.
3, 2	P40FUN1 P40FUN0	The P4.0 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P40CMP1 P40CMP0	The P4.0 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

P2ECON (AEH)

BIT	NAME	FUNCTION
7	P43CSINV	The active polarity of P4.3 when pin P4.3 is defined as read and/or write strobe signal. = 1: P4.3 is active high when pin P4.3 is defined as read and/or write strobe signal. = 0: P4.3 is active low when pin P4.3 is defined as read and/or write strobe signal.
6	P42CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
4	P40CSINV	The similarity definition as P43SINV.
3	-	Reserve
2	-	Reserve
1	-	0
0	-	0

Port 4 Base Address Registers

P40AH, P40AL:

The Base address register for comparator of P4.0. P40AH contains the high-order byte of address, P40AL contains the low-order byte of address.

P41AH, P41AL:

The Base address register for comparator of P4.1. P41AH contains the high-order byte of address, P41AL contains the low-order byte of address.

P42AH, P42AL:

The Base address register for comparator of P4.2. P42AH contains the high-order byte of address, P42AL contains the low-order byte of address.

P43AH, P43AL:

The Base address register for comparator of P4.3. P43AH contains the high-order byte of address, P43AL contains the low-order byte of address.

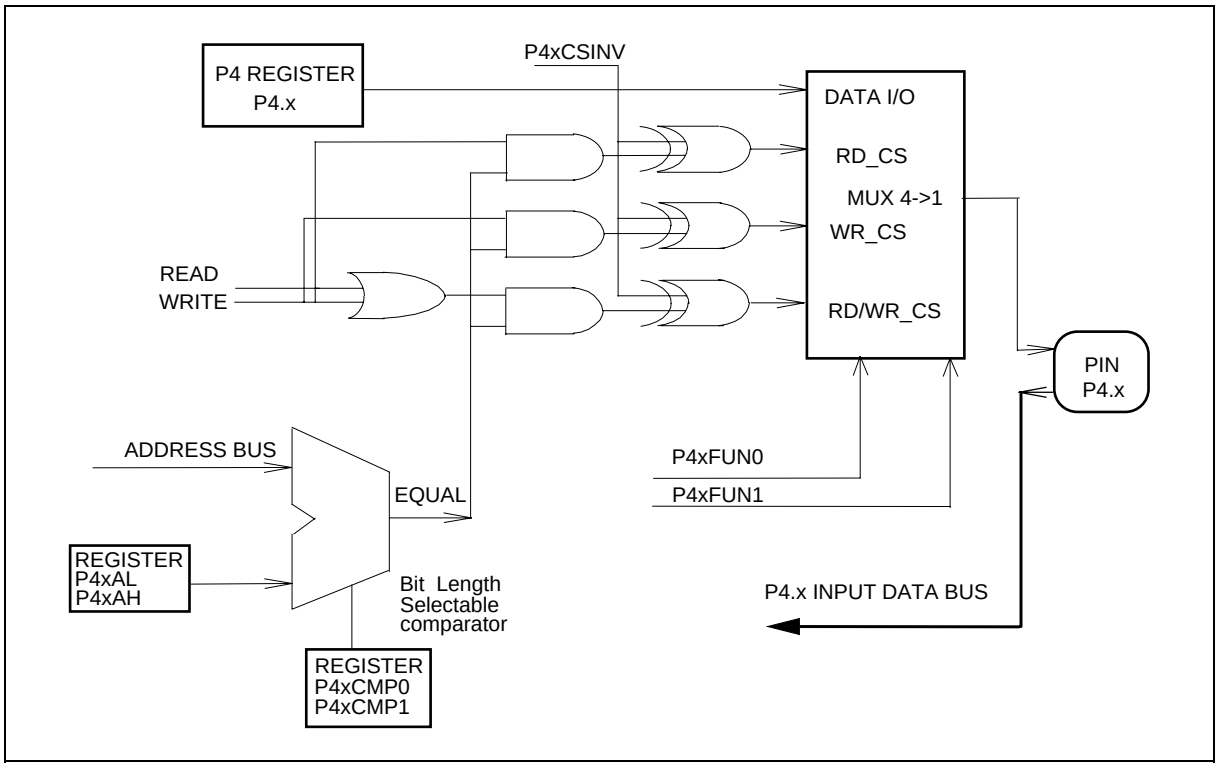
P4 (D8H)

BIT	NAME	FUNCTION
7	-	Reserve
6	-	Reserve
5	-	Reserve
4	-	Reserve
3	P43	Port 4 Data bit which outputs to pin P4.3 at mode 0.
2	P42	Port 4 Data bit. which outputs to pin P4.2 at mode 0.
1	P41	Port 4 Data bit. which outputs to pin P4.1at mode 0.
0	P40	Port 4 Data bit which outputs to pin P4.0 at mode 0.

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H–1237H and positive polarity, and P4.1–P4.3 are used as general I/O ports.

```
MOV  P40AH,#12H
MOV  P40AL,#34H          ; Base I/O address 1234H for P4.0
MOV  P4CONA,#00001010B   ; P4.0 a write strobe signal and address line A0 and A1 are masked.
MOV  P4CONB,#00H         ; P4.1–P4.3 as general I/O port which are the same as PORT1
MOV  P2ECON,#10H         ; Write the P40SINV = 1 to inverse the P4.0 write strobe polarity
                         ; default is negative.
```

Then any instruction MOVX @DPTR,A (with DPTR = 1234H–1237H) will generate the positive polarity write strobe signal at pin P4.0. And the instruction MOV P4,#XX will output the bit3 to bit1 of data #XX to pin P4.3–P4.1.



In-System Programming (ISP) Mode

The W78L058A equips one 32K byte of main ROM bank for application program (called APROM) and one 4K byte of auxiliary ROM bank for loader program (called LDROM). In the normal operation, the microcontroller executes the code in the APROM. If the content of APROM needs to be modified, the W78L058A allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write**

In-System Programming Control Register (CHPCON)

CHPCON (BFH)

BIT	NAME	FUNCTION
7	SWRESET (F04KMODE)	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation. To read this bit in logic-1 can determine that the F04KBOOT mode is running.
6	-	Reserve.
5	-	Reserve.
4	ENAUXRAM	1: Enable on-chip AUX-RAM. 0: Disable the on-chip AUX-RAM
3	0	Must set to 0.
2	0	Must set to 0.
1	FBOOTSL	The Program Location Select. 0: The Loader Program locates at the 32 KB APROM. 4KB LDROM is destination for re-programming. 1: The Loader Program locates at the 4 KB memory bank. 32KB APROM is destination for re-programming.
0	FPROGEN	ROM Programming Enable. = 1: enable. The microcontroller enter the in-system programming mode after entering the idle mode and wake-up from interrupt. During in-system programming mode, the operation of erase, program and read are achieve when device enters idle mode. = 0: disable. The on-chip flash memory is read-only. In-system programmability is disabled.

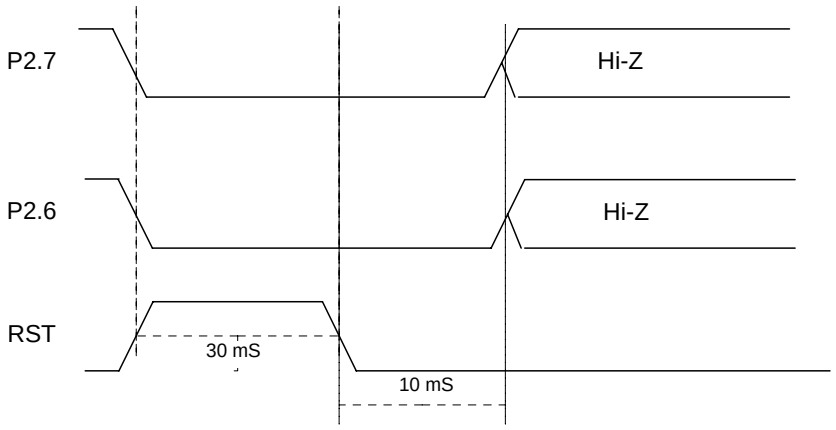
F04KBOOT Mode (Boot From LDROM)

By default, the W78L058A boots from APROM program after a power on reset. On some occasions, user can force the W78L058A to boot from the LDROM program via following settings. The possible situation that you need to enter F04KBOOT mode when the APROM program can not run properly and device can not jump back to LDROM to execute in-system programming function. Then you can use this F04KBOOT mode to force the W78L058A jumps to LDROM and executes in-system programming procedure. When you design your system, you may reserve the pins P2.6, P2.7 to switches or jumpers. For example in a CD-ROM system, you can connect the P2.6 and P2.7 to PLAY and EJECT buttons on the panel. When the APROM program fails to execute the normal application program. User can press both two buttons at the same time and then turn on the power of the personal computer to force the W78L058A to enter the F04KBOOT mode. After power on of personal computer, you can release both buttons and finish the in-system programming procedure to update the APROM code. In application system design, user must take care of the P2, P3, ALE, $\overline{EA}$ and $\overline{PSEN}$ pin value at reset to prevent from accidentally activating the programming mode or F04KBOOT mode.

F04KBOOT MODE

P4.3	P2.7	P2.6	MODE
X	L	L	FO4KBOOT
L	X	X	FO4KBOOT

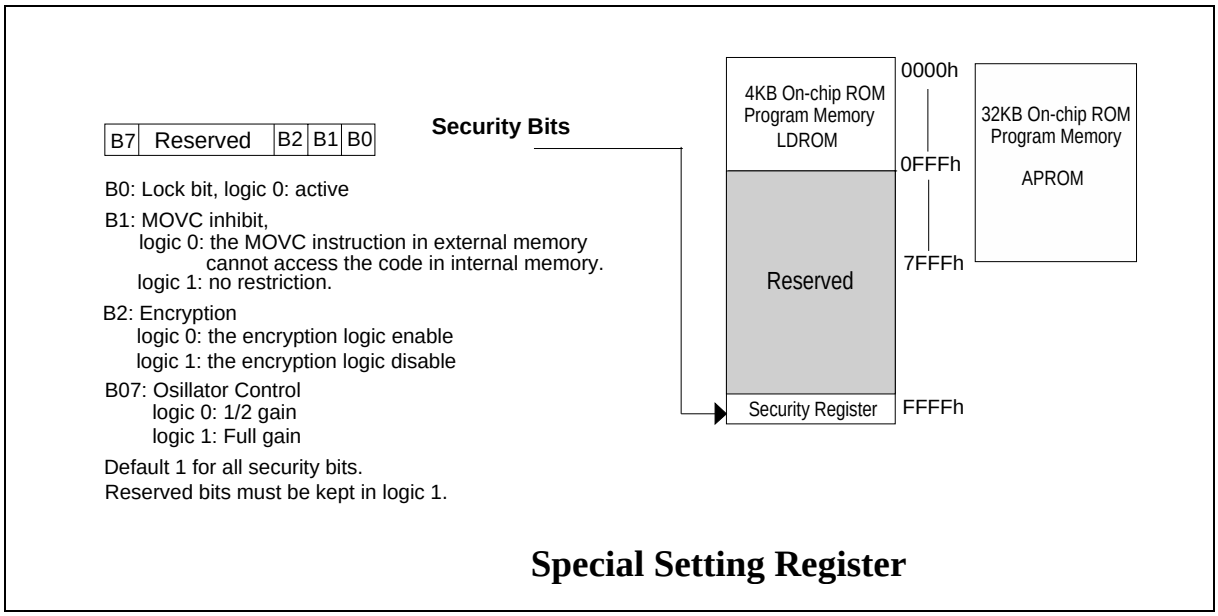
The Reset Timing For Entering F04KBOOT Mode



6. SECURITY

During the on-chip ROM programming mode, the ROM can be programmed and verified repeatedly. Until the code inside the ROM is confirmed OK, the code can be protected. The protection of ROM and those operations on it are described below.

The W78L058A has a Security Register that can be accessed in programming mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is located at the 0FFFFH of the LDROM space.



Special Setting Register

Lock bit

This bit is used to protect the customer's program code in the W78L058A. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the ROM data and Security Register can not be accessed again.

MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

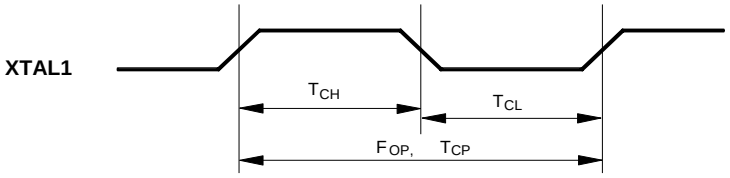
Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.

9. AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	FOP	0	-	20	MHz	1
Clock Period	TCP	50	-	-	nS	2
Clock High	TCH	25	-	-	nS	3
Clock Low	TCL	25	-	-	nS	3

Notes:
1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP-Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP-Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP-Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP-Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP-Δ	3 TCP	-	nS	4

Notes:
1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	T_{DAR}	3 T_{CP}-Δ	-	3 T_{CP}+Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	T_{DDA}	-	-	4 T_{CP}	nS	1
Data Hold from $\overline{RD}$ High	T_{DDH}	0	-	2 T_{CP}	nS	
Data Float from $\overline{RD}$ High	T_{DDZ}	0	-	2 T_{CP}	nS	
$\overline{RD}$ Pulse Width	T_{DRD}	6 T_{CP}-Δ	6 T_{CP}	-	nS	2

Notes:
1. Data memory access time is 8 T_{CP}.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	T_{DAW}	3 T_{CP}-Δ	-	3 T_{CP}+Δ	nS
Data Valid to $\overline{WR}$ Low	T_{DAD}	1 T_{CP}-Δ	-	-	nS
Data Hold from $\overline{WR}$ High	T_{DWD}	1 T_{CP}-Δ	-	-	nS
$\overline{WR}$ Pulse Width	T_{DWR}	6 T_{CP}-Δ	6 T_{CP}	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

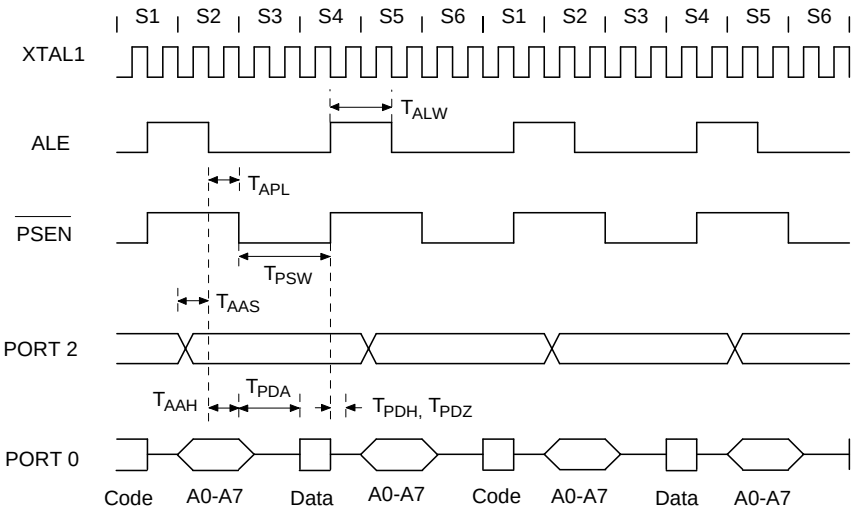
Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	T_{PDS}	1 TCP	-	-	nS
Port Input Hold from ALE Low	T_{PDH}	0	-	-	nS
Port Output to ALE	T_{PDA}	1 TCP	-	-	nS

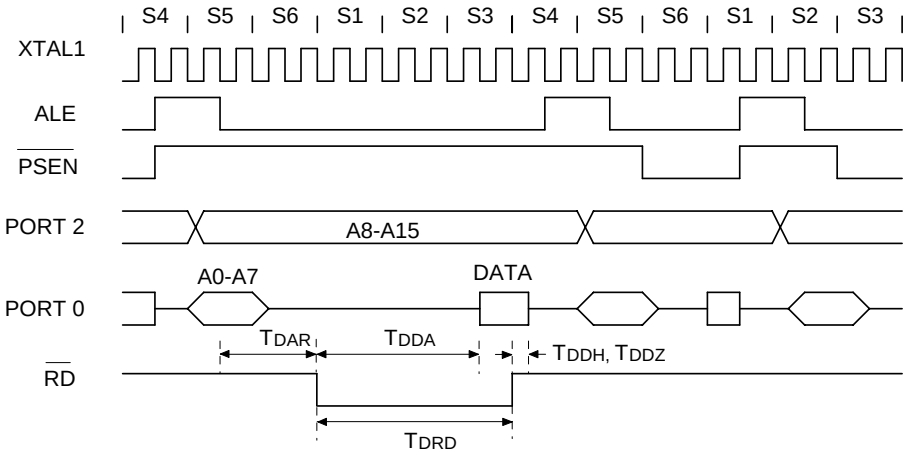
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

10. TIMING WAVEFORMS

Program Fetch Cycle

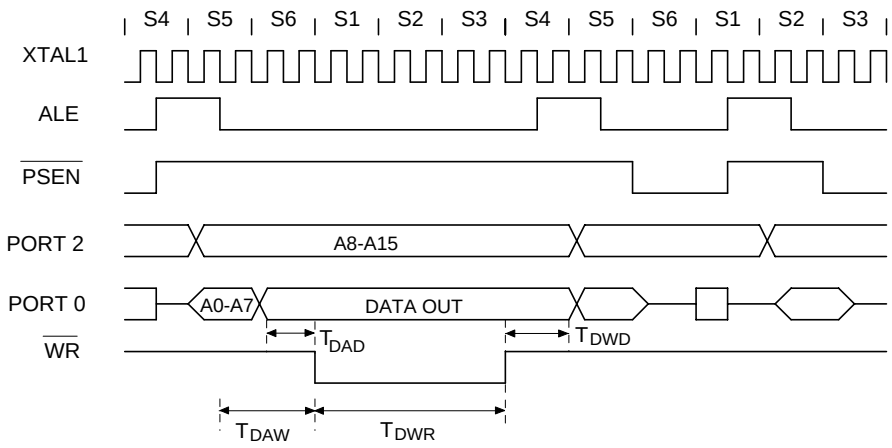


Data Read Cycle

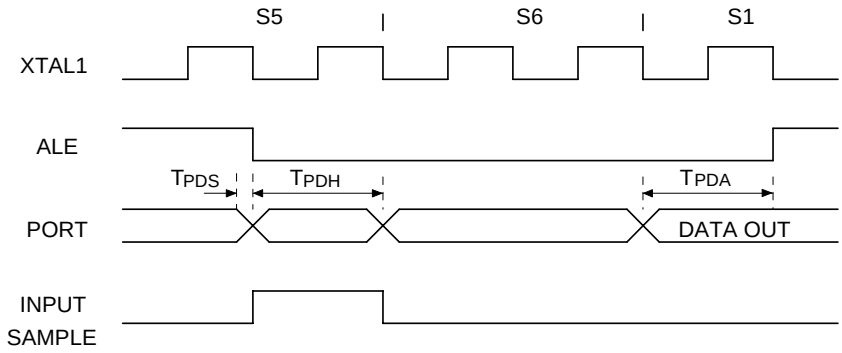


Timing Waveforms, continued

Data Write Cycle



Port Access Cycle



Typical Application Circuit, continued

11.1 Expanded External Data Memory and Oscillator

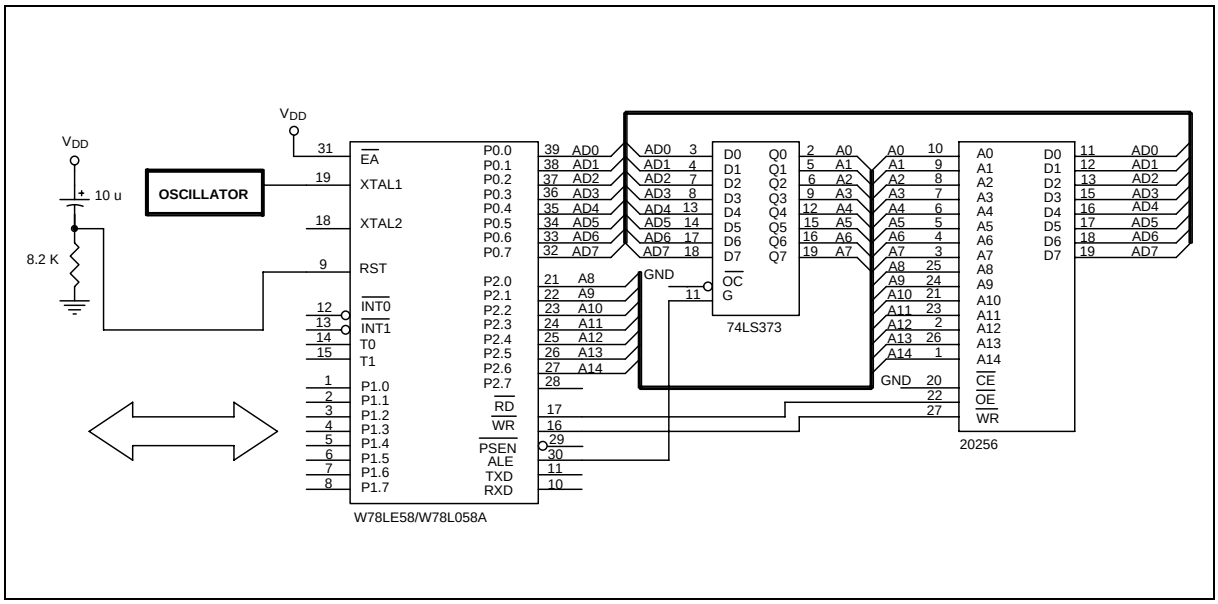
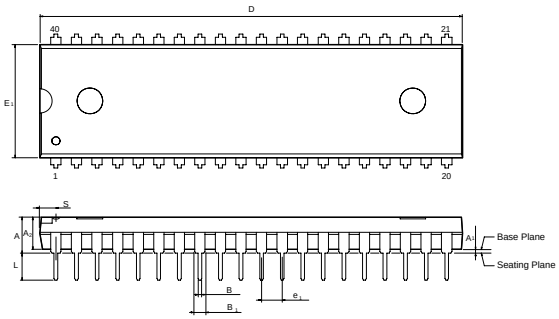


Figure B

12. PACKAGE DIMENSIONS

40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

Application Note: In-system Programming Software Examples

This application note illustrates the in-system programmability of the Winbond W78L058A ROM microcontroller. In this example, microcontroller will boot from 32KB APROM bank and waiting for a key to enter in-system programming mode for re-programming the contents of 32KB APROM. While entering in-system programming mode, microcontroller executes the loader program in 4KB LDROM bank. The loader program erases the 32KB APROM then reads the new code data from external SRAM buffer (or through other interfaces) to update the 32KB APROM.

EXAMPLE 1:

```
;*********************************************************************************************************************
;* Example of 32K APROM program: Program will scan the P1.0. if P1.0 = 0, enters in-system
;* programming mode for updating the content of APROM code else executes the current ROM code.
;* XTAL = 16 MHz
;*********************************************************************************************************************
        .chip 8052
        .RAMCHK OFF
        .symbols

        CHPCON    EQU     BFH
        CHPENR    EQU     F6H
        SFRAL     EQU     C4H
        SFRAH     EQU     C5H
        SFRFD     EQU     C6H
        SFRCN     EQU     C7H

        ORG     0H
        LJMP    100H                    ; JUMP TO MAIN PROGRAM
    ;*************************************************************************
    ;*  TIMER0 SERVICE VECTOR ORG = 000BH
    ;*************************************************************************
        ORG     00BH
        CLR     TR0                     ; TR0 = 0, STOP TIMER0
        MOV     TL0,R6
        MOV     TH0,R7
        RETI
    ;*************************************************************************
    ;*  32K APROM MAIN PROGRAM
    ;*************************************************************************
       ORG 100H

MAIN_32K:
        MOV A,P1                        ; SCAN P1.0
        ANL A,#01H
        CJNE A,#01H,PROGRAM_32K ; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING MODE
        JMP NORMAL_MODE

PROGRAM_32K:
        MOV CHPENR,#87H                 ; CHPENR = 87H, CHPCON REGISTER WRTE ENABLE
        MOV CHPENR,#59H                 ; CHPENR = 59H, CHPCON REGISTER WRITE ENABLE
        MOV CHPCON,#03H                 ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
        MOV TCON,#00H                   ; TR = 0 TIMER0 STOP
        MOV IP,#00H                     ; IP = 00H
        MOV IE,#82H                     ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
```

```
        MOV R6,#F0H             ; TL0 = F0H
        MOV R7,#FFH             ; TH0 = FFH
        MOV TL0,R6
        MOV TH0,R7
        MOV TMOD,#01H             ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
        MOV TCON,#10H           ; TCON = 10H, TR0 = 1,GO
        MOV PCON,#01H           ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM
                                ; PROGRAMMING
;*****************************************************************************
;* Normal mode 32KB APROM program: depending user's application
;*****************************************************************************
NORMAL_MODE:
            .                   ; User's application program
            .
            .
            .
```

EXAMPLE 2:

```
;*************************************************************************************************************************
Example of 4 KB LDROM program: This loader program will erase the 32KB APROM first, then reads the new ;*
code from external SRAM and program them into 32 KB APROM bank. XTAL = 16 MHz
;*************************************************************************************************************************
    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON     EQU    BFH
    CHPENR     EQU    F6H
    SFRAL      EQU    C4H
    SFRAH      EQU    C5H
    SFRFD      EQU    C6H
    SFRCN      EQU    C7H

        ORG    000H
        LJMP   100H             ; JUMP TO MAIN PROGRAM
  ;*************************************************************************
  ;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
  ;*************************************************************************
        ORG 000BH
        CLR   TR0               ; TR0 = 0, STOP TIMER0
        MOV TL0,R6
        MOV TH0,R7
        RETI
  ;*************************************************************************
  ;*  4KB LDROM MAIN PROGRAM
  ;*************************************************************************
       ORG 100H
```

```
        INC SFRAL               ; NEXT ADDRESS
        MOV A,SFRAL
        JNZ BLANK_CHECK_LOOP
        INC SFRAH
        MOV A,SFRAH
        CJNE A,#80H,BLANK_CHECK_LOOP   ; END ADDRESS = 7FFFH
        JMP PROGRAM_32KROM

BLANK_CHECK_ERROR:
        MOV P1,#F0H
        MOV P3,#F0H
        JMP $

;*******************************************************************************
;* RE-PROGRAMMING 32KB APROM BANK
;*******************************************************************************
PROGRAM_32KROM:
        MOV DPTR,#0H            ; THE ADDRESS OF NEW ROM CODE
        MOV R2,#00H             ; TARGET LOW BYTE ADDRESS
        MOV R1,#00H             ; TARGET HIGH BYTE ADDRESS
        MOV DPTR,#0H            ; EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH,R1              ; SFRAH, TARGET  HIGH ADDRESS
        MOV SFRCN,#21H          ; SFRCN(C7H) = 21 (PROGRAM 32K)
        MOV R6,#BEH             ; SET TIMER FOR PROGRAMMING, ABOUT 50 μS.
        MOV R7,#FFH
        MOV TL0,R6
        MOV TH0,R7

PROG_D_32K:
        MOV SFRAL,R2            ; SFRAL(C4H) = LOW BYTE ADDRESS
        MOVX A,@DPTR            ; READ DATA FROM EXTERNAL SRAM BUFFER. BY ACCORDING USER?
                                ; CIRCUIT, USER MUST MODIFY THIS INSTRUCTION TO FETCH CODE
        MOV SFRFD,A             ; SFRFD(C6H) = DATA IN
        MOV TCON,#10H           ; TCON = 10H, TR0 = 1,GO
        MOV PCON,#01H           ; ENTER IDLE MODE (PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2,#0H,PROG_D_32K
        INC  R1
        MOV SFRAH,R1
        CJNE R1,#80H,PROG_D_32K

;*******************************************************************************
; * VERIFY 32KB APROM BANK
;*******************************************************************************
        MOV R4,#03H             ; ERROR COUNTER
        MOV R6,#FEH             ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.
        MOV R7,#FFH
        MOV TL0,R6
        MOV TH0,R7
        MOV DPTR,#0H            ; The start address of sample code
        MOV R2,#0H              ; Target  low byte address
        MOV R1,#0H              ; Target  high byte address
        MOV SFRAH,R1            ; SFRAH, Target high address
        MOV SFRCN,#00H          ; SFRCN = 00 (Read ROM CODE)
```

13. REVISION HISTORY

VERSION	DATE	PAGE	REASONS FOR CHANGE
A2	November 2000		-
A3	April 19, 2005	32	Add Important Notice
A4	November 14, 2005	2	Add Lead-free(RoHS) parts
A5	October 2, 2006		Remove block diagram Change operating frequency into 20MHz
A6	December 4, 2006	2	Remove all Leaded package parts

Important Notice

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