Nuvoton Technology Corporation - W78L058A24PL Datasheet

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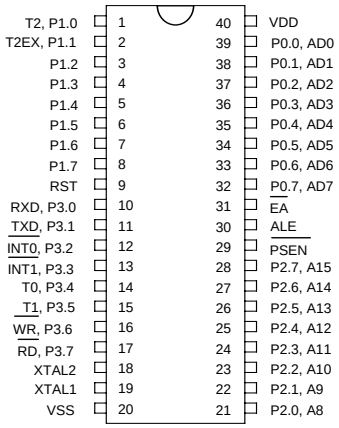
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

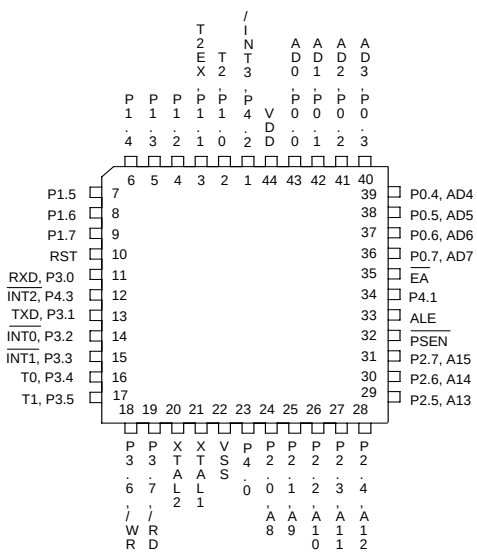
Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 60°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78l058a24pl

3. PIN CONFIGURATIONS

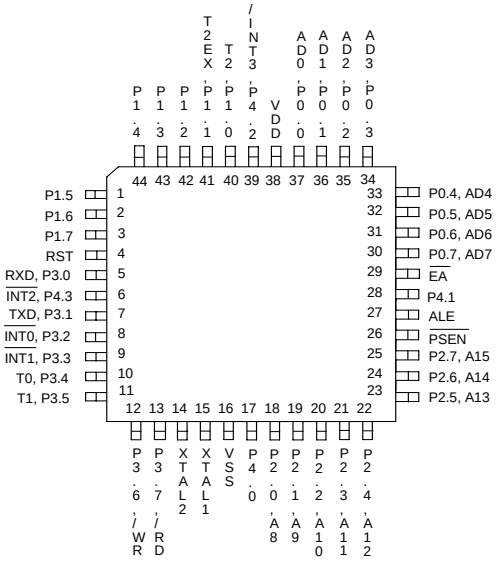
40-Pin DIP



44-Pin PLCC



44-Pin QFP



4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute the external ROM. The ROM address and data will not be presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency.
RST	I L	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	CRYSTAL 1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	CRYSTAL 2: This is the crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	I	GROUND: ground potential.
V_{DD}	I	POWER SUPPLY: Supply voltage for operation.
P0.0–P0.7	I/O D	PORT 0: Function is the same as that of standard 8052.
P1.0–P1.7	I/O H	PORT 1: Function is the same as that of standard 8052.
P2.0–P2.7	I/O H	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0–P3.7	I/O H	PORT 3: Function is the same as that of the standard 8052.
P4.0–P4.3	I/O H	PORT 4: A bi-directional I/O. See details below.

*** Note: TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

Clock

The W78L058A is designed with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78L058A relatively insensitive to duty cycle variations in the clock.

Crystal Oscillator

The W78L058A incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground.

External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.

Power Management

Idle Mode

Setting the IDL bit in the PCON register enters the idle mode. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. To exit from power-down mode is by a hardware reset or external interrupts $\overline{\text{INT0}}$ to $\overline{\text{INT1}}$ when enabled and set to level triggered.

Reduce EMI Emission

The W78L058A allows user to diminish the gain of on-chip oscillator amplifier by using programmer to clear the B7 bit of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may affect the external crystal operating improperly at high frequency. The value of C1 and C2 may need some adjustment while running at lower gain.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78L058A is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

P4CONB (C3H)

BIT	NAME	FUNCTION
7, 6	P43FUN1 P43FUN0	00: Mode 0. P4.3 is a general purpose I/O port which is the same as Port1. 01: Mode 1. P4.3 is a Read Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 10: Mode 2. P4.3 is a Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 11: Mode 3. P4.3 is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1, and P43CMP0.
5, 4	P43CMP1 P43CMP0	Chip-select signals address comparison: 00: Compare the full address (16 bits length) with the base address register P43AH, P43AL. 01: Compare the 15 high bits (A15–A1) of address bus with the base address register P43AH, P43AL. 10: Compare the 14 high bits (A15–A2) of address bus with the base address register P43AH, P43AL. 11: Compare the 8 high bits (A15–A8) of address bus with the base address register P43AH, P43AL.
3, 2	P42FUN1 P42FUN0	The P4.2 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P42CMP1 P42CMP0	The P4.2 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

P4CONA (C2H)

BIT	NAME	FUNCTION
7, 6	P41FUN1 P41FUN0	The P4.1 function control bits which are the similar definition as P43FUN1, P43FUN0.
5, 4	P41CMP1 P41CMP0	The P4.1 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.
3, 2	P40FUN1 P40FUN0	The P4.0 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P40CMP1 P40CMP0	The P4.0 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

P2ECON (AEH)

BIT	NAME	FUNCTION
7	P43CSINV	The active polarity of P4.3 when pin P4.3 is defined as read and/or write strobe signal. = 1: P4.3 is active high when pin P4.3 is defined as read and/or write strobe signal. = 0: P4.3 is active low when pin P4.3 is defined as read and/or write strobe signal.
6	P42CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
4	P40CSINV	The similarity definition as P43SINV.
3	-	Reserve
2	-	Reserve
1	-	0
0	-	0

Port 4 Base Address Registers

P40AH, P40AL:

The Base address register for comparator of P4.0. P40AH contains the high-order byte of address, P40AL contains the low-order byte of address.

P41AH, P41AL:

The Base address register for comparator of P4.1. P41AH contains the high-order byte of address, P41AL contains the low-order byte of address.

P42AH, P42AL:

The Base address register for comparator of P4.2. P42AH contains the high-order byte of address, P42AL contains the low-order byte of address.

P43AH, P43AL:

The Base address register for comparator of P4.3. P43AH contains the high-order byte of address, P43AL contains the low-order byte of address.

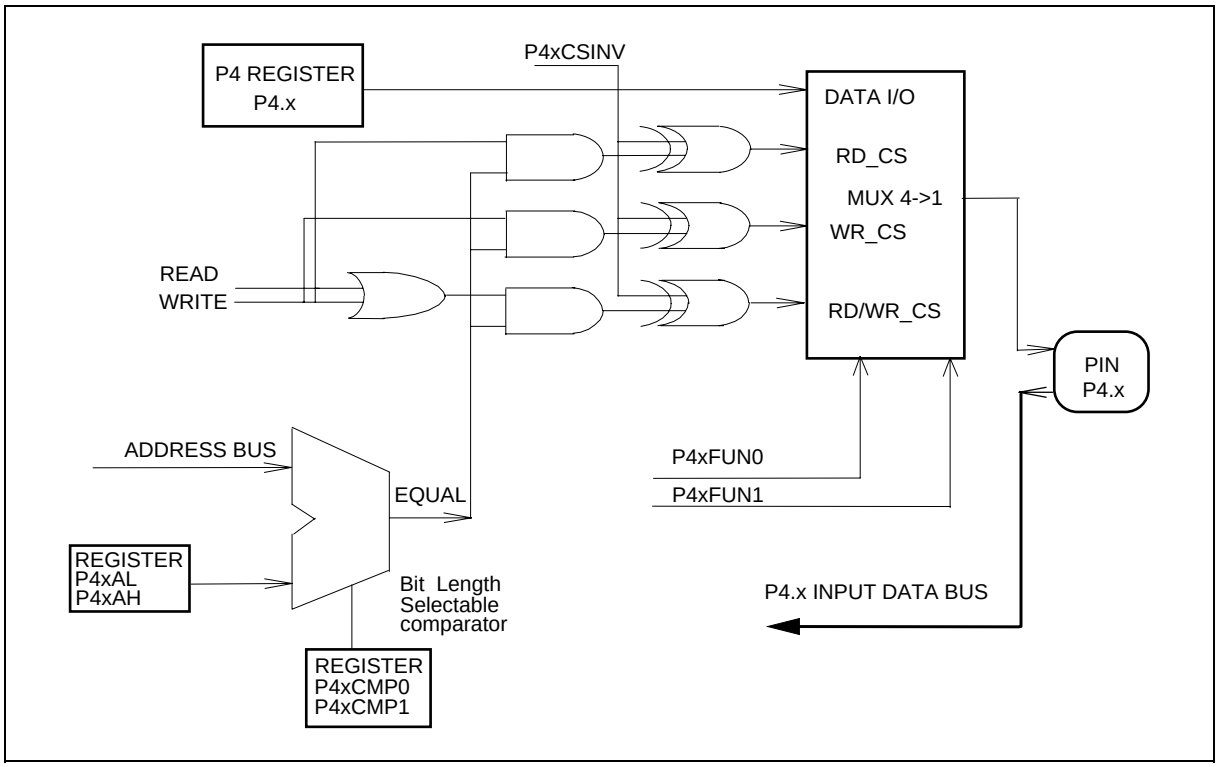
P4 (D8H)

BIT	NAME	FUNCTION
7	-	Reserve
6	-	Reserve
5	-	Reserve
4	-	Reserve
3	P43	Port 4 Data bit which outputs to pin P4.3 at mode 0.
2	P42	Port 4 Data bit. which outputs to pin P4.2 at mode 0.
1	P41	Port 4 Data bit. which outputs to pin P4.1at mode 0.
0	P40	Port 4 Data bit which outputs to pin P4.0 at mode 0.

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H–1237H and positive polarity, and P4.1–P4.3 are used as general I/O ports.

```
MOV  P40AH,#12H
MOV  P40AL,#34H          ; Base I/O address 1234H for P4.0
MOV  P4CONA,#00001010B   ; P4.0 a write strobe signal and address line A0 and A1 are masked.
MOV  P4CONB,#00H         ; P4.1–P4.3 as general I/O port which are the same as PORT1
MOV  P2ECON,#10H         ; Write the P40SINV = 1 to inverse the P4.0 write strobe polarity
                         ; default is negative.
```

Then any instruction MOVX @DPTR,A (with DPTR = 1234H–1237H) will generate the positive polarity write strobe signal at pin P4.0. And the instruction MOV P4,#XX will output the bit3 to bit1 of data #XX to pin P4.3–P4.1.



In-System Programming (ISP) Mode

The W78L058A equips one 32K byte of main ROM bank for application program (called APROM) and one 4K byte of auxiliary ROM bank for loader program (called LDROM). In the normal operation, the microcontroller executes the code in the APROM. If the content of APROM needs to be modified, the W78L058A allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write**

attribute. The W78L058A achieves all in-system programming operations including enter/exit ISP Mode, program, erase, read ... etc, during device in the idle mode. Setting the bit CHPCON.0 the device will enter in-system programming mode after a wake-up from idle mode. Because device needs proper time to complete the ISP operations before awaken from idle mode, software may use timer interrupt to control the duration for device wake-up from idle mode. To perform ISP operation for revising contents of APROM, software located at APROM setting the CHPCON register then enter idle mode, after awaken from idle mode the device executes the corresponding interrupt service routine in LDROM. Because the device will clear the program counter while switching from APROM to LDROM, the first execution of RETI instruction in interrupt service routine will jump to 00H at LDROM area. The device offers a software reset for switching back to APROM while the content of APROM has been updated completely. **Setting CHPCON register bit 0, 1 and 7 to logic-1 will result a software reset to reset the CPU**. The software reset serves as a external reset. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible to easily update the system firmware without opening the chassis.

Note: The ISP Mode operates by supply voltage from 3.3V to 5.5V.

SFRAH, SFRAL: The objective address of on-chip ROM in the in-system programming mode. SFRAH contains the high-order byte of address, SFRAL contains the low-order byte of address.

SFRFD: The programming data for on-chip ROM in programming mode.

SFRCN: The control byte of on-chip ROM programming mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip ROM bank select for in-system programming. = 0: 32K bytes ROM bank is selected as destination for re-programming. = 1: 4K bytes ROM bank is selected as destination for re-programming.
5	OEN	ROM output enable.
4	CEN	ROM chip enable.
3, 2, 1, 0	CTRL[3:0]	The flash control signals

MODE	WFWIN	CTRL<3:0>	OEN	CEN	SFRAH, SFRAL	SFRFD
Erase 32KB APROM	0	0010	1	0	X	X
Program 32KB APROM	0	0001	1	0	Address in	Data in
Read 32KB APROM	0	0000	0	0	Address in	Data out
Erase 4KB LDROM	1	0010	1	0	X	X
Program 4KB LDROM	1	0001	1	0	Address in	Data in
Read 4KB LDROM	1	0000	0	0	Address in	Data out

In-System Programming Control Register (CHPCON)

CHPCON (BFH)

BIT	NAME	FUNCTION
7	SWRESET (F04KMODE)	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation. To read this bit in logic-1 can determine that the F04KBOOT mode is running.
6	-	Reserve.
5	-	Reserve.
4	ENAUXRAM	1: Enable on-chip AUX-RAM. 0: Disable the on-chip AUX-RAM
3	0	Must set to 0.
2	0	Must set to 0.
1	FBOOTSL	The Program Location Select. 0: The Loader Program locates at the 32 KB APROM. 4KB LDROM is destination for re-programming. 1: The Loader Program locates at the 4 KB memory bank. 32KB APROM is destination for re-programming.
0	FPROGEN	ROM Programming Enable. = 1: enable. The microcontroller enter the in-system programming mode after entering the idle mode and wake-up from interrupt. During in-system programming mode, the operation of erase, program and read are achieve when device enters idle mode. = 0: disable. The on-chip flash memory is read-only. In-system programmability is disabled.

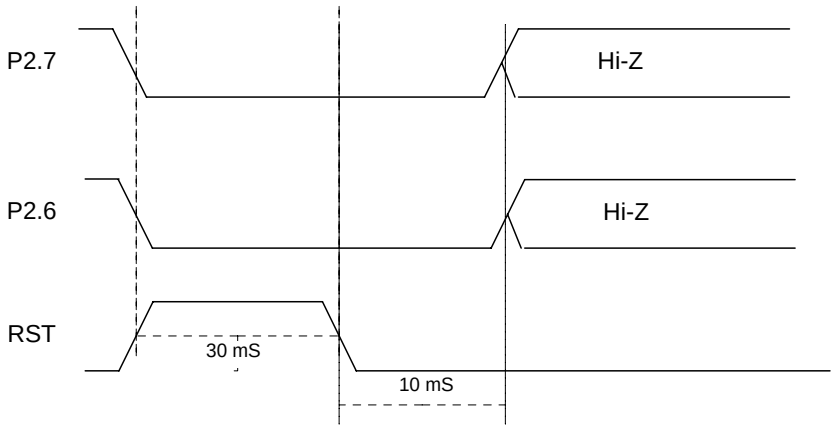
F04KBOOT Mode (Boot From LDROM)

By default, the W78L058A boots from APROM program after a power on reset. On some occasions, user can force the W78L058A to boot from the LDROM program via following settings. The possible situation that you need to enter F04KBOOT mode when the APROM program can not run properly and device can not jump back to LDROM to execute in-system programming function. Then you can use this F04KBOOT mode to force the W78L058A jumps to LDROM and executes in-system programming procedure. When you design your system, you may reserve the pins P2.6, P2.7 to switches or jumpers. For example in a CD-ROM system, you can connect the P2.6 and P2.7 to PLAY and EJECT buttons on the panel. When the APROM program fails to execute the normal application program. User can press both two buttons at the same time and then turn on the power of the personal computer to force the W78L058A to enter the F04KBOOT mode. After power on of personal computer, you can release both buttons and finish the in-system programming procedure to update the APROM code. In application system design, user must take care of the P2, P3, ALE, $\overline{EA}$ and $\overline{PSEN}$ pin value at reset to prevent from accidentally activating the programming mode or F04KBOOT mode.

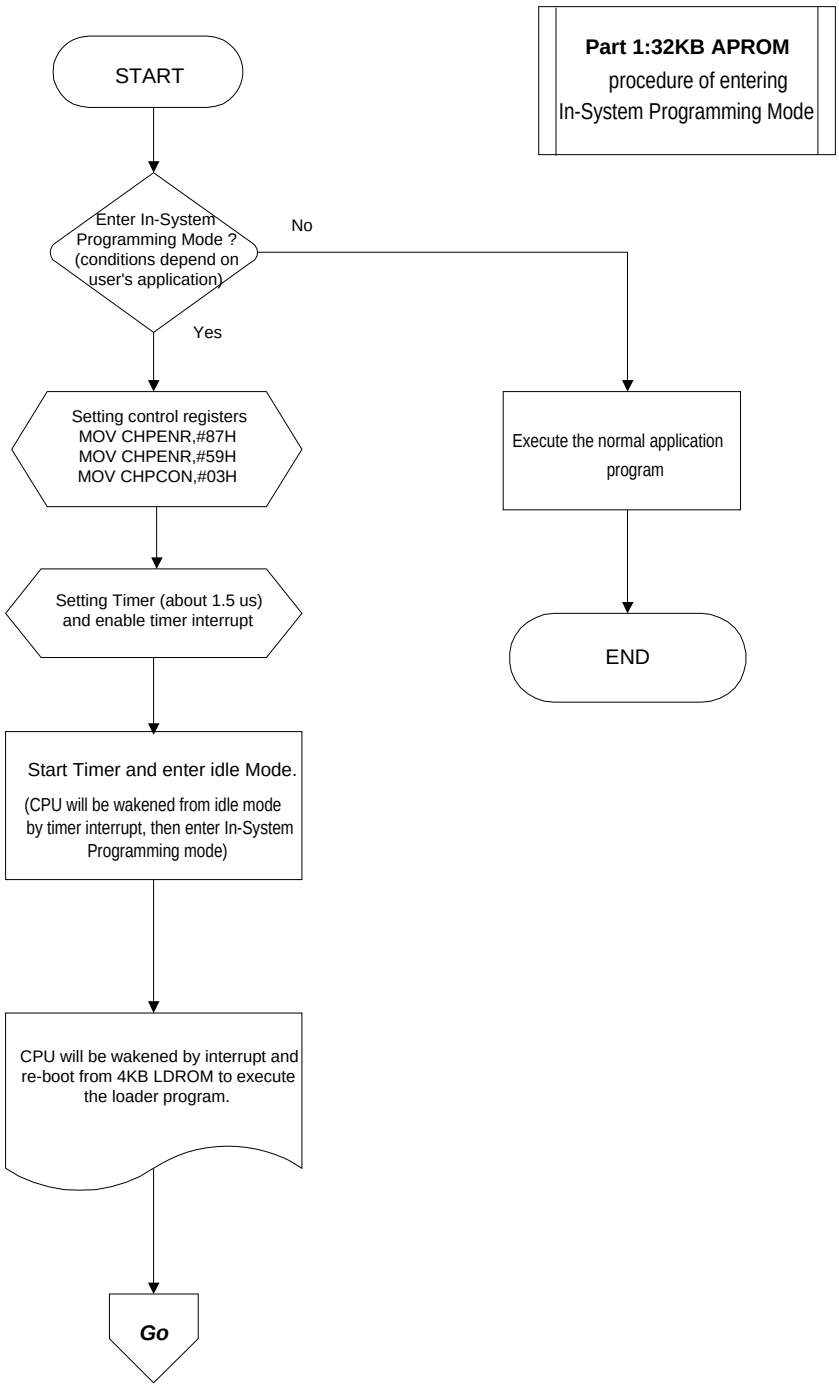
F04KBOOT MODE

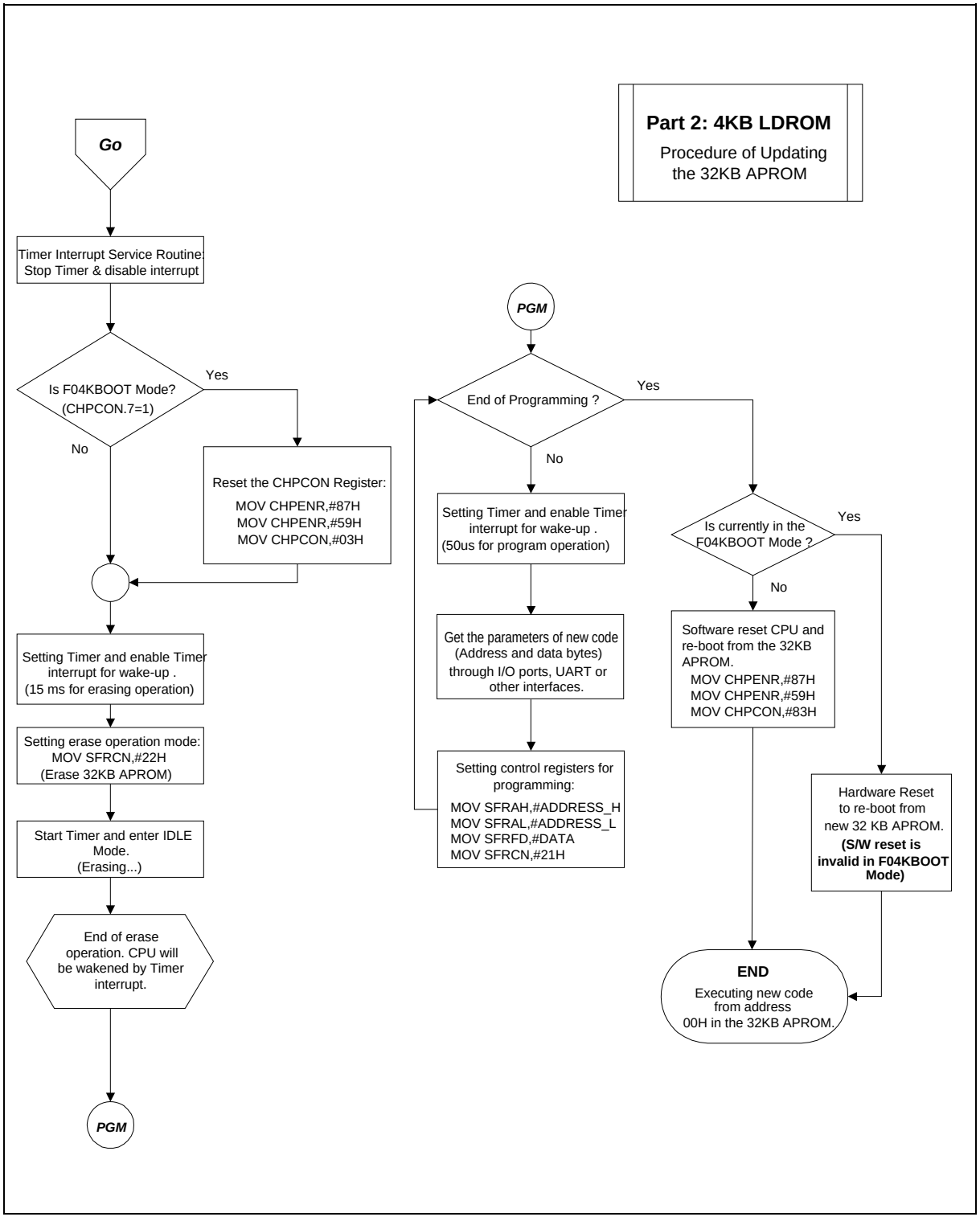
P4.3	P2.7	P2.6	MODE
X	L	L	FO4KBOOT
L	X	X	FO4KBOOT

The Reset Timing For Entering F04KBOOT Mode



The Algorithm of In-System Programming




Part 2: 4KB LDROM
Procedure of Updating the 32KB APROM
Go
Timer Interrupt Service Routine:
Stop Timer & disable interrupt
Is F04KBOOT Mode? (CHPCON.7=1)
Yes
No
Reset the CHPCON Register:
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#03H
Setting Timer and enable Timer interrupt for wake-up . (15 ms for erasing operation)
Setting erase operation mode:
MOV SFRCN,#22H
(Erase 32KB APROM)
Start Timer and enter IDLE Mode.
(Erasing...)
End of erase operation. CPU will be wakened by Timer interrupt.
PGM
PGM
End of Programming ?
Yes
No
Setting Timer and enable Timer interrupt for wake-up . (50us for program operation)
Get the parameters of new code (Address and data bytes) through I/O ports, UART or other interfaces.
Setting control registers for programming:
MOV SFRAH,#ADDRESS_H
MOV SFRAL,#ADDRESS_L
MOV SFRFD,#DATA
MOV SFRCN,#21H
Is currently in the F04KBOOT Mode ?
Yes
No
Software reset CPU and re-boot from the 32KB APROM.
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#83H
Hardware Reset to re-boot from new 32 KB APROM.
(S/W reset is invalid in F04KBOOT Mode)
END
Executing new code from address 00H in the 32KB APROM.

8. DC CHARACTERISTICS

V_{SS} = 0V, T_A = 25° C, unless otherwise specified.

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Operating Voltage	V_{DD}	2.4	5.5	V	Without ISP
	V_{DD}	3.3	5.5	V	With ISP
Operating Current	I_{DD}	-	20	mA	No load V_{DD} = 5.5V
		-	3	mA	No load V_{DD} = 2.4V
Idle Current	I_{IDLE}	-	6	mA	V_{DD} = 5.5V, Fosc = 20 MHz
		-	1.5	mA	V_{DD} = 2.4V, Fosc = 12 MHz
Power Down Current	I_{PWDN}	-	50	µA	V_{DD} = 5.5V, Fosc = 20 MHz
		-	20	µA	V_{DD} = 2.4V, Fosc = 12 MHz
Input Current P1, P2, P3, P4	I_{IN1}	-50	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST	I_{IN2}	-10	+300	µA	V_{DD} = 5.5V 0 < V_{IN} < V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 5.5V 0V < V_{IN} < V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3, P4	I_{TL} [*4]	-500	-	µA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
		0	0.5	V	V_{DD} = 2.4V
Input Low Voltage RST[*1]	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
		0	0.3	V	V_{DD} = 2.4V
Input Low Voltage XTAL1 [*3]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V
		0	0.4	V	V_{DD} = 2.4V
Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.4	V_{DD} +0.2	V	V_{DD} = 2.4V
Input High Voltage RST[*1]	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.7	V_{DD} +0.2	V	V_{DD} = 2.4V
Input High Voltage XTAL1 [*3]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	V_{DD} +0.2	V	V_{DD} = 2.4V

DC CHARACtERISTICS, continued

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Output Low Voltage	V_{OL1}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +2 mA
P1, P2, P3, P4		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +1 mA
Output Low Voltage	V_{OL2}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +4 mA
P0, ALE, $\overline{PSEN}$ [*2]		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +2 mA
Sink Current	I_{SK1}	4	12	mA	V_{DD} = 4.5V, Vin = 0.45V
P1, P2, P3, P4		1.8	5.4	mA	V_{DD} = 2.4V, Vin = 0.45V
Sink Current	I_{SK2}	8	16	mA	V_{DD} = 4.5V, Vin = 0.45V
P0, ALE, $\overline{PSEN}$		4.5	9	mA	V_{DD} = 2.4V, Vin = 0.4V
Output High Voltage	V_{OH1}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -100 μA
P1, P2, P3, P4		1.4	-	V	V_{DD} = 2.4V, I_{OH} = -8 μA
Output High Voltage	V_{OH2}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -400 μA
P0, ALE, $\overline{PSEN}$ [*2]		1.4	-	V	V_{DD} = 2.4V, I_{OH} = -200 μA
Source Current	I_{SR1}	-100	-250	μA	V_{DD} = 4.5V, Vin = 2.4V
P1, P2, P3, P4		-20	-50	μA	V_{DD} = 2.4V, Vin = 1.4V
Source Current	I_{SR2}	-8	-14	mA	V_{DD} = 4.5V, Vin = 2.4V
P0, ALE, $\overline{PSEN}$		-1.9	-3.8	mA	V_{DD} = 2.4V, Vin = 1.4V

Notes:

*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

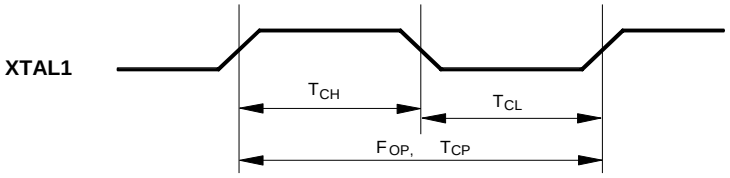
*3. XTAL1 is a CMOS input.

*4. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0.

9. AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	FOP	0	-	20	MHz	1
Clock Period	TCP	50	-	-	nS	2
Clock High	TCH	25	-	-	nS	3
Clock Low	TCL	25	-	-	nS	3

Notes:
1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

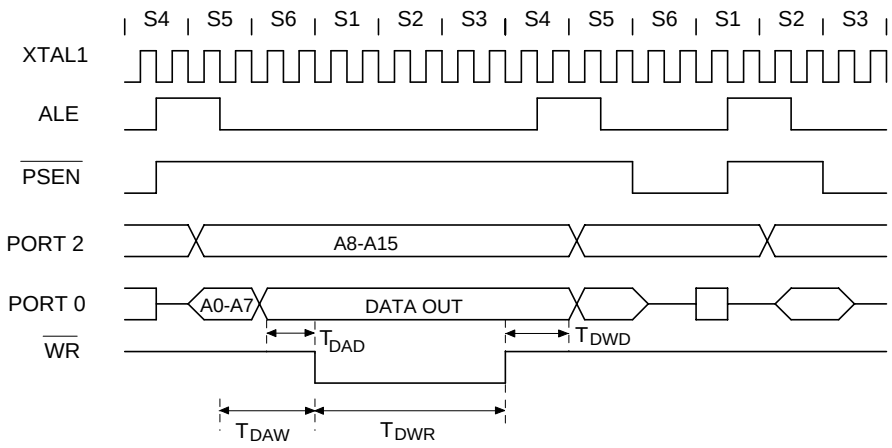
Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP-Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP-Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP-Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP-Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP-Δ	3 TCP	-	nS	4

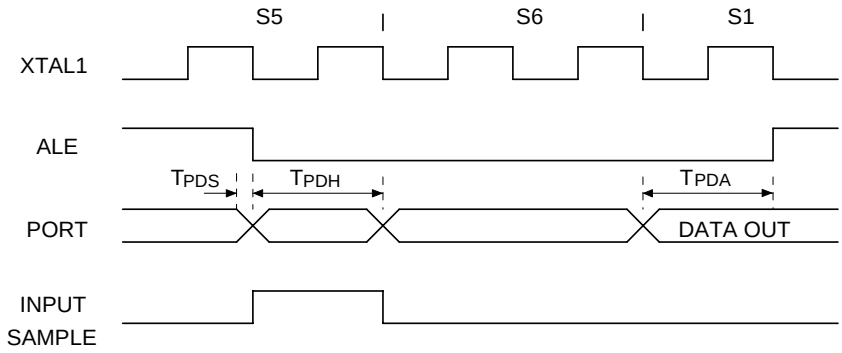
Notes:
1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Timing Waveforms, continued

Data Write Cycle



Port Access Cycle



11. TYPICAL APPLICATION CIRCUIT

Expanded External Program Memory and Crystal

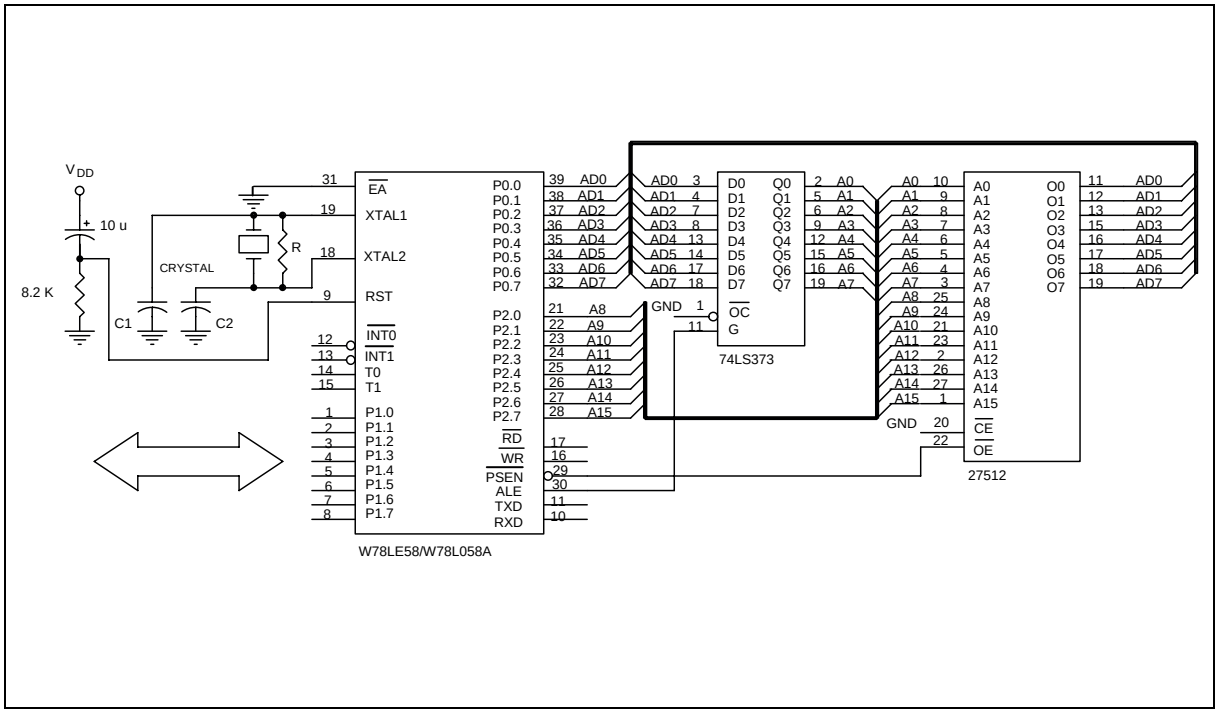


Figure A

CRYSTAL	C1	C2	R
6 MHz	47P	47P	-
16 MHz	30P	30P	-
20 MHz	15P	10P	-

Above table shows the reference values for crystal applications.

Notes:

1. C1, C2, R components refer to Figure A
2. Crystal layout must get close to XTAL1 and XTAL2 pins on user's application board.

Typical Application Circuit, continued

11.1 Expanded External Data Memory and Oscillator

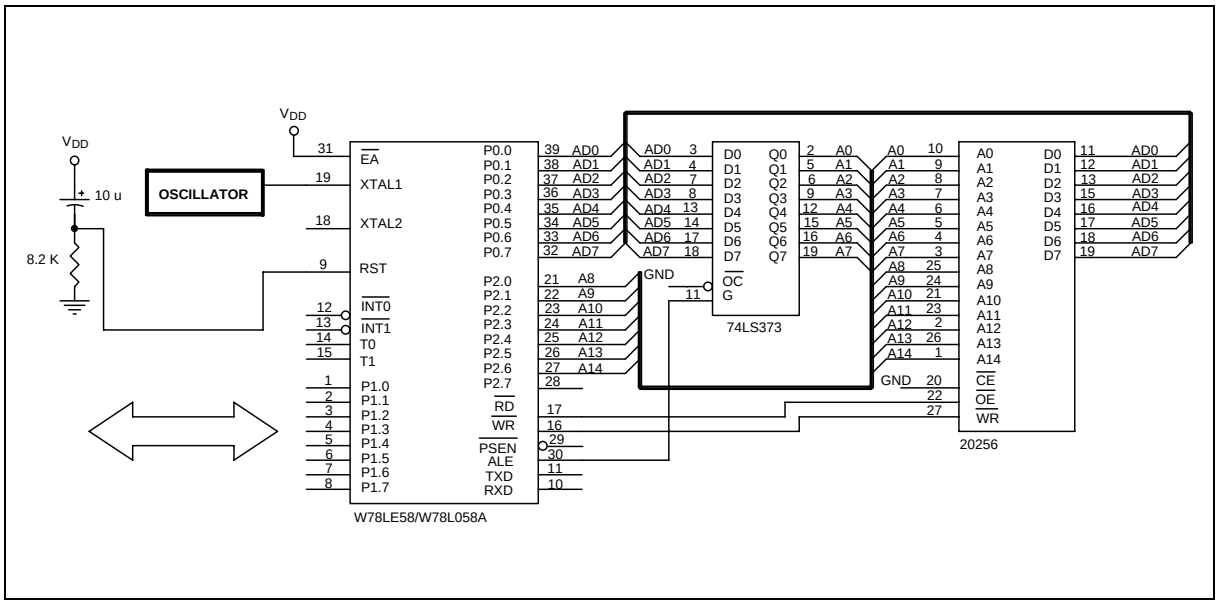
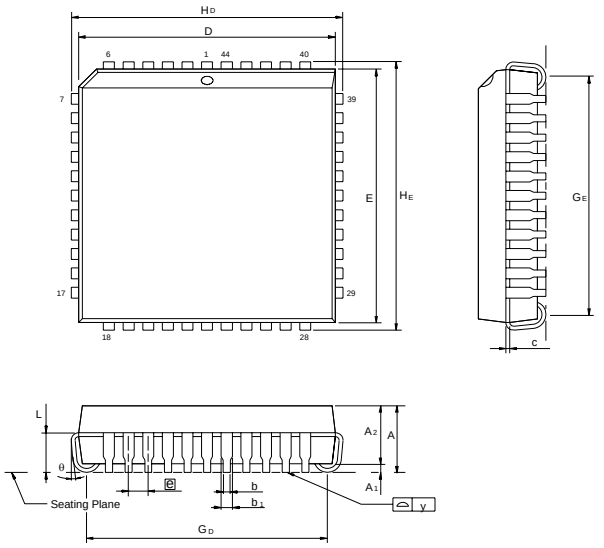


Figure B

Package Dimensions, continued

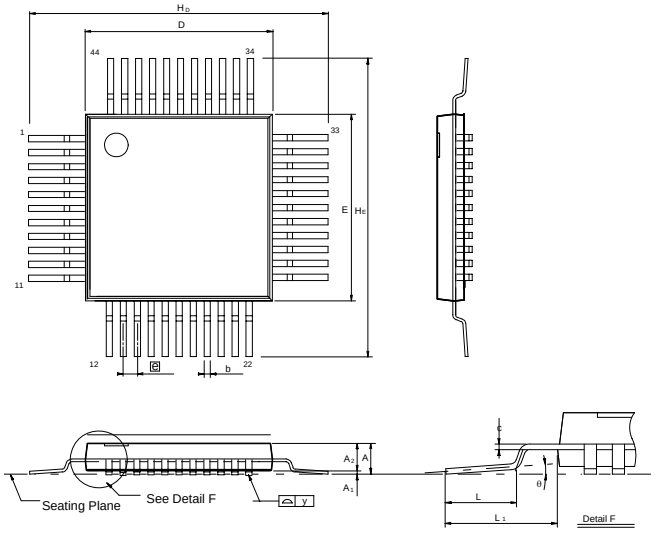
44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

44-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

```
MAIN_4K:
        MOV SP,#C0H
        MOV CHPENR,#87H    ; CHPENR = 87H, CHPCON WRITE ENABLE.
        MOV CHPENR,#59H    ; CHPENR = 59H, CHPCON WRITE ENABLE.
         MOV A,CHPCON
        ANL A,#80H
        CJNE A,#80H,UPDATE_32K ; CHECK  F04KBOOT MODE ?

        MOV CHPCON,#03H   ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV CHPENR,#00H    ; DISABLE CHPCON WRITE ATTRIBUTE

        MOV TCON,#00H       ; TCON = 00H, TR = 0 TIMER0 STOP
         MOV TMOD,#01H      ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV IP,#00H         ; IP = 00H
        MOV IE,#82H         ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV R6,#F0H
       MOV R7,#FFH
        MOV TL0,R6
        MOV TH0,R7
        MOV TCON,#10H       ; TCON = 10H, TR0 = 1, GO
        MOV PCON,#01H       ; ENTER IDLE MODE

 UPDATE_32K:
        MOV CHPENR,#00H   ; DISABLE CHPCON WRITE-ATTRIBUTE
        MOV TCON,#00H       ; TCON = 00H , TR = 0 TIM0 STOP
        MOV IP,#00H         ; IP = 00H
        MOV IE,#82H         ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV TMOD,#01H         ; TMOD = 01H, MODE1
        MOV R6,#E0H         ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 mS. DEPENDING
                            ; ON USER'S SYSTEM CLOCK RATE.
        MOV R7,#B1H
        MOV TL0,R6
        MOV TH0,R7

ERASE_P_4K:
        MOV SFRCN,#22H      ; SFRCN(C7H) = 22H  ERASE 32K
        MOV TCON,#10H       ; TCON = 10H, TR0 = 1,GO
        MOV PCON,#01H       ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV SFRCN,#0H       ; READ 32KB APROM MODE
        MOV SFRAH,#0H       ; START ADDRESS = 0H
        MOV SFRAL,#0H
         MOV R6,#FEH        ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
        MOV R7,#FFH
        MOV TL0,R6
        MOV TH0,R7

BLANK_CHECK_LOOP:
        SETB TR0            ; ENABLE TIMER 0
        MOV PCON,#01H       ; ENTER IDLE MODE
        MOV A,SFRFD         ; READ ONE BYTE
        CJNE A,#FFH,BLANK_CHECK_ERROR
```

```
        INC SFRAL               ; NEXT ADDRESS
        MOV A,SFRAL
        JNZ BLANK_CHECK_LOOP
        INC SFRAH
        MOV A,SFRAH
        CJNE A,#80H,BLANK_CHECK_LOOP   ; END ADDRESS = 7FFFH
        JMP PROGRAM_32KROM

BLANK_CHECK_ERROR:
        MOV P1,#F0H
        MOV P3,#F0H
        JMP $

;*******************************************************************************
;* RE-PROGRAMMING 32KB APROM BANK
;*******************************************************************************
PROGRAM_32KROM:
        MOV DPTR,#0H            ; THE ADDRESS OF NEW ROM CODE
        MOV R2,#00H             ; TARGET LOW BYTE ADDRESS
        MOV R1,#00H             ; TARGET HIGH BYTE ADDRESS
        MOV DPTR,#0H            ; EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH,R1              ; SFRAH, TARGET  HIGH ADDRESS
        MOV SFRCN,#21H          ; SFRCN(C7H) = 21 (PROGRAM 32K)
        MOV R6,#BEH             ; SET TIMER FOR PROGRAMMING, ABOUT 50 μS.
        MOV R7,#FFH
        MOV TL0,R6
        MOV TH0,R7

PROG_D_32K:
        MOV SFRAL,R2            ; SFRAL(C4H) = LOW BYTE ADDRESS
        MOVX A,@DPTR            ; READ DATA FROM EXTERNAL SRAM BUFFER. BY ACCORDING USER?
                                ; CIRCUIT, USER MUST MODIFY THIS INSTRUCTION TO FETCH CODE
        MOV SFRFD,A             ; SFRFD(C6H) = DATA IN
        MOV TCON,#10H           ; TCON = 10H, TR0 = 1,GO
        MOV PCON,#01H           ; ENTER IDLE MODE (PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2,#0H,PROG_D_32K
        INC  R1
        MOV SFRAH,R1
        CJNE R1,#80H,PROG_D_32K

;*******************************************************************************
; * VERIFY 32KB APROM BANK
;*******************************************************************************
        MOV R4,#03H             ; ERROR COUNTER
        MOV R6,#FEH             ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.
        MOV R7,#FFH
        MOV TL0,R6
        MOV TH0,R7
        MOV DPTR,#0H            ; The start address of sample code
        MOV R2,#0H              ; Target  low byte address
        MOV R1,#0H              ; Target  high byte address
        MOV SFRAH,R1            ; SFRAH, Target high address
        MOV SFRCN,#00H          ; SFRCN = 00 (Read ROM CODE)
```