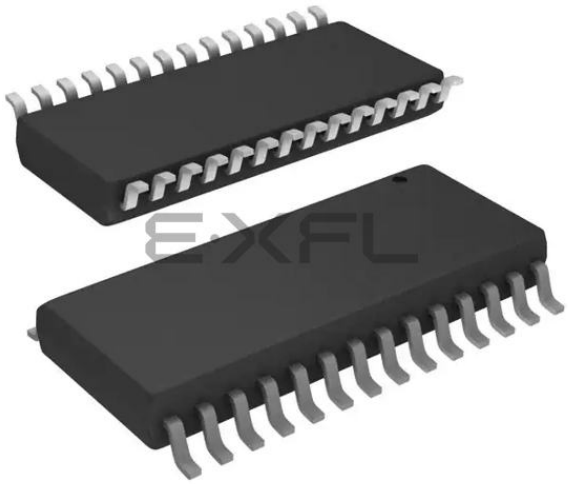
Microchip Technology - PIC16LF1566-I/SO Datasheet



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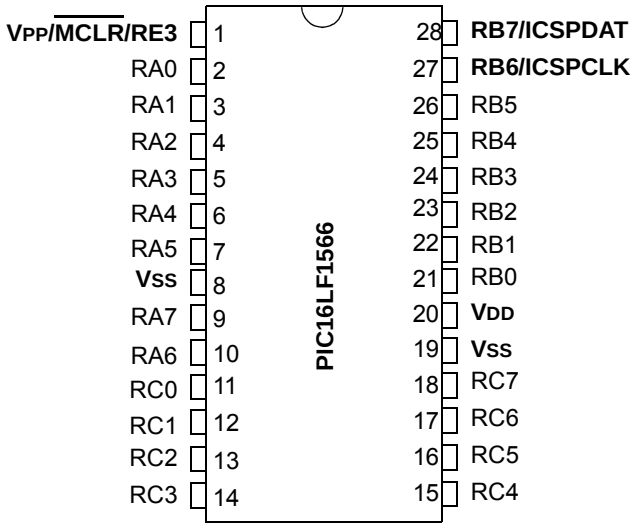
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 23x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1566-i-so

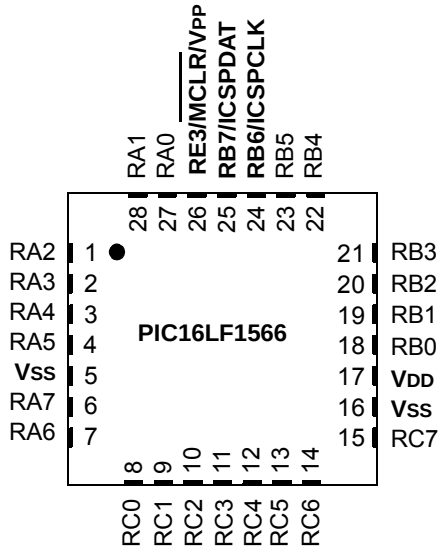
PIN DIAGRAMS

FIGURE 1: 28-PIN SPDIP, SOIC, SSOP DIAGRAM FOR PIC16LF1566



Note: See Table 2 for the pin allocation tables.

FIGURE 2: 28-PIN UQFN DIAGRAM FOR PIC16LF1566



Note: See Table 2 or the pin allocation tables.

TABLE 1-3: PIC16LF1567 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN20/PWM10/SS1(1)	RA0	TTL	CMOS	General Purpose I/O.
	AN20	AN	—	ADC Channel Input for ADC2.
	PWM10	—	CMOS	PWM Output for PWM1.
	SS1	ST	—	Slave Select Input for MSSP1.
RA1/AN10/PWM11/SS2	RA1	TTL	CMOS	General Purpose I/O.
	AN10	AN	—	ADC Channel Input for ADC1.
	PWM11	—	CMOS	PWM Output for PWM1.
	SS2	ST	—	Slave Select Input for MSSP2.
RA2/AN0/PWM12	RA2	TTL	CMOS	General Purpose I/O.
	AN0	AN	—	ADC Channel Input for both ADC1 and ADC2.
	V_{REF-}	AN	—	ADC Negative Voltage Reference Input
	PWM12	—	CMOS	PWM Output for PWM1.
RA3/AN1/V_{REF+}/PWM13	RA3	TTL	CMOS	General Purpose I/O.
	AN1	AN	—	ADC Channel Input for both ADC1 and ADC2.
	V_{REF+}	AN	—	ADC Positive Voltage Reference Input.
	PWM13	—	CMOS	PWM Output for PWM1.
RA4/AN2/T0CKI	RA4	TTL	CMOS	General Purpose I/O.
	AN2	AN	—	ADC Channel Input for both ADC1 and ADC2.
	T0CKI	ST	—	Timer0 Clock Input.
RA5/AN21/SS1(1)	RA5	TTL	CMOS	General Purpose I/O.
	AN21	AN	—	ADC Channel Input for ADC2.
	SS1	ST	—	Slave Select Input for MSSP1.
RA6/AN22/ADTRIG/CLKOUT	RA6	TTL	CMOS	General Purpose I/O.
	AN22	AN	—	ADC Channel Input for ADC2.
	ADTRIG	ST	—	ADC Conversion Trigger Input.
	CLKOUT	—	CMOS	F_{OSC}/4 Output.
RA7/AN11/CLKIN	RA7	TTL	CMOS	General Purpose I/O.
	AN11	AN	—	ADC Channel Input for ADC1.
	CLKIN	CMOS	—	External Clock Input (EC mode).
RB0/AN16/PWM20/INT	RB0	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN16	AN	—	ADC Channel Input for ADC1.
	PWM20	—	CMOS	PWM Output for PWM2.
	INT	ST	—	External Interrupt.
RB1/AN27/PWM21	RB1	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN27	AN	—	ADC Channel Input for ADC2.
	PWM21	—	CMOS	PWM Output for PWM2.
RB2/AN17/PWM22	RB2	TTL	CMOS	General Purpose I/O with IOC and WPU.
	AN17	AN	—	ADC Channel Input for ADC1.
	PWM22	—	CMOS	PWM Output for PWM2.

FIGURE 3-2: BANKED MEMORY PARTITIONING

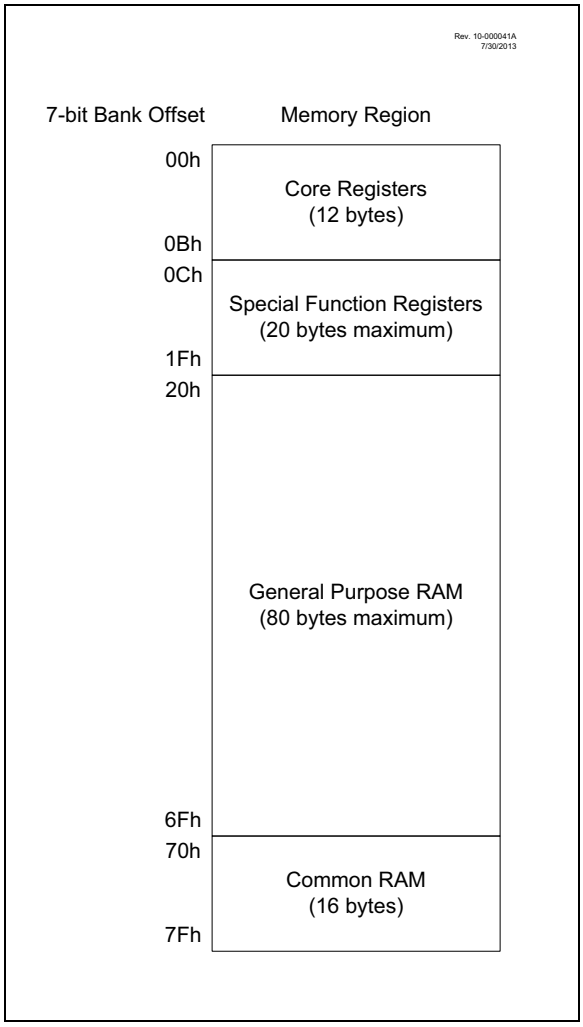


TABLE 3-4: PIC16LF1567 MEMORY MAP, BANKS 0-7

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7
000h	CPU Core Register, see Table 3-2 for specifics														
001h															
002h															
003h															
004h															
005h															
006h															
007h															
008h															
009h															
00Ah															
00Bh															
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch		28Ch	—	30Ch	—	38Ch	—
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	—	30Dh	—	38Dh	—
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	—	28Eh	—	30Eh	—	38Eh	—
00Fh	PORTD	08Fh	TRISD	10Fh	LATD	18Fh	ANSELD	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	PORTE	090h	TRISE	110h	LATE	190h	ANSELE	210h	WPUE	290h	—	310h	—	390h	—
011h	PIR1	091h	PIE1	111h	—	191h	PMADRL	211h	SSP1BUF	291h	—	311h	—	391h	—
012h	PIR2	092h	PIE2	112h	—	192h	PMADRH	212h	SSP1ADD	292h	—	312h	—	392h	—
013h	—	093h	—	113h	—	193h	PMDATL	213h	SSP1MSK	293h	—	313h	—	393h	—
014h	—	094h	—	114h	—	194h	PMDATH	214h	SSP1STAT	294h	—	314h	—	394h	IOCBP
015h	TMR0	095h	OPTION_REG	115h	—	195h	PMCON1	215h	SSP1CON1	295h	—	315h	—	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	SSP1CON2	296h	—	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	—	217h	SSP1CON3	297h	—	317h	—	397h	—
018h	T1CON	098h	—	118h	—	198h	—	218h	SSPLVL	298h	—	318h	—	398h	—
019h	T1GCON	099h	OSCCON	119h	—	199h	RCREG	219h	SSP2BUF	299h	—	319h	—	399h	—
01Ah	TMR2	09Ah	OSCSTAT	11Ah	—	19Ah	TXREG	21Ah	SSP2ADD	29Ah	—	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	—	19Bh	SPBRGL	21Bh	SSP2MSK	29Bh	—	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	—	19Ch	SPBRGH	21Ch	SSP2STAT	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	APFCON	19Dh	RCSTA	21Dh	SSP2CON1	29Dh	—	31Dh	—	39Dh	—
01Eh	—	09Eh	ADCON1	11Eh	—	19Eh	TXSTA	21Eh	SSP2CON2	29Eh	—	31Eh	—	39Eh	—
01Fh	—	09Fh	ADCON2	11Fh	—	19Fh	BAUDCON	21Fh	SSP2CON3	29Fh	—	31Fh	—	39Fh	—
020h	General Purpose Register 96 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes	220h	General Purpose Register 80 Bytes	2A0h	General Purpose Register 80 Bytes	320h	General Purpose Register 80 Bytes	3A0h	General Purpose Register 80 Bytes
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		36Fh		3EFh	
070h		0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	370h	Accesses 70h – 7Fh	3F0h	Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: These ADC registers are the same as the registers in Bank 14.

TABLE 3-11: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 15											
780h	INDF0(1)	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
781h	INDF1(1)	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
782h	PCL(1)	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
783h	STATUS(1)	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
784h	FSR0L(1)	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
785h	FSR0H(1)	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
786h	FSR1L(1)	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
787h	FSR1H(1)	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
788h	BSR(1)	—	—	—	BSR<4:0>					---0 0000	---0 0000
789h	WREG(1)	Working Register								0000 0000	uuuu uuuu
78Ah	PCLATH(1)	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
78Bh	INTCON(1)	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 000u
78Ch	—	Unimplemented								—	—
78Dh	—	Unimplemented								—	—
78Eh	—	Unimplemented								—	—
78Fh	—	Unimplemented								—	—
790h	—	Unimplemented								—	—
791h	AD2CON0	CHS<5:0>						GO/$\overline{DONE}$2	AD2CON	0000 0000	0000 0000
792h	—	Unimplemented								—	—
793h	AD2CON2	—	TRIGSEL<2:0>			—	—	—	—	-000 ----	-000 ----
794h	AD2CON3	AD2EPPOL	AD2IPPOL	—	—	—	—	AD2IPEN	AD2DSEN	00-- --00	00-- --00
795h	—	Unimplemented								—	—
796h	AD2PRECON	—	ADPRE<6:0>							-000 0000	-000 0000
797h	AD2ACQCON	—	ADACQ<6:0>							-000 0000	-000 0000
798h	AD2GRD	GRD2BOE	GRD2AOE	GRD2POL	—	—	—	—	TX2POL	000- ---x	000- ---u
799h	AD2CAPCON	—	—	—	—	ADD2CAP<3:0>				---- 0000	---- 0000
79Ah	AAD2RES0L	ADRESL								xxxx xxxx	uuuu uuuu
79Bh	AAD2RES0H	ADRESH								xxxx xxxx	uuuu uuuu
79Ch	AAD2RES1L	ADRESL								xxxx xxxx	uuuu uuuu
79Dh	AAD2RES1H	ADRESH								xxxx xxxx	uuuu uuuu
79Eh	AD2CH0	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	0000 0000	0000 0000
79Fh	AD2CH1	—	—	—	—	—	CH40	CH29	CH28	-----000	-----000
	AD2CH1(2)	CH45	CH44	CH43	CH42	CH41	CH40	CH29	CH28	00000000	00000000

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: These registers can be accessed from any bank.
2: PIC16LF1567.
3: These registers/bits are available at two address locations, in Bank 1 and Bank 14.
4: PIC16LF1566 only.
5: Unimplemented, read as '1'.

FIGURE 3-5: ACCESSING THE STACK EXAMPLE 2

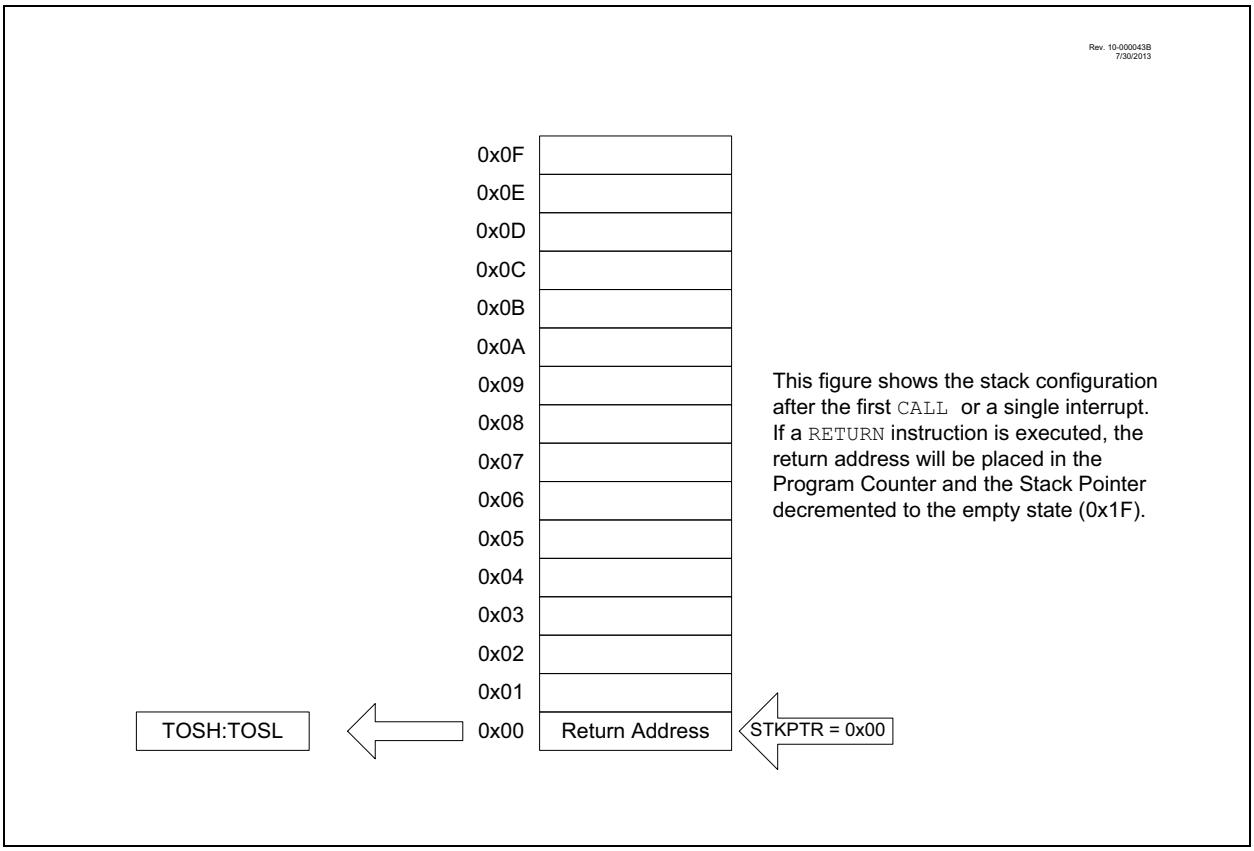
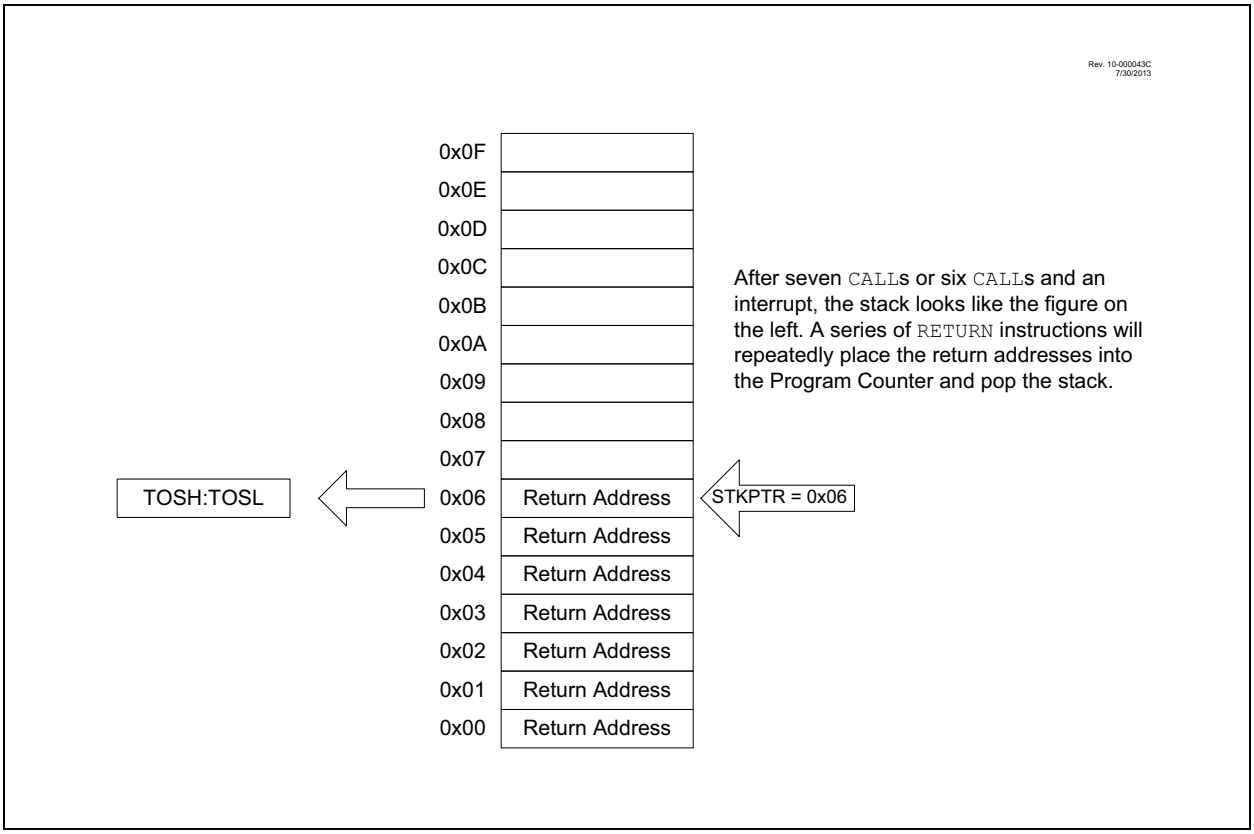


FIGURE 3-6: ACCESSING THE STACK EXAMPLE 3



5.0 OSCILLATOR MODULE

5.1 Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 5-1 illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external clock oscillators. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal sources via software.

The oscillator module can be configured in one of the following clock modes.

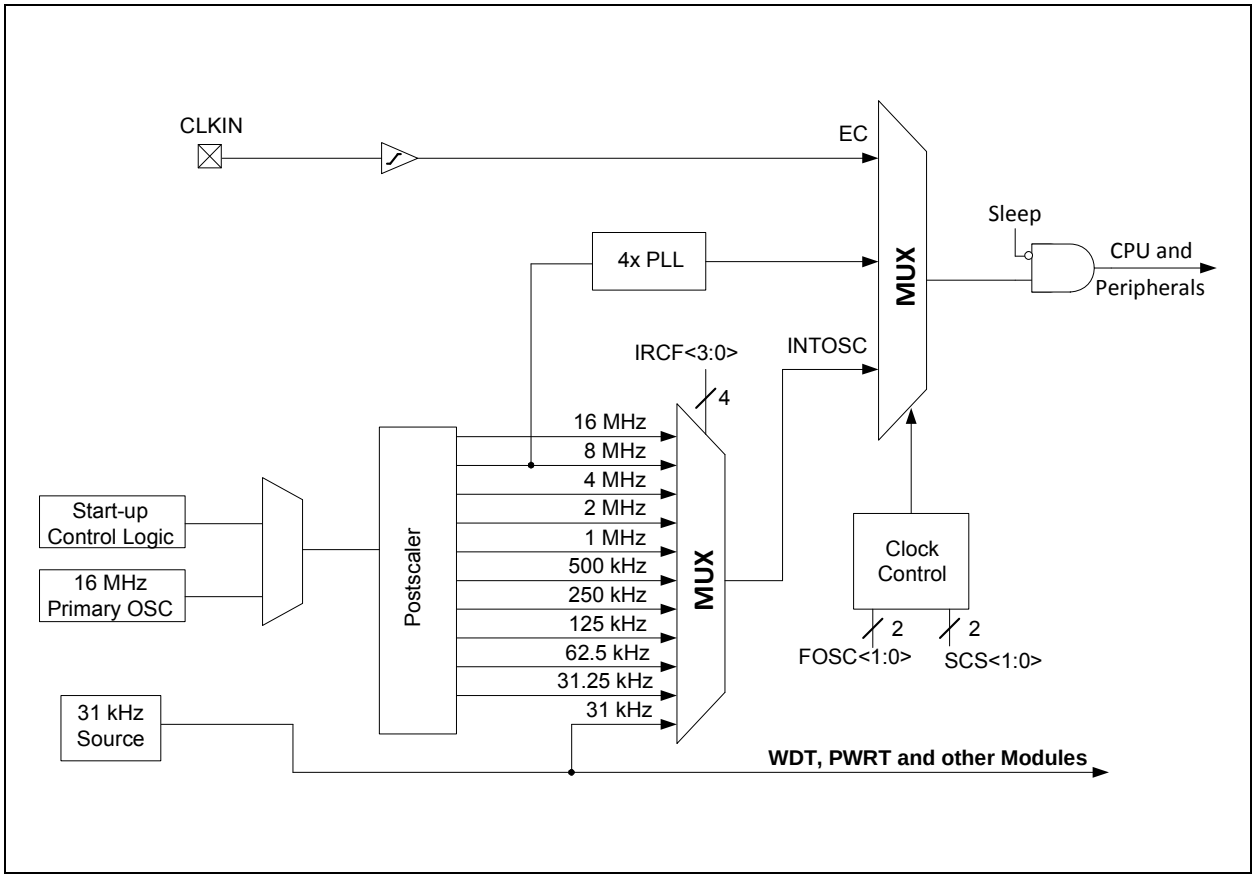
1. ECL – External Clock Low-Power mode (0 MHz to 0.5 MHz)
2. ECM – External Clock Medium Power mode (0.5 MHz to 4 MHz)
3. ECH – External Clock High-Power mode (4 MHz to 20 MHz)
4. INTOSC – Internal oscillator (31 kHz to 32 MHz)

Clock source modes are selected by the FOSC<1:0> bits in the Configuration Words. The FOSC bits determine the type of oscillator that will be used when the device is first powered.

The EC clock mode relies on an external logic level signal as the device clock source.

The INTOSC internal oscillator block produces low and high-frequency clock sources, designated LFINTOSC and HFINTOSC (see Internal Oscillator Block, Figure 5-1). A wide selection of device clock frequencies may be derived from these clock sources.

FIGURE 5-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



5.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bits of the OSCCON register. The following clock sources can be selected using the SCS bits:

- Default system oscillator determined by FOSC bits in Configuration Words
- Internal Oscillator Block (INTOSC)

5.3.1 SYSTEM CLOCK SELECT (SCS) BITS

The System Clock Select (SCS) bits of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bits of the OSCCON register = `00`, the system clock source is determined by value of the FOSC<1:0> bits in the Configuration Words.
- When the SCS bits of the OSCCON register = `1x`, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<3:0> bits of the OSCCON register. After a Reset, the SCS bits of the OSCCON register are always cleared.

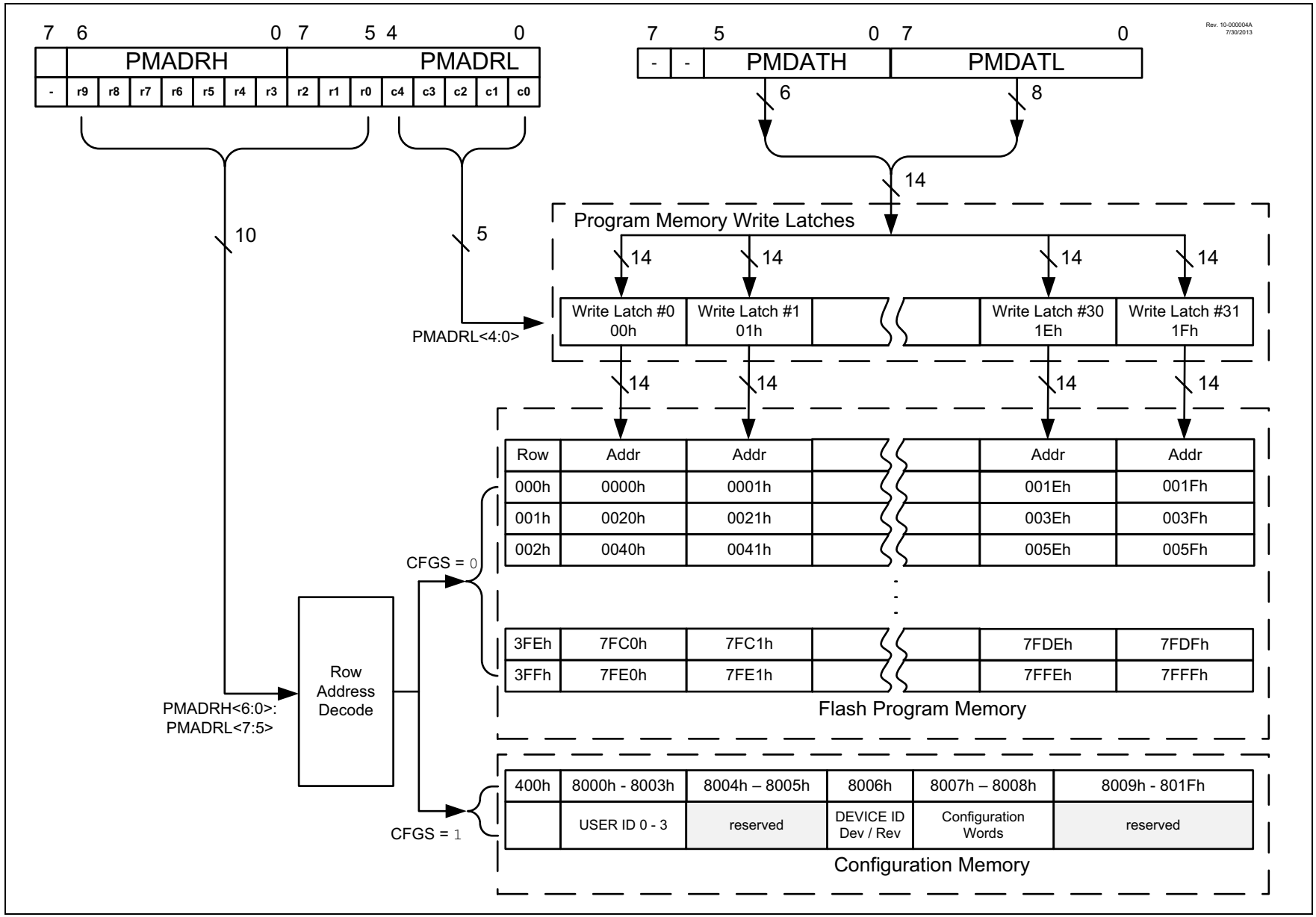
When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 5-1.

TABLE 5-1: OSCILLATOR SWITCHING DELAYS

Switch From	Switch To	Frequency	Oscillator Delay
Sleep	LFINTOSC(1) MFINTOSC(1) HFINTOSC(1)	31 kHz 31.25 kHz-500 kHz 31.25 kHz-16 MHz	Oscillator Warm-Up Delay TWARM(2)
Sleep/POR	EC(1)	DC – 32 MHz	2 cycles
LFINTOSC	EC(1)	DC – 32 MHz	1 cycle of each
Any clock source	MFINTOSC(1) HFINTOSC	31.25 kHz-500 MHz 31.25 kHz-16 MHz	2 μs (approx.)
Any clock source	LFINTOSC	31 kHz	1 cycle of each
PLL inactive	PLL active	16-32 MHz	2 ms (approx.)

Note 1: PLL inactive
2: See **Section 25.0 “Electrical Specifications”**

FIGURE 10-5: BLOCK WRITES TO FLASH PROGRAM MEMORY WITH 32 WRITE LATCHES



15.4 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 15-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 15-4. **The maximum recommended impedance for analog sources is 10 kΩ.**

As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an ADC acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 15-1 may be used. This equation assumes that 1/2 LSb error is used (1,024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 15-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10 kΩ 3.3V VDD

$$TACQ = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= TAMP + TC + TCOFF$$
$$= 2\ \mu s + TC + [(\text{Temperature} - 25°C)(0.05\ \mu s/°C)]$$

The value for TC can be approximated with the following equations:

$$VAPPLIED\left(1 - \frac{1}{(2^{n+1}) - 1}\right) = VCHOLD \quad ;[1]\ V_{CHOLD}\ \text{charged to within 1/2 lsb}$$

$$VAPPLIED\left(1 - e^{\frac{-TC}{RC}}\right) = VCHOLD \quad ;[2]\ V_{CHOLD}\ \text{charge response to}\ V_{APPLIED}$$

$$VAPPLIED\left(1 - e^{\frac{-TC}{RC}}\right) = VAPPLIED\left(1 - \frac{1}{(2^{n+1}) - 1}\right) \quad ;\text{combining [1] and [2]}$$

Note: Where n = number of bits of the ADC.

Solving for TC:

$$TC = -CHOLD(RIC + RSS + RS)\ ln(1/2047)$$
$$= -15\ pF(1k\Omega + 7k\Omega + 10k\Omega)\ ln(0.0004885)$$
$$= 2.06\ \mu s$$

Therefore: $TACQ = 2\mu s + 2.06\mu s + [(50°C - 25°C)(0.05\mu s/°C)]$
$= 5.31\ \mu s$

Note 1: The reference voltage (VRPOS) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

4: The calculation above assumed CHOLD = 15pF. This value can be larger than 15pF by setting the AADxCAP register.

REGISTER 16-7: ADxCON2: ADC CONTROL REGISTER 2(1)

U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
—	TRIGSEL<2:0>			—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **TRIGSEL<2:0>:** Auto-Conversion Trigger Selection bits
- 111 = ADTRIG Falling Edge
- 110 = ADTRIG Rising Edge
- 101 = TMR2 match to PR2(1)
- 100 = Timer1 Overflow(1)
- 011 = Timer0 Overflow(1)
- 010 = TMR4 match to PR4
- 001 = Reserved
- 000 = No Auto Conversion Trigger selected

bit 3-0 **Unimplemented:** Read as '0'

Note 1: Signal also sets its corresponding interrupt flag.

FIGURE 18-5: TIMER1 GATE SINGLE-PULSE MODE

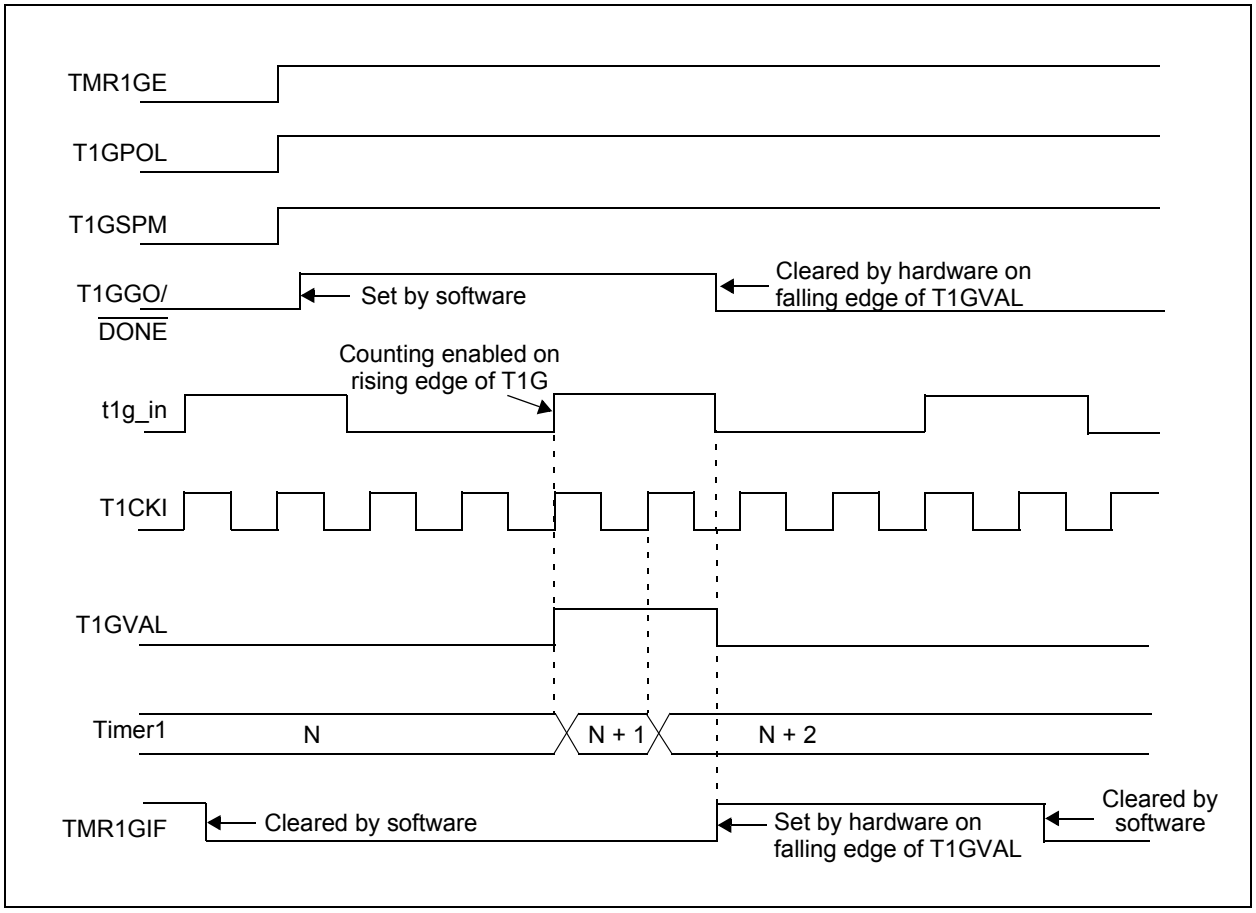
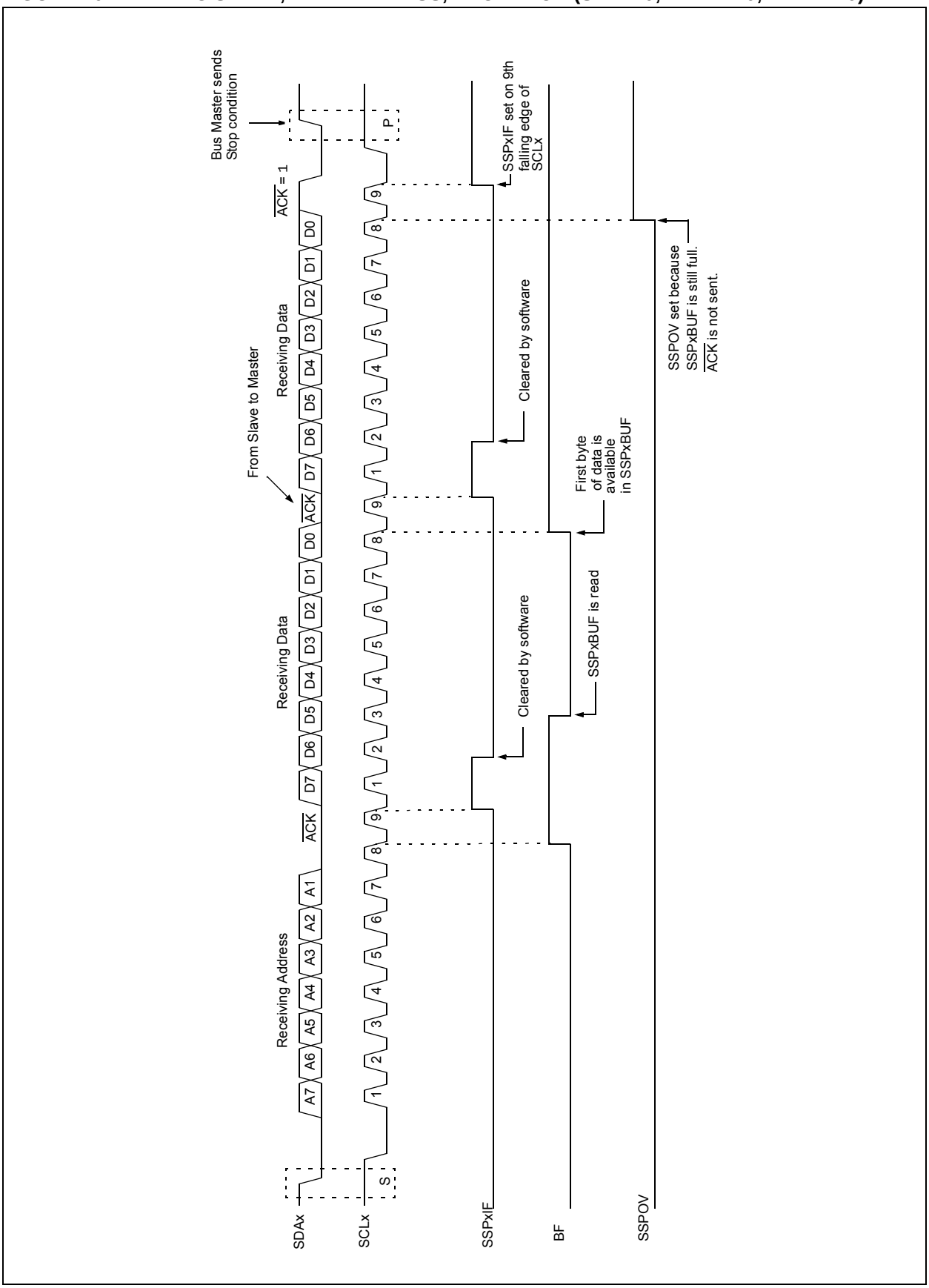


FIGURE 20-14: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 0, DHEN = 0)



REGISTER 21-3: BAUDCON: BAUD RATE CONTROL REGISTER

R-0/0	R-1/1	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0
ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ABDOVF:** Auto-Baud Detect Overflow bit
Asynchronous mode:
1 = Auto-baud timer overflowed
0 = Auto-baud timer did not overflow
Synchronous mode:
Don't care

bit 6 **RCIDL**: Receive Idle Flag bit
Asynchronous mode:
1 = Receiver is idle
0 = Start bit has been received and the receiver is receiving
Synchronous mode:
Don't care

bit 5 **Unimplemented:** Read as '0'

bit 4 **SCKP**: Synchronous Clock Polarity Select bit
Asynchronous mode:
1 = Transmit inverted data to the TX/CK pin
0 = Transmit non-inverted data to the TX/CK pin
Synchronous mode:
1 = Data is clocked on rising edge of the clock
0 = Data is clocked on falling edge of the clock

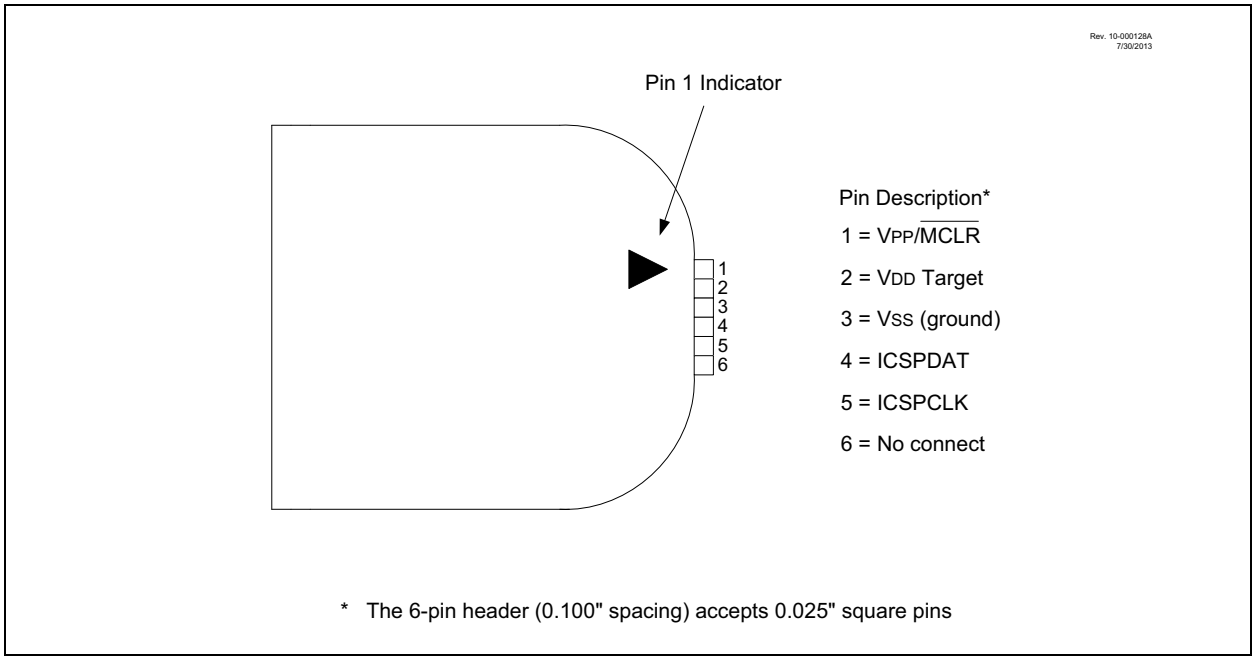
bit 3 **BRG16:** 16-bit Baud Rate Generator bit
1 = 16-bit Baud Rate Generator is used
0 = 8-bit Baud Rate Generator is used

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = Receiver is waiting for a falling edge. No character will be received, RCIF bit will be set. WUE will automatically clear after RCIF is set.
0 = Receiver is operating normally
Synchronous mode:
Don't care

bit 0 **ABDEN**: Auto-Baud Detect Enable bit
Asynchronous mode:
1 = Auto-Baud Detect mode is enabled (clears when auto-baud is complete)
0 = Auto-Baud Detect mode is disabled
Synchronous mode:
Don't care

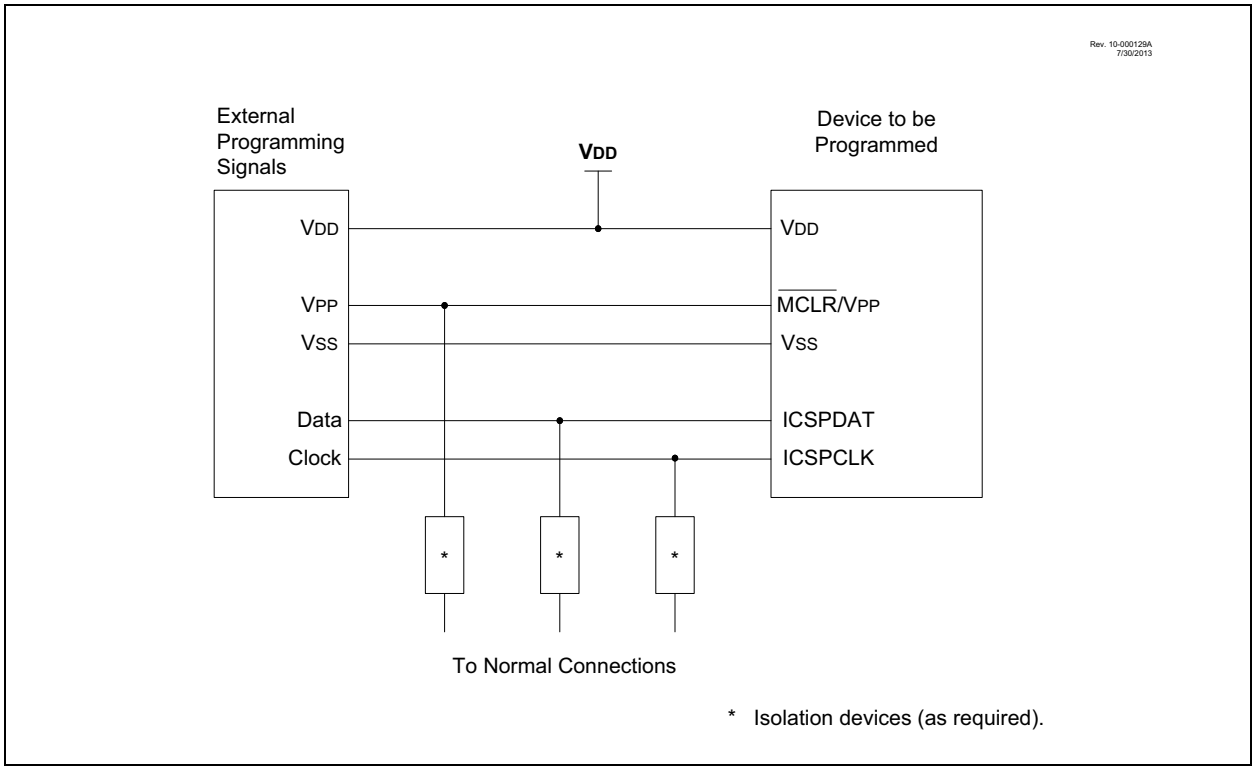
FIGURE 23-2: PICkit™ PROGRAMMER STYLE CONNECTOR INTERFACE



For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 23-3 for more information.

FIGURE 23-3: TYPICAL CONNECTION FOR ICSP™ PROGRAMMING



MOVIW **Move INDFn to W**

Syntax: [*label*] MOVIW ++FSRn
[*label*] MOVIW --FSRn
[*label*] MOVIW FSRn++
[*label*] MOVIW FSRn--
[*label*] MOVIW k[FSRn]

Operands: n ∈ [0,1]
mm ∈ [00,01, 10, 11]
-32 ≤ k ≤ 31

Operation: INDFn → W
Effective address is determined by
- FSR + 1 (preincrement)
- FSR - 1 (predecrement)
- FSR + k (relative offset)

After the Move, the FSR value will be either:
- FSR + 1 (all increments)
- FSR - 1 (all decrements)
- Unchanged

Status Affected: Z

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

Description: This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h - FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.

MOVLB **Move literal to BSR**

Syntax: [*label*] MOVLB k

Operands: 0 ≤ k ≤ 31

Operation: k → BSR

Status Affected: None

Description: The 5-bit literal 'k' is loaded into the Bank Select Register (BSR).

MOVLP **Move literal to PCLATH**

Syntax: [*label*] MOVLP k

Operands: 0 ≤ k ≤ 127

Operation: k → PCLATH

Status Affected: None

Description: The 7-bit literal 'k' is loaded into the PCLATH register.

MOVLW **Move literal to W**

Syntax: [*label*] MOVLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W)

Status Affected: None

Description: The 8-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: 0 ≤ f ≤ 127

Operation: (W) → (f)

Status Affected: None

Description: Move data from W register to register 'f'.

Words: 1

Cycles: 1

Example:
```
MOVWF   OPTION_REG
```
Before Instruction
OPTION_REG = 0xFF
W = 0x4F
After Instruction
OPTION_REG = 0x4F
W = 0x4F

TABLE 25-7: CLOCK OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
OS01	FOSC	External CLKIN Frequency(1)	DC	—	0.5	MHz	EC Oscillator mode (low)
			DC	—	4	MHz	EC Oscillator mode (medium)
			DC	—	20	MHz	EC Oscillator mode (high)
OS02	TOSC	External CLKIN Period(1)	50	—	∞	ns	EC mode
OS03	TCY	Instruction Cycle Time(1)	200	—	DC	ns	TCY = FOSC/4

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to CLKIN pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

TABLE 25-8: OSCILLATOR PARAMETERS

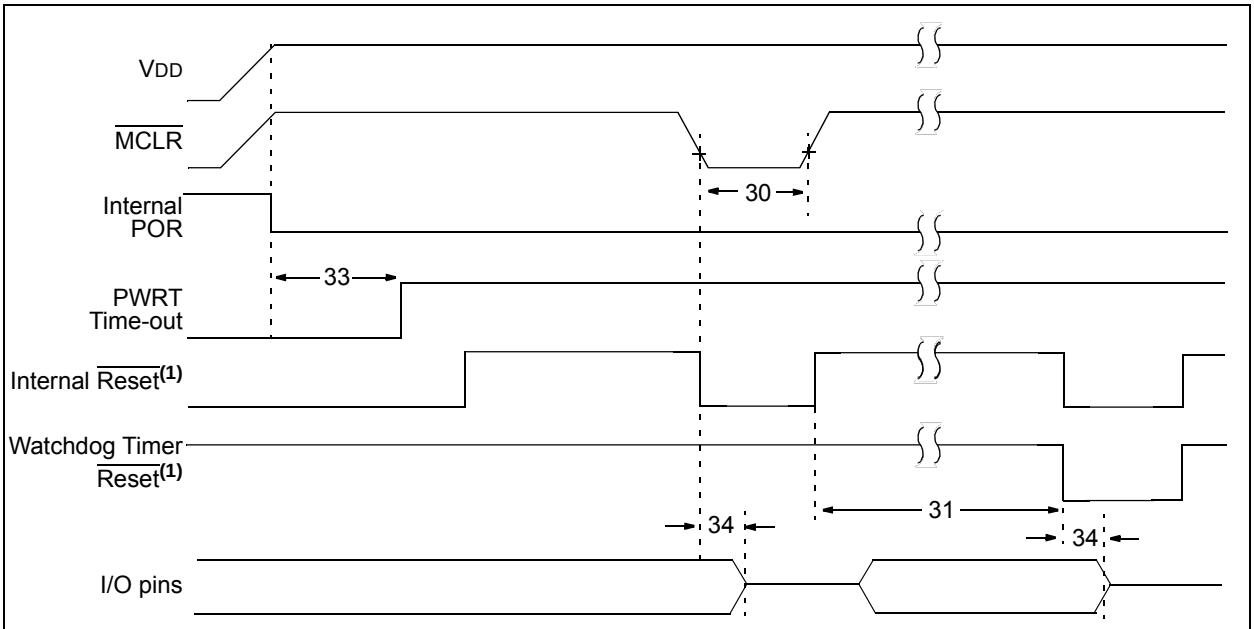
Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(1)	—	16.0	—	MHz	0°C ≤ TA ≤ +85°C
OS08A	HFTOL	Frequency Tolerance	—	±3	—	%	25°C, 16 MHz
			—	±6	—	%	0°C ≤ TA ≤ +85°C, 16 MHz
OS09	LFOSC	Internal LFINTOSC Frequency	—	31	—	kHz	-40°C ≤ TA ≤ +125°C
OS10*	TWARM	HFINTOSC Wake-up from Sleep Start-up Time	—	5	15	µs	
		LFINTOSC Wake-up from Sleep Start-up Time	—	0.5	—	ms	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

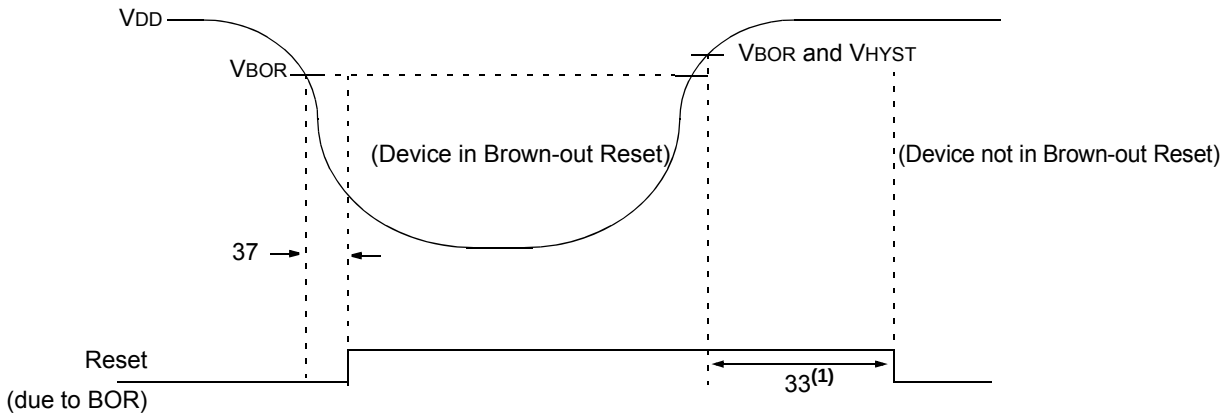
Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

FIGURE 25-6: RESET, WATCHDOG TIMER AND POWER-UP TIMER TIMING



Note 1: Asserted low.

FIGURE 25-7: BROWN-OUT RESET TIMING AND CHARACTERISTICS



Note 1: 64 ms delay only if $\overline{\text{PWRTE}}$ bit in the Configuration Words is programmed to '0'.
2 ms delay if $\overline{\text{PWRTE}}$ = 0.

FIGURE 25-13: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

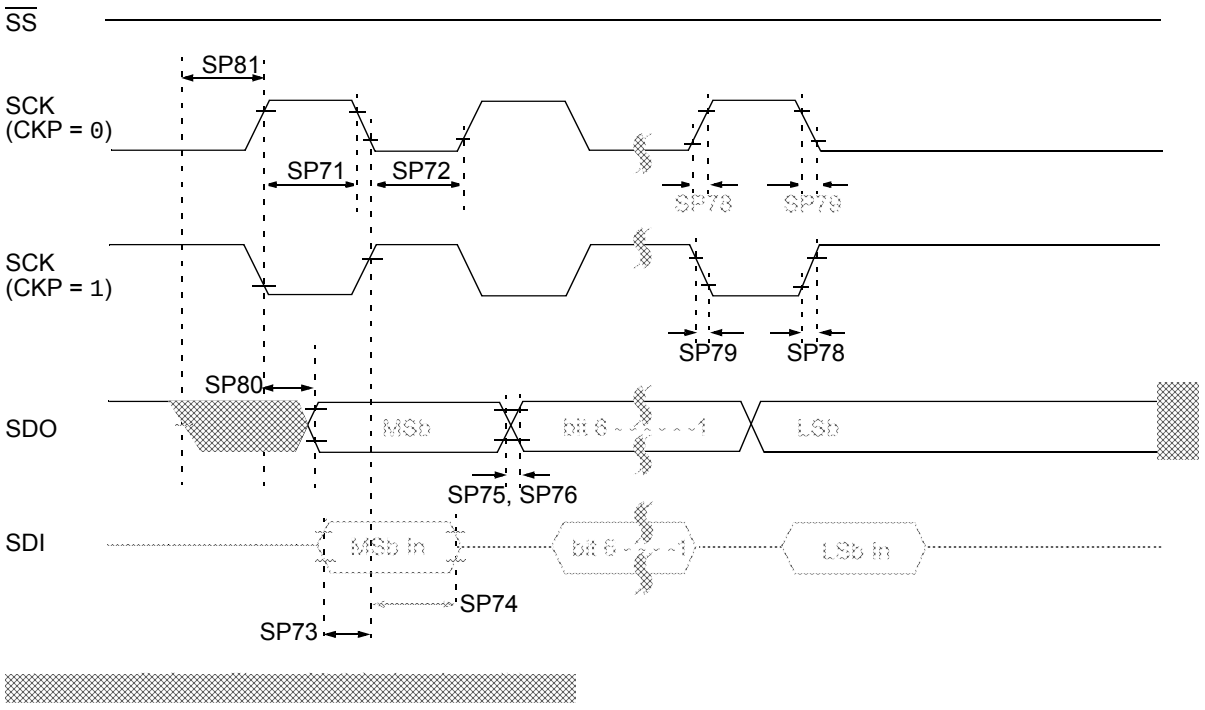
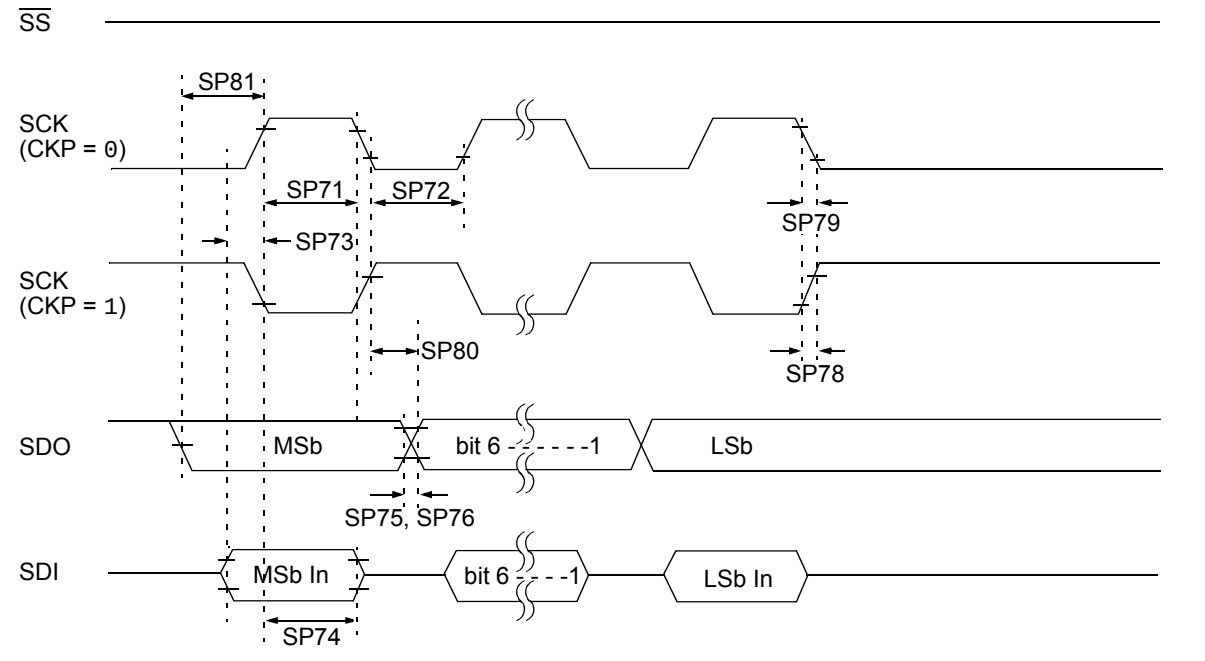


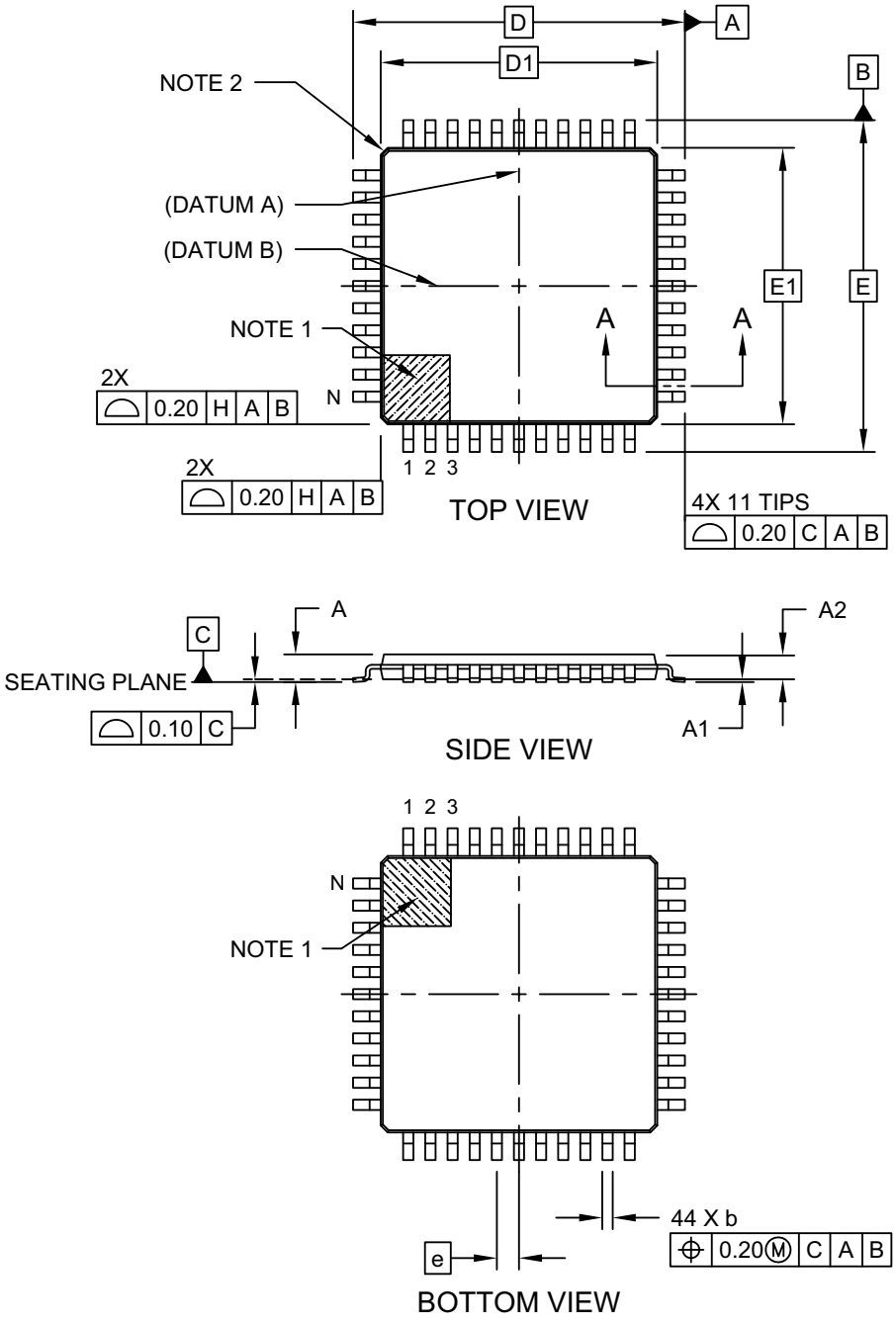
FIGURE 25-14: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 25-3 for Load conditions.

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-076C Sheet 1 of 2