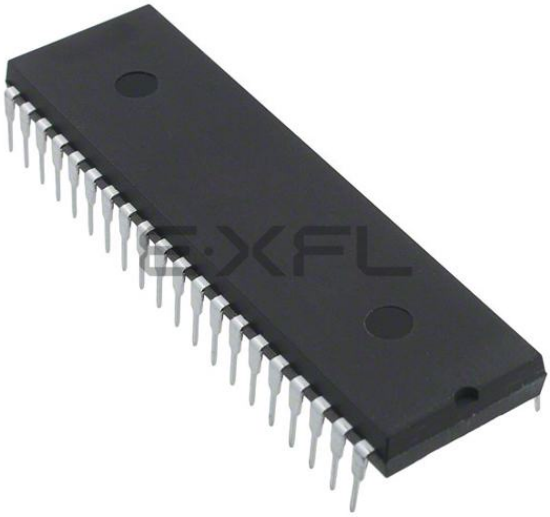


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 34x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1567-e-p

1.0 DEVICE OVERVIEW

The PIC16LF1566/1567 devices are described within this data sheet. The block diagram of these devices is shown in Figure 1-1, the available peripherals are shown in Table 1-1 and the pinout descriptions are shown in Table 1-2 and Table 1-3.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16LF1566	PIC16LF1567
Analog-to-Digital Converter (ADC)			
	ADC1	●	●
	ADC2	●	●
Hardware Capacitive Voltage Divider (CVD)		●	●
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)		●	●
Fixed Voltage Reference (FVR)		●	●
Temperature Indicator		●	●
Master Synchronous Serial Ports			
	MSSP1	●	●
	MSSP2	●	●
PWM Modules			
	PWM1	●	●
	PWM2	●	●
Timers			
	Timer0	●	●
	Timer1	●	●
	Timer2	●	●
	Timer4	●	●

TABLE 3-11: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 12											
600h	INDF0(1)	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
601h	INDF1(1)	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
602h	PCL(1)	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
603h	STATUS(1)	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
604h	FSR0L(1)	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
605h	FSR0H(1)	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
606h	FSR1L(1)	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
607h	FSR1H(1)	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
608h	BSR(1)	—	—	—	BSR<4:0>					---0 0000	---0 0000
609h	WREG(1)	Working Register								0000 0000	uuuu uuuu
60Ah	PCLATH(1)	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
60Bh	INTCON(1)	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
60Ch	—	Unimplemented								—	—
60Dh	—	Unimplemented								—	—
60Eh	—	Unimplemented								—	—
60Fh	—	Unimplemented								—	—
610h	—	Unimplemented								—	—
611h	PWM1DCL	PWM1DCL<7:6>		—	—	—	—	—	—	xx-- ----	uu-- ----
612h	PWM1DCH	PWM1DCH								xxxx xxxx	uuuu uuuu
613h	PWM1CON	PWM1EN	PWM1OE	PWM1OUT	PWM1POL	—	—	—	—	00x0 ----	00x0 ----
614h	PWM2DCL	PWM2DCL<7:6>		—	—	—	—	—	—	xx-- ----	uu-- ----
615h	PWM2DCH	PWM2DCH								xxxx xxxx	uuuu uuuu
616h	PWM2CON	PWM2EN	PWM2OE	PWM2OUT	PWM2POL	—	—	—	—	00x0 ----	0x00 ----
617h	—	Unimplemented								—	—
618h	—	Unimplemented								—	—
619h	—	Unimplemented								—	—
61Ah	—	Unimplemented								—	—
61Bh	—	Unimplemented								—	—
61Ch	—	Unimplemented								—	—
61Dh	PWMTMRS						P2TSEL		P1TSEL	-----0-0	-----0-0
61Eh	PWM1AOE					PWM1OE				----0000	----0000
61Fh	PWM2AOE					PWM2OE				----0000	----0000

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: These registers can be accessed from any bank.
2: PIC16LF1567.
3: These registers/bits are available at two address locations, in Bank 1 and Bank 14.
4: PIC16LF1566 only.
5: Unimplemented, read as '1'.

TABLE 3-11: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 14											
700h	INDF0(1)	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
701h	INDF1(1)	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
702h	PCL(1)	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
703h	STATUS(1)	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
704h	FSR0L(1)	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
705h	FSR0H(1)	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
706h	FSR1L(1)	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
707h	FSR1H(1)	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
708h	BSR(1)	—	—	—	BSR<4:0>					---0 0000	---0 0000
709h	WREG(1)	Working Register								0000 0000	uuuu uuuu
70Ah	PCLATH(1)	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
70Bh	INTCON(1)	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 000u
70Ch	—	Unimplemented								—	—
70Dh	—	Unimplemented								—	—
70Eh	—	Unimplemented								—	—
70Fh	—	Unimplemented								—	—
710h	—	Unimplemented								—	—
711h	AD1CON0	CHS15	CHS14	CHS13	CHS12	CHS11	CHS10	GO/$\overline{DONE}$1	AD1ON	0000 0000	0000 0000
712h	ADCOMCON	ADFM	ADCS<2:0>			ADNREF	GO/$\overline{DONE}$_ALL	ADPREF<1:0>		0000 0000	0000 0000
713h	AD1CON2	—	TRIGSEL<2:0>			—	—	—	—	-000 ----	-000 ----
714h	AD1CON3	AD1EPPOL	AD1IPPOL	—	—	—	—	AD1IPEN	AD1DSEN	00-- --00	00-- --00
715h	ADSTAT	—	AD2CONV	AD2STG<1:0>		—	AD1CONV	AD1STG		-000 -000	-000 -000
716h	AD1PRECON	—	ADPRE<6:0>							-000 0000	-000 0000
717h	AD1ACQCON	—	ADACQ<6:0>							-000 0000	-000 0000
718h	AD1GRD	GRD1BOE	GRD1AOE	GRD1POL	—	—	—	—	TX1POL	000- ---0	000- ---0
719h	AD1CAPCON	—	—	—	—	ADDCAP<3:0>				---- 0000	---- 0000
71Ah	AAD1RES0L	ADRESL								xxxx xxxx	uuuu uuuu
71Bh	AAD1RES0H	ADRESH								xxxx xxxx	uuuu uuuu
71Ch	AAD1RES1L	ADRESL								xxxx xxxx	uuuu uuuu
71Dh	AAD1RES1H	ADRESH								xxxx xxxx	uuuu uuuu
71Eh	AD1CH0	CHS17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	0000 0000	0000 0000
71Fh	AD1CH1	—	—	—	—	—	—	CH19	CH18	------00	------00
	AD1CH1(2)	CH35	CH34	CH33	CH32	CH31	CH30	CH19	CH18	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: These registers can be accessed from any bank.

2: PIC16LF1567.

3: These registers/bits are available at two address locations, in Bank 1 and Bank 14.

4: PIC16LF1566 only.

5: Unimplemented, read as '1'.

5.2.2.3 Internal Oscillator Frequency Selection

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register.

The outputs of the 16 MHz HFINTOSC postscaler and the LFINTOSC connect to a multiplexer (see Figure 5-1). The Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register select the frequency. One of the following frequencies can be selected via software:

- 32 MHz (requires 4x PLL)
- 16 MHz
- 8 MHz
- 4 MHz
- 2 MHz
- 1 MHz
- 500 kHz (default after Reset)
- 250 kHz
- 125 kHz
- 62.5 kHz
- 31.25 kHz
- 31 kHz (LFINTOSC)

Note:	Following any Reset, the IRCF<3:0> bits of the OSCCON register are set to '0111' and the frequency selection is set to 500 kHz. The user can modify the IRCF bits to select a different frequency.

The IRCF<3:0> bits of the OSCCON register allow duplicate selections for some frequencies. These duplicate choices can offer system design trade-offs. Lower power consumption can be obtained when changing oscillator sources for a given frequency. Faster transition times can be obtained between frequency changes that use the same oscillator source.

5.2.2.4 Internal Oscillator Clock Switch Timing

When switching between the HFINTOSC and the LFINTOSC, the new oscillator may already be shut down to save power (see Figure 5-3). If this is the case, there is a delay after the IRCF<3:0> bits of the OSCCON register are modified before the frequency selection takes place. The OSCSTAT register will reflect the current active status of the HFINTOSC and LFINTOSC oscillators. The sequence of a frequency selection is as follows:

1. IRCF<3:0> bits of the OSCCON register are modified.
2. If the new clock is shut down, a clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. Clock switch is complete.

See Figure 5-3 for more details.

If the internal oscillator speed is switched between two clocks of the same source, there is no start-up delay before the new frequency is selected.

Start-up delay specifications are located in the oscillator tables of **Section 25.0 "Electrical Specifications"**.

5.2.2.5 32 MHz Internal Oscillator Frequency Selection

The Internal Oscillator Block can be used with the 4x PLL to produce a 32 MHz internal system clock source. The following settings are required to use the 32 MHz internal clock source:

- The FOSC bits in Configuration Word 1 must be set to use the INTOSC source as the device system clock (FOSC<1:0> = 00).
- The SCS bits in the OSCCON register must be cleared to use the clock determined by FOSC<1:0> in Configuration Word 1 (SCS<1:0> = 00).
- The IRCF bits in the OSCCON register must be set to the 8 MHz HFINTOSC set to use (IRCF<3:0> = 1110).
- The SPLLEN bit in the OSCCON register must be set to enable the 4x PLL.

The 4x PLL is not available for use with the internal oscillator when the SCS bits of the OSCCON register are set to '1x'. The SCS bits must be set to '00' to use the 4x PLL with the internal oscillator.

7.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

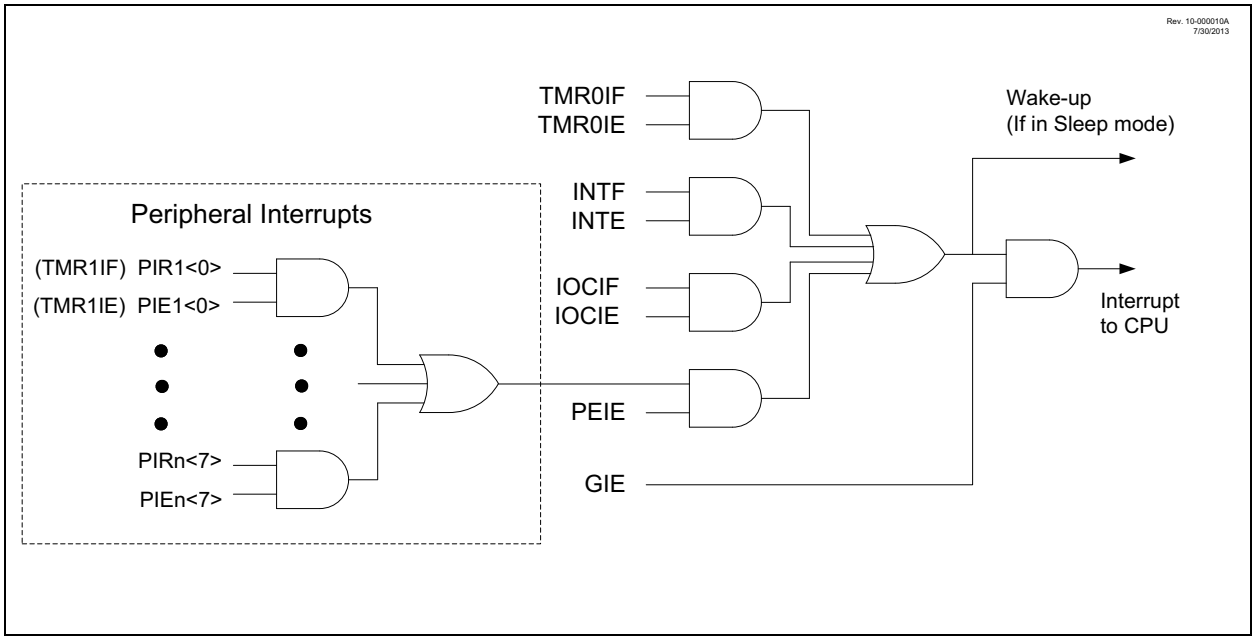
This chapter contains the following information for interrupts:

- Operation
- Interrupt latency
- Interrupts during Sleep
- INT pin
- Automatic context saving

Many peripherals produce interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 7-1.

FIGURE 7-1: INTERRUPT LOGIC



9.6 Register Definitions: Watchdog Control

REGISTER 9-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-1/1	R/W-0/0
—	—	WDTPS<4:0>					SWDTEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-1 **WDTPS<4:0>:** Watchdog Timer Period Select bits(1)

Bit Value = Prescale Rate

11111 = Reserved. Results in minimum interval (1:32)
•
•
•
10011 = Reserved. Results in minimum interval (1:32)

10010 = 1:8388608 (2^{23}) (Interval 256s nominal)
10001 = 1:4194304 (2^{22}) (Interval 128s nominal)
10000 = 1:2097152 (2^{21}) (Interval 64s nominal)
01111 = 1:1048576 (2^{20}) (Interval 32s nominal)
01110 = 1:524288 (2^{19}) (Interval 16s nominal)
01101 = 1:262144 (2^{18}) (Interval 8s nominal)
01100 = 1:131072 (2^{17}) (Interval 4s nominal)
01011 = 1:65536 (Interval 2s nominal) (Reset value)
01010 = 1:32768 (Interval 1s nominal)
01001 = 1:16384 (Interval 512 ms nominal)
01000 = 1:8192 (Interval 256 ms nominal)
00111 = 1:4096 (Interval 128 ms nominal)
00110 = 1:2048 (Interval 64 ms nominal)
00101 = 1:1024 (Interval 32 ms nominal)
00100 = 1:512 (Interval 16 ms nominal)
00011 = 1:256 (Interval 8 ms nominal)
00010 = 1:128 (Interval 4 ms nominal)
00001 = 1:64 (Interval 2 ms nominal)
00000 = 1:32 (Interval 1 ms nominal)

bit 0 **SWDTEN:** Software Enable/Disable for Watchdog Timer bit

If WDTE<1:0> = 1x:
This bit is ignored.
If WDTE<1:0> = 01:
1 = WDT is turned on
0 = WDT is turned off
If WDTE<1:0> = 00:
This bit is ignored.

Note 1: Times are approximate. WDT time is based on 31 kHz LFINTOSC.

15.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Result formatting

15.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRISx and ANSELx bits. Refer to **Section 11.0 "I/O Ports"** for more information.

Note:	Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

15.1.2 CHANNEL SELECTION

There are 24 channel selections available for PIC16LF1566 and 35 for PIC16LF1567. Three channels (AN0, AN1 and AN2) can be selected by both ADC1 and ADC2. The following channels can be selected by either of the ADCs:

- AN<2:0> pins
- Temperature Indicator
- FVR Buffer 1
- VREFH

The CHS bits of the ADxCON0 register determine which channel is connected to the sample and hold circuit of ADCx.

When changing channels, a delay (TACQ) is required before starting the next conversion. Refer to **Section 15.2.6 "Individual ADC Conversion Procedure"** for more information.

15.1.3 ADC VOLTAGE REFERENCE

The ADC module uses a positive and a negative voltage reference. The positive reference is labeled VREFH and the negative reference is labeled VREFL.

The positive voltage reference (VREFH) is selected by the ADPREF bits in the ADCON1 register. The positive voltage reference source can be:

- VREF+ pin
- VDD

The negative voltage reference (VREFL) source is:

- VSS

15.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- FOSC/2
- FOSC/4
- FOSC/8
- FOSC/16
- FOSC/32
- FOSC/64
- FRC (internal RC oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11.5 TAD periods as shown in Figure 15-2.

For correct conversion, the appropriate TAD specification must be met. Refer to the ADC conversion requirements in **Section 25.0 "Electrical Specifications"** for more information. Table 15-1 gives examples of appropriate ADC clock selections.

Note:	Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

REGISTER 15-3: ADCON1(1)/ADCOMCON(2): ADC CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ADFM	ADCS<2:0>			ADNREF	GO/$\overline{\text{DONE}}$_ALL	ADPREF<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ADFM:** ADC Result Format Select bit
- 1 = Right justified. Six Most Significant bits of ADxRESxH are set to '0' when the conversion result is loaded.
- 0 = Left justified. Six Least Significant bits of ADxRESxL are set to '0' when the conversion result is loaded.

bit 6-4 **ADCS<2:0>:** ADC Conversion Clock Select bits
- 111 = FRC (clock supplied from an internal RC oscillator)
- 110 = FOSC/64
- 101 = FOSC/16
- 100 = FOSC/4
- 011 = FRC (clock supplied from an internal RC oscillator)
- 010 = FOSC/32
- 001 = FOSC/8
- 000 = FOSC/2

bit 3 **ADNREF:** ADC Negative Voltage Reference Configuration bit
- 1 = VREFL is connected to external VREF- pin(4)
- 0 = VREFL is connected to AVSS.

bit 2 **GO/$\overline{\text{DONE}}$_ALL(3):** Synchronized ADC Conversion Status bit
- 1 = Synchronized ADC conversion in progress. Setting this bit starts conversion in any ADC with ADxON = 1.
- 0 = Synchronized ADC conversion completed/ not in progress.

bit 1-0 **ADPREF<1:0>:** ADC Positive Voltage Reference Configuration bits
- 11 = VREFH is connected to internal Fixed Voltage Reference.
- 10 = VREFH is connected to external VREF+ pin(4)
- 01 = Reserved
- 00 = VREFH is connected to VDD

Note 1: Bank 1 name is ADCON1.

2: Bank 14 name is ADCOMCON.

3: Setting this bit triggers the GO/$\overline{\text{DONE}}$x bits in both ADCs. Each ADC will run a conversion according to its control register settings. This bit reads as an OR of the individual GO/$\overline{\text{DONE}}$x bits.

4: When selecting the VREF+ or VREF- pin as the source of the positive or negative reference, be aware that a minimum voltage specification exists. See **Section 25.0 "Electrical Specifications"** for details.

REGISTER 16-12: ADxGRD: HARDWARE CVD GUARD RING CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0
GRDxBOE(2)	GRDxAOE(2)	GRDxPOL(1,2)	—	—	—	—	TXxPOL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **GRDxBOE:** Guard Ring B Output Enable bit(2,3,5)
- 1 = ADC guard ring output is enabled to ADxGRDB(6) pin. Its corresponding TRISx bit must be clear.
- 0 = No ADC guard ring function to this pin is enabled

bit 6 **GRDxAOE:** Guard Ring A Output Enable bit(1,3,5)
- 1 = ADC Guard Ring Output is enabled to ADxGRDA(6) pin. Its corresponding TRISx, x bit must be clear.
- 0 = No ADC Guard Ring function is enabled

bit 5 **GRDxPOL:** Guard Ring Polarity Selection bit(4)
- 1 = ADCx guard ring outputs start as digital high during precharge stage
- 0 = ADCx guard ring outputs start as digital low during precharge stage

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **TXxPOL:** ADC x TX Polarity Select(3,4,5). ADxTXy registers determine location of TX pins.
- 1 = TX starts as digital high during Precharge stage
- 0 = TX starts as digital low during Precharge stage

Note 1: If precharge is enabled (ADxPRE! = '000000'), then Guard A switches polarity at the start of Acquisition / Charge Share. If precharge is disabled, then Guard A switches polarity as soon as the GO/DONEx bit is set.

2: Output function "B" is constant throughout all stages of the conversion cycle. In a dual sample setup it will switch polarity at the start of precharge.

3: The corresponding TRISx,x bit must be set to '0' to enable output.

4: When the ADxDSEN = 1 and ADxIPEN = 1; the polarity of this output is inverted for the second conversion time. The stored bit value does not change.

5: Outputs are maintained while ADxON = 1.

6: ADxGRD pin locations are selectable in APFCON, Register 3-9.

REGISTER 18-2: T1GCON: TIMER1 GATE CONTROL REGISTER

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W/HC-0/u	R-x/x	U-0	R/W-0/u
TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	—	T1GSS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **TMR1GE:** Timer1 Gate Enable bit
If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 counting is controlled by the Timer1 gate function
0 = Timer1 counts regardless of Timer1 gate function

bit 6 **T1GPOL:** Timer1 Gate Polarity bit
1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 5 **T1GTM:** Timer1 Gate Toggle Mode bit
1 = Timer1 Gate Toggle mode is enabled
0 = Timer1 Gate Toggle mode is disabled and toggle flip-flop is cleared
Timer1 gate flip-flop toggles on every rising edge.

bit 4 **T1GSPM:** Timer1 Gate Single-Pulse Mode bit
1 = Timer1 gate Single-Pulse mode is enabled and is controlling Timer1 gate
0 = Timer1 gate Single-Pulse mode is disabled

bit 3 **T1GGO/$\overline{\text{DONE}}$:** Timer1 Gate Single-Pulse Acquisition Status bit
1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge
0 = Timer1 gate single-pulse acquisition has completed or has not been started

bit 2 **T1GVAL:** Timer1 Gate Value Status bit
Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L.
Unaffected by Timer1 Gate Enable (TMR1GE).

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **T1GSS:** Timer1 Gate Source Select bits
01 = Timer0 overflow output (T0_overflow)
00 = Timer1 gate pin (T1G)

FIGURE 20-21: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 1, DHEN = 0)

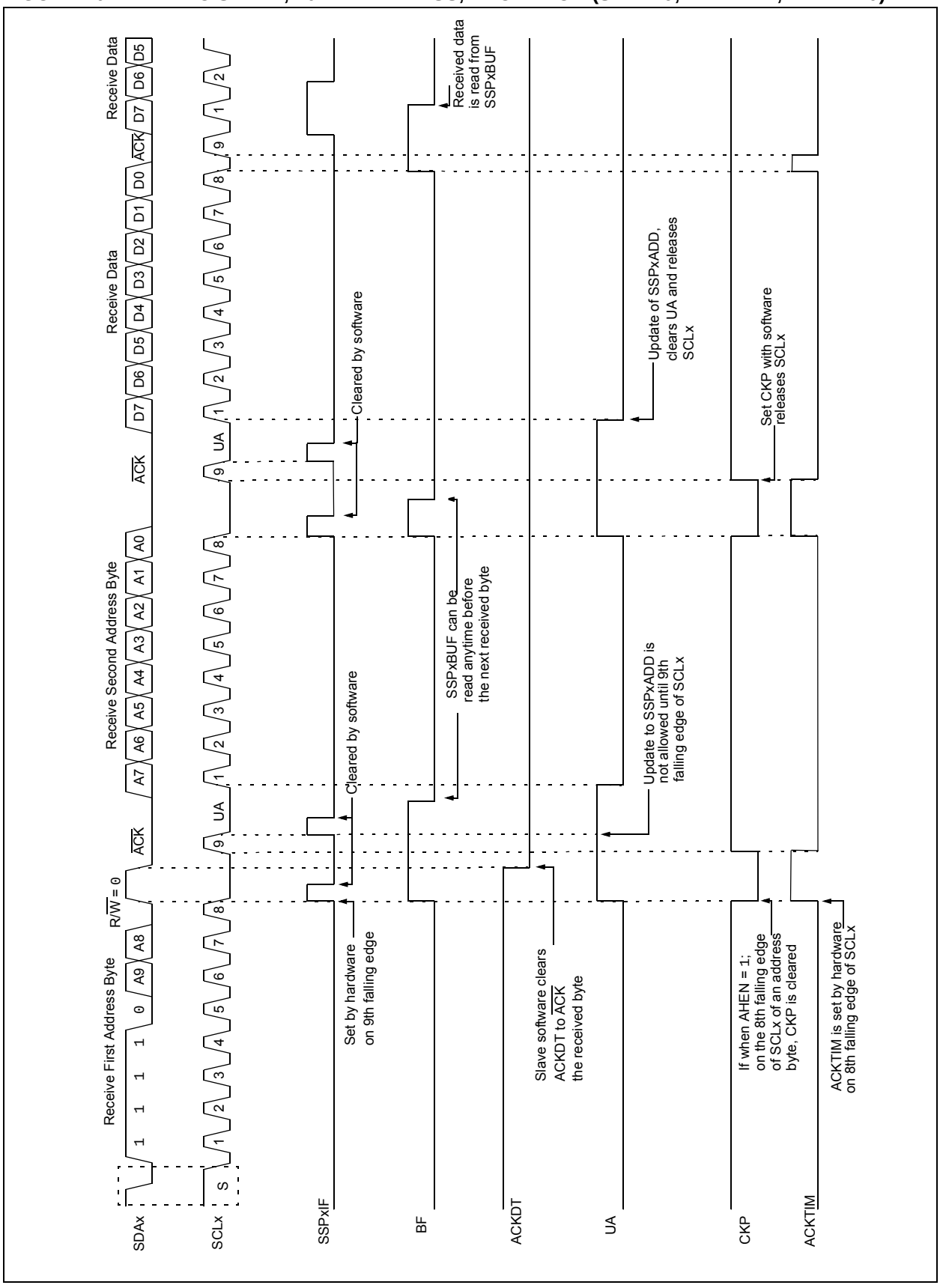


FIGURE 20-34: BUS COLLISION DURING START CONDITION (SCLX = 0)

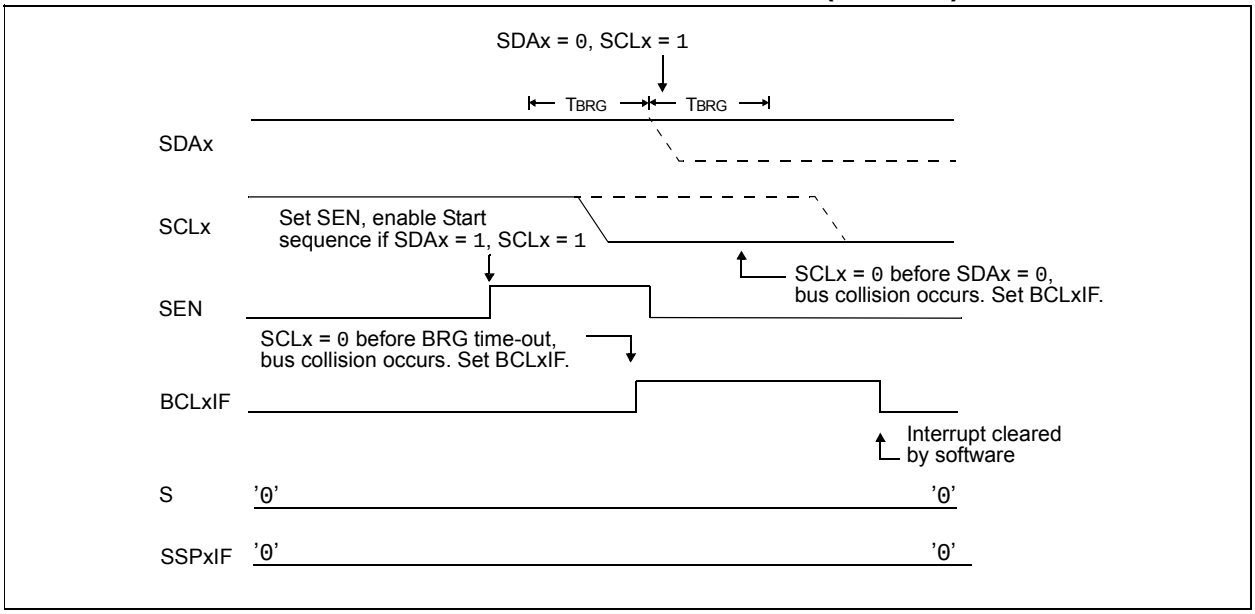
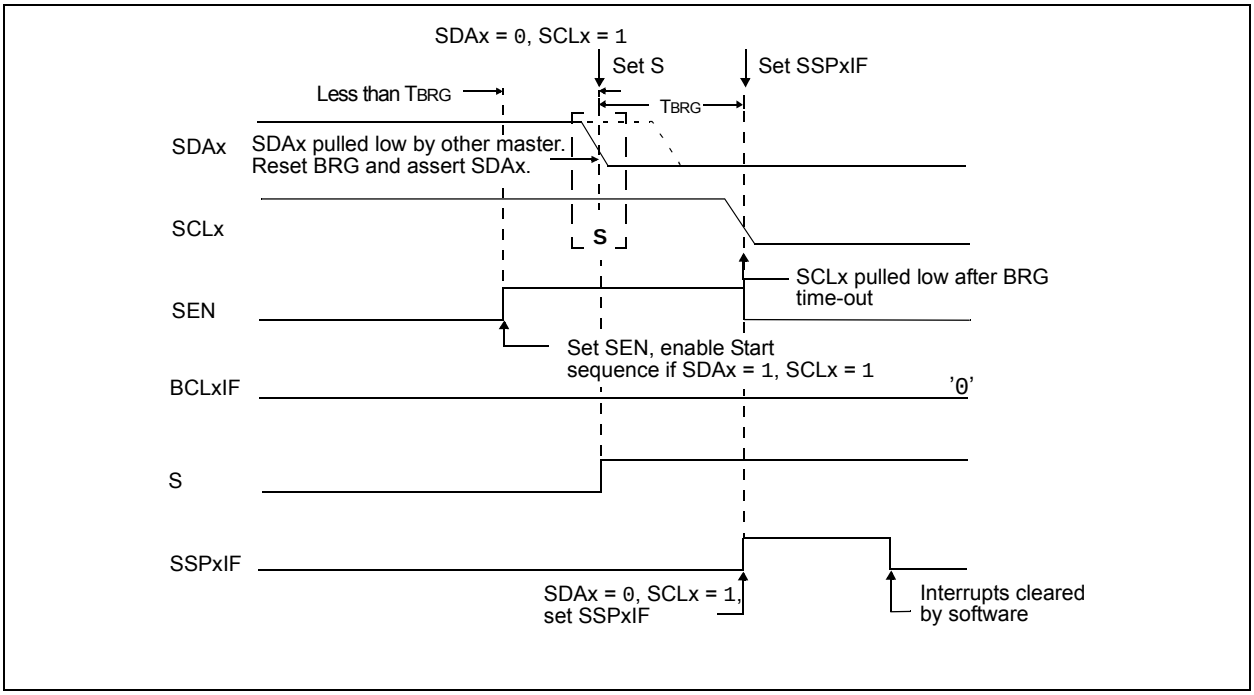


FIGURE 20-35: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION



21.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as ADC or DAC integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 21-1 and Figure 21-2.

The EUSART transmit output (TX_out) is available to the TX/CK pin and internally to the following peripherals:

- Configurable Logic Cell (CLC)

FIGURE 21-1: EUSART TRANSMIT BLOCK DIAGRAM

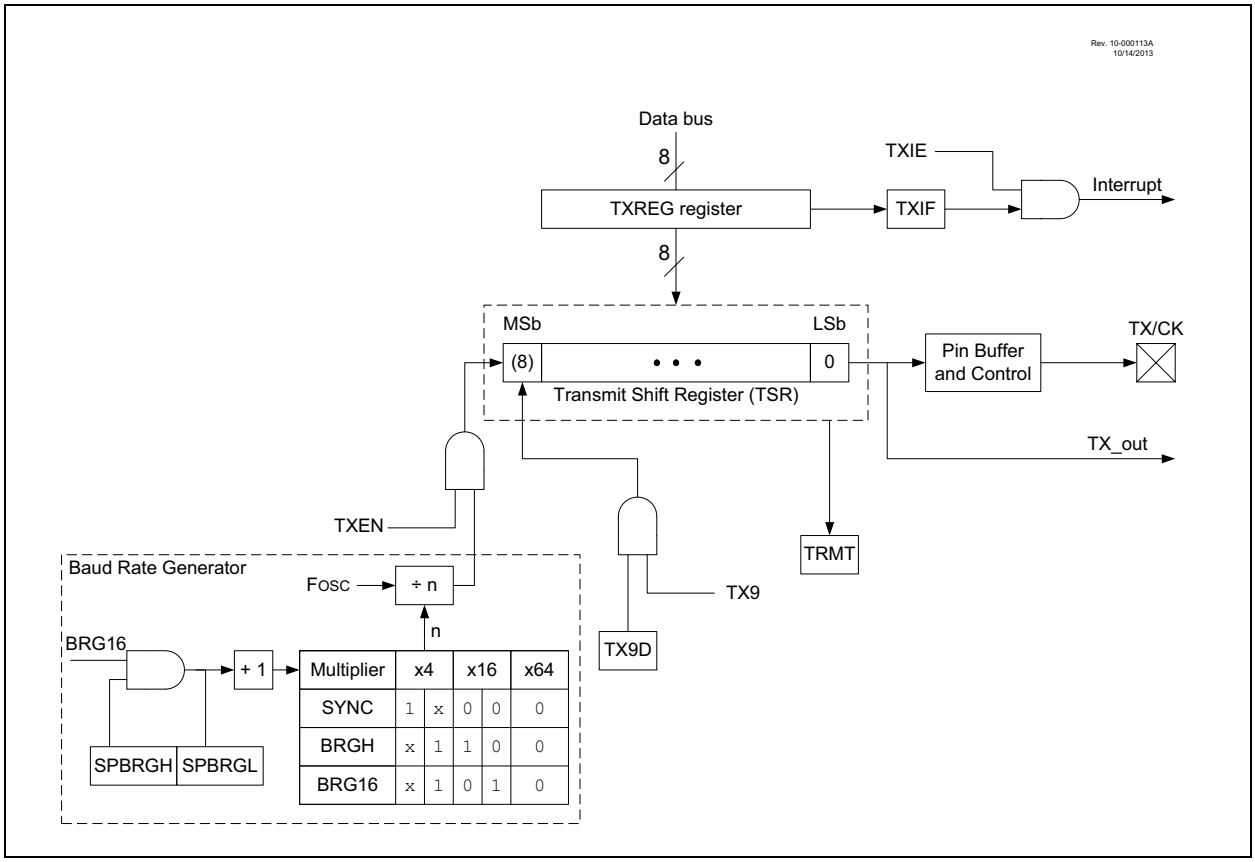
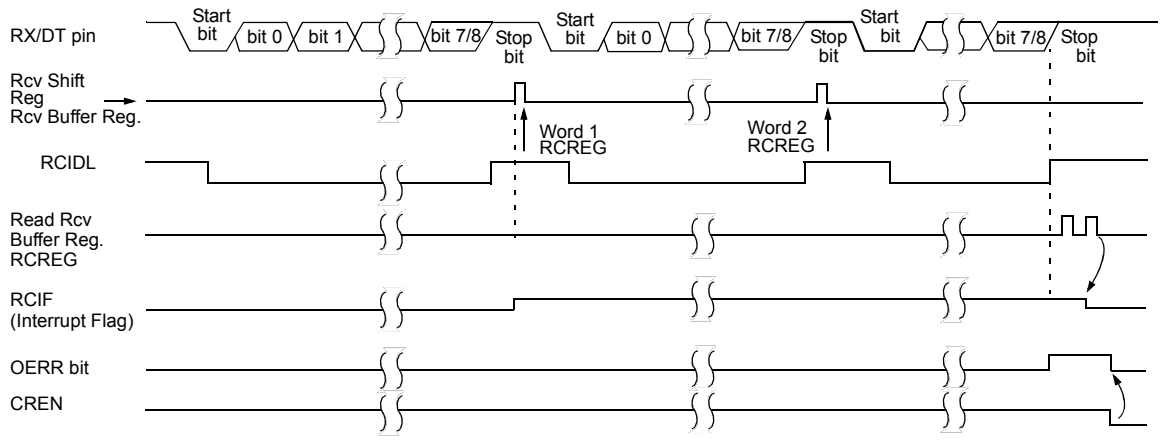


FIGURE 21-5: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows three words appearing on the RX input. The RCREG (receive buffer) is read after the third word, causing the OERR (overrun) bit to be set.

TABLE 21-2: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	266
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	84
PIE1	TMR1GIE	AD1IE	RCIE	TXIE	SSP1IE	SSP2IE	TMR2IE	TMR1IE	85
PIR1	TMR1GIF	AD1IF	RCIF	TXIF	SSP1IF	SSP2IF	TMR2IF	TMR1IF	87
RCREG	EUSART Receive Data Register								260*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	265
SPBRGL	BRG<7:0>								267*
SPBRGH	BRG<15:8>								267*
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	119
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	264

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for asynchronous reception.

* Page provides register information.

21.2 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as V_{DD} or temperature changes, and this directly affects the asynchronous baud rate.

The Auto-Baud Detect feature (see **Section 21.4.1 "Auto-Baud Detect"**) can be used to compensate for changes in the INTOSC frequency.

There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

21.4.1 AUTO-BAUD DETECT

The EUSART module supports automatic detection and calibration of the baud rate.

In the Auto-Baud Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. The Baud Rate Generator is used to time the period of a received 55h (ASCII "U") which is the Sync character for the LIN bus. The unique feature of this character is that it has five rising edges including the Stop bit edge.

Setting the ABDEN bit of the BAUDCON register starts the auto-baud calibration sequence (Figure 21-6). While the ABD sequence takes place, the EUSART state machine is held in Idle. On the first rising edge of the receive line, after the Start bit, the SPBRG begins counting up using the BRG counter clock as shown in Table 21-6. The fifth rising edge will occur on the RX pin at the end of the eighth bit period. At that time, an accumulated value totaling the proper BRG period is left in the SPBRGH:SPBRGL register pair, the ABDEN bit is automatically cleared and the RCIF interrupt flag is set. The value in the RCREG needs to be read to clear the RCIF interrupt. RCREG content should be discarded. When calibrating for modes that do not use the SPBRGH register the user can verify that the SPBRGL register did not overflow by checking for 00h in the SPBRGH register.

The BRG auto-baud clock is determined by the BRG16 and BRGH bits as shown in Table 21-6. During ABD, both the SPBRGH and SPBRGL registers are used as a 16-bit counter, independent of the BRG16 bit setting. While calibrating the baud rate period, the SPBRGH and SPBRGL registers are clocked at 1/8th the BRG base clock rate. The resulting byte measurement is the average bit time when clocked at full speed.

Note 1: If the WUE bit is set with the ABDEN bit, auto-baud detection will occur on the byte following the Break character (see **Section 21.4.3 "Auto-Wake-up on Break"**).

2: It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible.

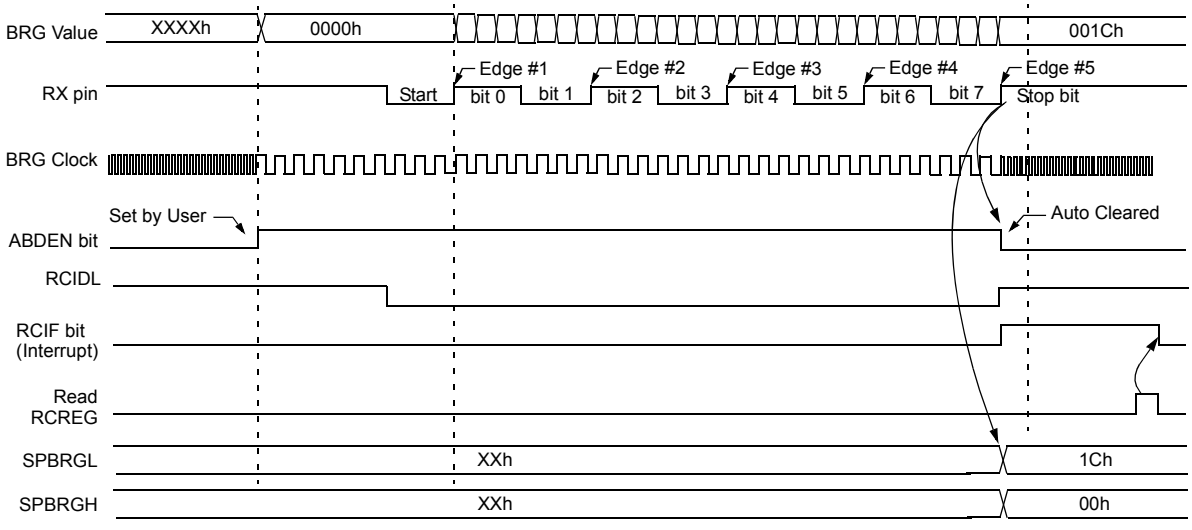
3: During the auto-baud process, the auto-baud counter starts counting at 1. Upon completion of the auto-baud sequence, to achieve maximum accuracy, subtract 1 from the SPBRGH:SPBRGL register pair.

TABLE 21-6: BRG COUNTER CLOCK RATES(1)

BRG16	BRGH	BRG Base Clock	BRG ABD Clock
0	0	FOSC/64	FOSC/512
0	1	FOSC/16	FOSC/128
1	0	FOSC/16	FOSC/128
1	1	FOSC/4	FOSC/32

Note 1: During the ABD sequence, SPBRGL and SPBRGH registers are both used as a 16-bit counter, independent of BRG16 setting.

FIGURE 21-6: AUTOMATIC BAUD RATE CALIBRATION



Note 1: The ABD sequence requires the **EUSART** module to be configured in Asynchronous mode.

22.1.5 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when PRx is 255. The resolution is a function of the PRx register value as shown by Equation 22-4.

EQUATION 22-4: PWM RESOLUTION

$$Resolution = \frac{log[4(PRxs + 1)]}{log(2)} \ bits$$

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 22-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 32 MHz)

PWM Frequency	1.95 kHz	7.81 kHz	31.25 kHz	125 kHz	250 kHz	333.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PRx Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 22-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	0.31 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale	64	4	1	1	1	1
PRx Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 22-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	0.31 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	64	4	1	1	1	1
PRx Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

22.1.6 OPERATION IN SLEEP MODE

In Sleep mode, the TMRx register will not increment and the state of the module will not change. If the PWMx pin is driving a value, it will continue to drive that value. When the device wakes up, TMRx will continue from its previous state.

22.1.7 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency (FOSC). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 5.0 "Oscillator Module"** for additional details.

22.1.8 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the PWM registers to their Reset states.

22.2 Register Definitions: PWM Control

REGISTER 22-1: PWMxCON: PWM CONTROL REGISTER

R/W-0	R/W-0	R-0	R/W-0	U-0	U-0	U-0	U-0
PWMxEN	PWMxOE	PWMxOUT	PWMxPOL	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **PWMxEN:** PWM Enable Bit
1 = PWM module is enabled
0 = PWM module is disabled

bit 6 **PWMxOE:** PWM Output on pin PWMx Enable Bit
1 = Output to PWMx pin is enabled
0 = Output to PWMx pin is disabled (PWMxy pins may still be enabled, see Register 22-3)

bit 5 **PWMxOUT:** PWM Output Value Bit
1 = PWM output is high
0 = PWM output is low

bit 4 **PWMxPOL:** PWM Polarity Bit
1 = PWM output is active-low
0 = PWM output is active-high

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 22-2: PWMTMRS: PWM TIMER SELECT REGISTER(1)

U-0	U-0	U-0	R/W-0/0	U-0	R/W-0/0	U-0	R/W-0/0
				—	P2TSEL	—	P1TSEL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2 **P2TSEL:** PWM2 Timer Selection bit
1 = PWM is based off Timer 4
0 = PWM is based off Timer 2

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **P1TSEL:** PWM1 Timer Selection bit
1 = PWM is based off Timer 4
0 = PWM is based off Timer 2

SWAPF	Swap Nibbles in f
Syntax:	[*label*] SWAPF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f<3:0>) → (destination<7:4>), (f<7:4>) → (destination<3:0>)
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

TRIS	Load TRIS Register with W
Syntax:	[*label*] TRIS f
Operands:	$5 \le f \le 7$
Operation:	(W) → TRIS register 'f'
Status Affected:	None
Description:	Move data from W register to TRIS register. When 'f' = 5, TRISA is loaded. When 'f' = 6, TRISB is loaded. When 'f' = 7, TRISC is loaded.

XORLW	Exclusive OR literal with W
Syntax:	[*label*] XORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .XOR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) → (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

25.4 AC Characteristics

Timing Parameter Symbology has been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

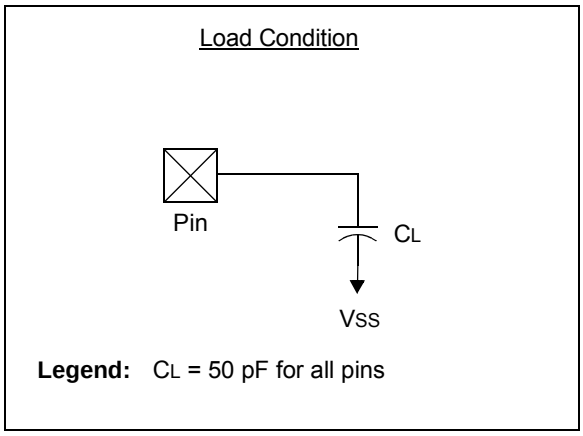
Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	CLKIN
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDIx	sc	SCKx
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O PORT	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

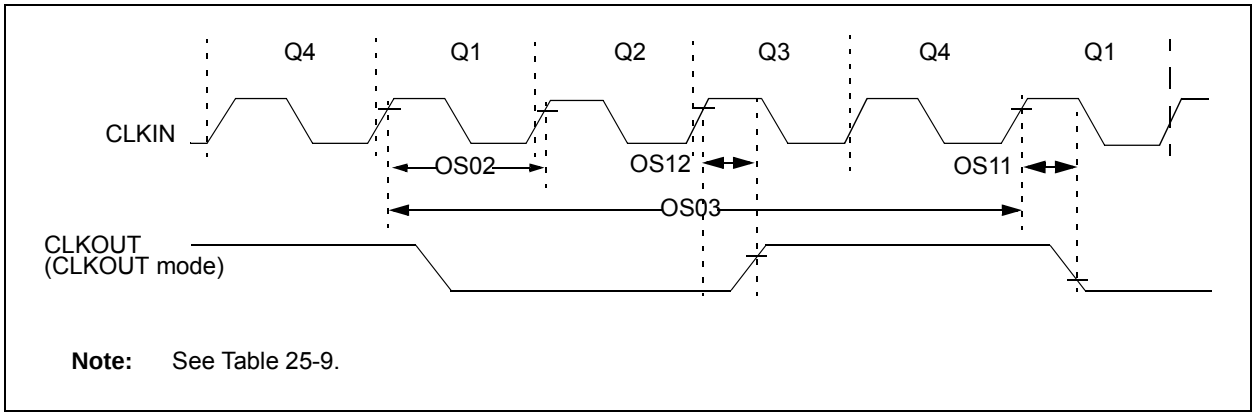
S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 25-3: LOAD CONDITIONS



Legend: CL = 50 pF for all pins

FIGURE 25-4: CLOCK TIMING



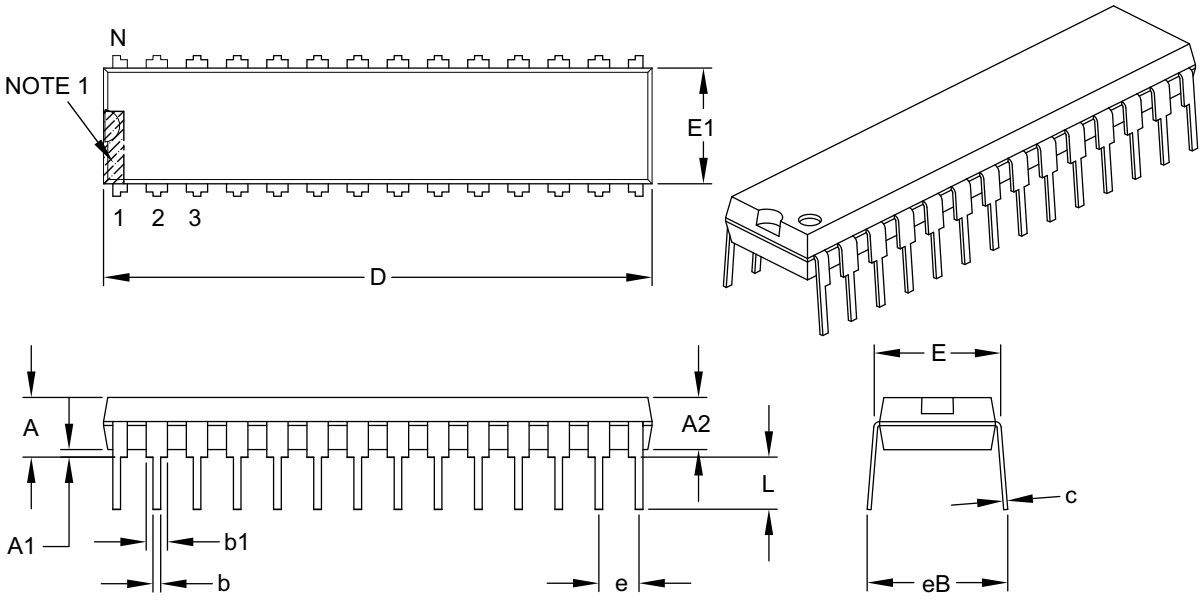
Note: See Table 25-9.

28.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

