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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 34x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1567-i-pt

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

	BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23
800h															
801h															
802h															
803h															
804h															
805h							CPI I Core Registe	r 600 Ta	hle 3-2 for specifics						
806h							CI O COIE Registe	1, 300 10	bie 5-2 for specifics						
807h															
808h															
809h															
80Ah															
80Bh															
80Ch	—	88Ch	—	90Ch	—	98Ch	—	A0Ch	—	A8Ch	—	B0Ch	—	B8Ch	—
80Dh	—	88Dh	—	90Dh	—	98Dh	—	A0Dh	—	A8Dh	—	B0Dh	_	B8Dh	—
80Eh	—	88Eh	—	90Eh	—	98Eh	—	A0Eh	—	A8Eh	—	B0Eh	_	B8Eh	—
80Fh	—	88Fh	—	90Fh	—	98Fh	—	A0Fh	—	A8Fh	—	B0Fh	_	B8Fh	—
810h	—	890h	—	910h	—	990h	—	A10h	—	A90h	—	B10h	—	B90h	—
811h	—	891h	—	911h	—	991h	—	A11h	—	A91h	—	B11h	_	B91h	—
812h	—	892h	—	912h	—	992h	—	A12h	—	A92h	—	B12h	—	B92h	—
813h	—	893h	—	913h	—	993h	—	A13h	—	A93h	—	B13h	_	B93h	—
814h	—	894h	—	914h	—	994h	—	A14h	—	A94h	—	B14h	_	B94h	—
815h	—	895h	—	915h	—	995h	—	A15h	—	A95h	—	B15h	_	B95h	—
816h	—	896h	—	916h	—	996h	—	A16h	—	A96h	—	B16h	_	B96h	—
817h	—	897h	—	917h	—	997h	—	A17h	—	A97h	—	B17h	_	B97h	—
818h	—	898h	—	918h	—	998h	_	A18h	_	A98h	_	B18h	—	B98h	_
819h	—	899h	—	919h	—	999h	_	A19h	_	A99h	_	B19h	—	B99h	_
81Ah	—	89Ah	—	91Ah	—	99Ah	_	A1Ah	_	A9Ah	_	B1Ah	—	B9Ah	_
81Bh	—	89Bh	—	91Bh	—	99Bh	—	A1Bh	—	A9Bh	—	B1Bh	_	B9Bh	—
81Ch	—	89Ch	—	91Ch	—	99Ch	_	A1Ch	_	A9Ch	_	B1Ch	—	B9Ch	
81Dh	—	89Dh	—	91Dh	—	99Dh	—	A1Dh	—	A9Dh	—	B1Dh	_	B9Dh	—
81Eh	—	89Eh	—	91Eh	—	99Eh	—	A1Eh	—	A9Eh	—	B1Eh	_	B9Eh	—
81Fh	—	89Fh	—	91Fh	—	99Fh	—	A1Fh	—	A9Fh	—	B1Fh	—	B9Fh	—
820h		8A0h		920h		9A0h		A20h		AA0h		B20h		BA0h	
	Unimplemented		Unimplemented		Unimplemented		Unimplemented		Unimplemented		Unimplemented		Unimplemented		Unimplemented

Read as '0'

Accesses

70h – 7Fh

A6Fh

A70h

A7Fh

Read as '0'

Accesses

70h – 7Fh

AEFh

AF0h

AFFh

Read as '0'

Accesses

70h – 7Fh

B6Fh

B70h

B7Fh

Read as '0'

Accesses

70h – 7Fh

BEFh

BF0h

BFFh

Read as '0'

Accesses

70h – 7Fh

TABLE 3-6: PIC16LF1566/1567 MEMORY MAP, BANKS 16-23

86Fh

870h

87Fh

Read as '0'

Accesses

70h – 7Fh

8EFh

8F0h

8FFh

Read as '0'

Accesses

70h – 7Fh

Read as '0'

Accesses

70h – 7Fh

9EFh

9F0h

9FFh

96Fh

970h

97Fh

PIC16LF1566/1567

PIC16LF1566/1567

REGISTE	$-\pi 4-2$. CON		GURATION					
		R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1	
		LVP	DEBUG	LPBOR	BORV	STVREN	_	
		bit 13					bit 8	
U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1	
_	—	_	_	_	—	WRT	<1:0>	
bit 7							bit 0	
1								
Legend:								
R = Read	able bit	P = Program	nable bit	U = Unimplem	nented bit, rea	d as '1'		
'0' = Bit is	cleared	'1' = Bit is set		-n = Value wh	en blank or af	ter Bulk Erase		
bit 13 bit 12	bit 13 LVP: Low-Voltage Programming Enable bit ⁽¹⁾ 1 = Low-voltage programming enabled 0 = High-voltage on MCLR must be used for programming bit 12 DEBUG: In-Circuit Debugger Mode bit ⁽²⁾ 1 = In-Circuit Debugger disabled ICSPCI K and ICSPDAT are general purpose I/O pins							
bit 11	1 = Low-Pow 0 = Low-Pow	-Power BOR E ver Brown-out F ver Brown-out F	inable bit Reset is disable Reset is enable	d d			21	
bit 10	BORV: Brow 1 = Brown-ou 0 = Brown-ou	n-Out Reset Vo ut Reset voltage ut Reset voltage	bltage Selection e (VBOR), low tr e (VBOR), high t	n bit ⁽³⁾ Tip point selecte trip point select	ed			
bit 9	STVREN: Sta 1 = Stack Ov 0 = Stack Ov	ack Overflow/U erflow or Under erflow or Under	nderflow Rese flow will cause flow will not ca	t Enable bit a Reset uuse a Reset				
bit 8-2	Unimplemer	nted: Read as '	1'					
bit 1-0	bit 1-0 WRT<1:0>: Flash Memory Self-Write Protection bits 8 kW Flash memory 11 = Write protection off 10 = 000h to 01FFh write protected, 0200h to 1FFFh may be modified 01 = 000h to 0FFFh write protected, 1000h to 1FFFh may be modified 00 = 000h to 1FFFh write protected, no addresses may be modified							
Note 1: 2:	The LVP bit canr The DEBUG bit i debuggers and p	he LVP bit cannot be programmed to '0' when Programming mode is entered via LVP. he DEBUG bit in Configuration Words is managed automatically by device development tools including ebuggers and programmers. For normal device operation, this bit should be maintained as a '1'.						

REGISTER 4-2: CONFIG2: CONFIGURATION WORD 2

3: See VBOR parameter for specific trip point voltages.

5.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bits of the OSCCON register. The following clock sources can be selected using the SCS bits:

- Default system oscillator determined by FOSC bits in Configuration Words
- Internal Oscillator Block (INTOSC)

5.3.1 SYSTEM CLOCK SELECT (SCS) BITS

The System Clock Select (SCS) bits of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bits of the OSCCON register = 00, the system clock source is determined by value of the FOSC<1:0> bits in the Configuration Words.
- When the SCS bits of the OSCCON register = 1x, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<3:0> bits of the OSCCON register. After a Reset, the SCS bits of the OSCCON register are always cleared.

When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 5-1.

Switch From	Switch To	Frequency	Oscillator Delay
Sleep	LFINTOSC ⁽¹⁾ MFINTOSC ⁽¹⁾ HFINTOSC ⁽¹⁾	31 kHz 31.25 kHz-500 kHz 31.25 kHz-16 MHz	Oscillator Warm-Up Delay Twarm ⁽²⁾
Sleep/POR	EC ⁽¹⁾	DC – 32 MHz	2 cycles
LFINTOSC	EC ⁽¹⁾	DC – 32 MHz	1 cycle of each
Any clock source	MFINTOSC ⁽¹⁾ HFINTOSC	31.25 kHz-500 MHz 31.25 kHz-16 MHz	2 μs (approx.)
Any clock source	LFINTOSC	31 kHz	1 cycle of each
PLL inactive	PLL active	16-32 MHz	2 ms (approx.)

TABLE 5-1: OSCILLATOR SWITCHING DELAYS

Note 1: PLL inactive

2: See Section 25.0 "Electrical Specifications"

11.4 Register Definitions: PORTA

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R-x/x	R/W-x/x	R/W-x/x	R/W-x/x
RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimplemented bit, read as '0'				
u = Bit is unchanged x = Bit is unknown		iown	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets	
'1' = Bit is set		'0' = Bit is clea	ared				

REGISTER 11-2: PORTA: PORTA REGISTER

bit 7-0 RA<7:0>: RA7:RA0 PORTA I/O Value bits⁽¹⁾ 1 = Port pin is ≥ VIH 0 = Port pin is ≤ VIL

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 11-3: TRISA: PORTA TRI-STATE REGISTER

| R/W-1/1 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 |
| bit 7 | | | | | | | bit 0 |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 TRISA<7:0>: PORTA Tri-State Control bit

1 = PORTA pin configured as an input (tri-stated)

0 = PORTA pin configured as an output

14.0 TEMPERATURE INDICATOR MODULE

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The circuit's range of operating temperature falls between -40°C and +85°C. The output is a voltage that is proportional to the device temperature. The output of the temperature indicator is internally connected to the device ADC.

The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately. Reference Application Note AN1333, *"Use and Calibration of the Internal Temperature Indicator"* (DS01333) for more details regarding the calibration process.

14.1 Circuit Operation

Figure 14-1 shows a simplified block diagram of the temperature circuit. The proportional voltage output is achieved by measuring the forward voltage drop across multiple silicon junctions.

Equation 14-1 describes the output characteristics of the temperature indicator.

EQUATION 14-1: VOUT RANGES

High Range: VOUT = VDD - 4VT

Low Range: VOUT = VDD - 2VT

The temperature sense circuit is integrated with the Fixed Voltage Reference (FVR) module. See **Section 13.0 "Fixed Voltage Reference (FVR)"** for more information.

The circuit is enabled by setting the TSEN bit of the FVRCON register. When disabled, the circuit draws no current.

The circuit operates in either high or low range. The high range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range, but may be less consistent from part to part. This range requires a higher bias voltage to operate and thus, a higher VDD is needed.

The low range is selected by clearing the TSRNG bit of the FVRCON register. The low range generates a lower voltage drop and thus, a lower bias voltage is needed to operate the circuit. The low range is provided for low voltage operation.

FIGURE 14-1: TEMPERATURE CIRCUIT DIAGRAM



14.2 Minimum Operating VDD

When the temperature circuit is operated in low range, the device may be operated at any operating voltage that is within specifications.

When the temperature circuit is operated in high range, the device operating voltage, VDD, must be high enough to ensure that the temperature circuit is correctly biased.

Table 14-1 shows the recommended minimum VDD vs. range setting.

TABLE 14-1: RECOMMENDED VDD vs. RANGE

Min. VDD, TSRNG = 1	Min. VDD, TSRNG = 0			
3.6V	1.8V			

14.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to **Section 15.0 "Analog-to-Digital Converter (ADC) Module"** for detailed information.

15.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- · Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- · Interrupt control
- Result formatting

15.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRISx and ANSELx bits. Refer to **Section 11.0 "I/O Ports"** for more information.

Note:	Analog voltages on any pin that is defined				
	as a digital input may cause the input				
	buffer to conduct excess current.				

15.1.2 CHANNEL SELECTION

There are 24 channel selections available for PIC16LF1566 and 35 for PIC16LF1567. Three channels (AN0, AN1 and AN2) can be selected by both ADC1 and ADC2. The following channels can be selected by either of the ADCs:

- AN<2:0> pins
- Temperature Indicator
- FVR Buffer 1
- VREFH

The CHS bits of the ADxCON0 register determine which channel is connected to the sample and hold circuit of ADCx.

When changing channels, a delay (TACQ) is required before starting the next conversion. Refer to **Section 15.2.6 "Individual ADC Conversion Procedure"** for more information.

15.1.3 ADC VOLTAGE REFERENCE

The ADC module uses a positive and a negative voltage reference. The positive reference is labeled VREFH and the negative reference is labeled VREFL.

The positive voltage reference (VREFH) is selected by the ADPREF bits in the ADCON1 register. The positive voltage reference source can be:

- VREF+ pin
- Vdd
- The negative voltage reference (VREFL) source is:
- Vss

15.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- FRC (internal RC oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11.5 TAD periods as shown in Figure 15-2.

For correct conversion, the appropriate TAD specification must be met. Refer to the ADC conversion requirements in **Section 25.0 "Electrical Specifications"** for more information. Table 15-1 gives examples of appropriate ADC clock selections.

Note: Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

16.1 Hardware CVD Operation

Capacitive Voltage Divider is a charge averaging capacitive sensing method. The hardware CVD module will automate the process of charging, averaging between the external sensor and the internal ADC sample and hold capacitor, and then initiating the ADC conversions. The whole process can be expanded into three stages: precharge, acquisition, and conversion. See Figure 16-5 for basic information on the timing of three stages.

16.1.1 PRE-CHARGE TIMER

The precharge stage is an optional 1-127 instruction/TAD cycle time delay used to put the external ADC channel and the internal sample and hold capacitor (CHOLD) into pre-conditioned states. The precharge stage of conversion is enabled by writing a non-zero value to the ADxPRE<6:0> bits of the AADxPRE register. This stage is initiated when a conversion sequence is started by either the GO/DONEx, GO/DONE_ALL bit or a Special Event Trigger. When initiating an ADC conversion, if the ADxPRE bits are cleared, this stage is skipped.

During the precharge time, CHOLD is disconnected from the outer portion of the sample path that leads to the external capacitive sensor and is connected to either VDD or VSS, depending on the value of the ADxEPPOL bit of the AADxCON3 register. At the same time, the port pin logic of the selected analog channel is overridden to drive a digital high or low out, in order to precharge the outer portion of the ADC's sample path, which includes the external sensor. The output polarity of this override is determined by the ADxEPPOL bit of the AADxCON3 register.

Even though the analog channel of the pin is selected, the analog multiplexer is forced open during the precharge stage. The ADC multiplex or logic is overridden and disabled only during the precharge time.

16.1.2 ACQUISITION TIMER

The acquisition timer controls the time allowed to acquire the signal to be sampled. The acquisition delay time is from 1 to 127 instruction/TAD cycles and is used to allow the voltage on the internal sample and hold capacitor (CHOLD) to settle to a final value through charge averaging. The acquisition time of conversion is enabled by writing a non-zero value to the AADxACQ<6:0> bits of the AADxACQ register. When the acquisition time is enabled, the time starts immediately following the precharge stage. If the ADxPRE<6:0> bits of the AADxPRE register are set to zero, the acquisition time is initiated by either setting the GO/DONEx, GO/DONE_ALL bit or a Special Event Trigger.

At the start of the acquisition stage, the port pin logic of the selected analog channel is again overridden to turn off the digital high/low output drivers so that they do not affect the final result of charge averaging. Also, the selected ADC channel is connected to CHOLD. This allows charge averaging to proceed between the precharged channel and the CHOLD capacitor.

16.1.3 STARTING A CONVERSION

To enable the ADC module, the ADxCON bit of the AADxCON0 register must be set. Setting the GO/DONEx, GO/DONE_ALL or by the Special Event Trigger inputs will start the Analog-to-Digital conversion.

Once a conversion begins, it proceeds until complete, while the ADxON bit is set. If the ADxON bit is cleared, the conversion is halted. The GO/DONEx bit of the AADxCON0 register indicates that a conversion is occurring, regardless of the starting trigger.

Note:	The GO/DONEx bit should not be set in the same instruction that turns on the ADC.					
	Refer to Section Section 16.1.12					
	"Hardware CVD Double Conversion					
	Flocedule					

16.1.4 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/DONEx bit of the AADxCON0 register or clear the GO/DONE_ALL bit of the ADCON1 register if synchronized conversion is used.
- Set the ADxIF interrupt flag bit of the PIRx register.
- Update the AADxRESxH and AADxRESxL registers with new conversion results.

REGISTER 16-4: AD2CH0: HARDWARE CVD 2 SECONDARY CHANNEL SELECT **REGISTER**^(1,2,3,4)

	NEOR						
R/W-0/0							
CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20
bit 7	·					•	bit 0

Legena:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

CHx: Channel x to A/D 2 Connection bit ^(1,2,3,4,5)
1 = ANx is connected to A/D 2
0 = ANx is not connected to A/D 2

Note 1: This register selects secondary channels which are connected in parallel to the primary channel selected in ADxCON1. Precharge bias is applied to both the primary and secondary channels.

- **2:** If the same channel is selected as both primary (ADxCON1) and secondary then the selection as primary takes precedence.
- 3: Enabling these bits automatically overrides the corresponding TRISx.x bit to tri-state the selected pin.
- 4: In the same way that the CHSx bits in ADCON0 only close the switch when the A/D is enabled, these connections and the TRIS overrides are only active if the A/D is enabled by setting ADxON.

REGISTER 16-5: AD2CH1: ANALOG-TO-DIGITAL (A/D) 2 SECONDARY CHANNEL SELECT REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CH45 ⁽⁵⁾	CH44 ⁽⁵⁾	CH43 ⁽⁵⁾	CH42 ⁽⁵⁾	CH41 ⁽⁵⁾	CH40	CH29	CH28
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 CHx: Channel x to A/D 2 Connection bit^(1,2,3,4)

- 1 = ANx is connected to A/D 2
 - 0 = ANx is not connected to A/D 2
- **Note 1:** This register selects secondary channels which are connected in parallel to the primary channel selected in ADxCON1. Precharge bias is applied to both the primary and secondary channels.
 - **2:** If the same channel is selected as both primary (ADxCON1) and secondary then the selection as primary takes precedence.
 - 3: Enabling these bits automatically overrides the corresponding TRISx.x bit to tri-state the selected pin.
 - 4: In the same way that the CHSx bits in ADCON0 only close the switch when the A/D is enabled, these connections and the TRIS overrides are only active if the A/D is enabled by setting ADxON.
 - 5: PIC16LF1567 only. Unimplemented / Read as '0' on PIC16LF1566

FIGURE 18-6:	TIMER1 GATE SINGLE	E-PULSE AND TOGGLE COMBIN	IED MODE
TMR1 <u>GE</u> T1GP <u>OL</u>			
T1GSPM			
T1GTM			
T1GG <u>O/</u> DONE	✓ Set by software Counting enabled	on	Cleared by hardware on falling edge of T1GVAL
t1g_in	rising edge of 110		
т1скі			
T1GVAL			
Timer1	Ν	N + 1 N + 2 N + 3 N + 4	
TMR1GIF	 Cleared by software 	Set by hardware on falling edge of T1GVAL —►	Cleared by ← software

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	84
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	SSP2IE	TMR2IE	TMR1IE	85
PIE2	—	AD2IE	—	—	BCL1IE	BCL2IE	TMR4IE	—	86
PIR1	TMR1GIF	AD1IF	RCIF	TXIF	SSP1IF	SSP2IF	TMR2IF	TMR1IF	87
PIR2	—	AD2IF	—	—	BCL1IF	BCL2IF	TMR4IF	—	88
PR2	Timer2 Mod	ule Period Re	gister						194*
PR4	Timer4 Mod	ule Period Re	gister						194*
T2CON	—		T2OUT	PS<3:0>		TMR2ON	T2CKPS1	T2CKPS0	195
T4CON	—	T4OUTPS<3:0> TMR4ON T4CKPS1 T4CKPS0						195	
TMR2	Holding Register for the 8-bit TMR2 Register								193*
TMR4	Holding Reg	ister for the 8	-bit TMR4 Re	gister ⁽¹⁾					193*

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Timer2/4 module.

* Page provides register information.

20.5.2 SLAVE RECEPTION

When the R/\overline{W} bit of a matching received address byte is clear, the R/\overline{W} bit of the SSPxSTAT register is cleared. The received address is loaded into the SSPxBUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF of the SSPxSTAT register is set, or bit SSPOV of the SSPxCON1 register is set. The BOEN bit of the SSPxCON3 register modifies this operation. For more information see Register 20-4.

An MSSPx interrupt is generated for each transferred data byte. Flag bit, SSPxIF, must be cleared by software.

When the SEN bit of the SSPxCON2 register is set, SCLx will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit of the SSPxCON1 register, except sometimes in 10-bit mode. See **Section 20.2.3 "SPI Master Mode**" for more detail.

20.5.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSPx module configured as an I^2C slave in 7-bit Addressing mode. Figure 20-14 and Figure 20-15 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I^2C communication.

- 1. Start bit detected.
- 2. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- 3. Matching address with R/\overline{W} bit clear is received.
- 4. The slave pulls SDAx low sending an ACK to the master, and sets SSPxIF bit.
- 5. Software clears the SSPxIF bit.
- 6. Software reads received address from SSPxBUF clearing the BF flag.
- 7. If SEN = 1; Slave software sets CKP bit to release the SCLx line.
- 8. The master clocks out a data byte.
- 9. Slave drives SDAx low sending an ACK to the master, and sets SSPxIF bit.
- 10. Software clears SSPxIF.
- 11. Software reads the received byte from SSPxBUF clearing BF.
- 12. Steps 8-12 are repeated for all received bytes from the master.
- 13. Master sends Stop condition, setting P bit of SSPxSTAT, and the bus goes idle.

20.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the eighth falling edge of SCLx. These additional interrupts allow the slave software to decide whether it wants to ACK the receive address or data byte, rather than the hardware. This functionality adds support for PMBus[™] that was not present on previous versions of this module.

This list describes the steps that need to be taken by slave software to use these options for $I^{2}C$ communication. Figure 20-16 displays a module using both address and data holding. Figure 20-17 includes the operation with the SEN bit of the SSPxCON2 register set.

- 1. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- Matching address with R/W bit clear is clocked in. SSPxIF is set and CKP cleared after the eighth falling edge of SCLx.
- 3. Slave clears the SSPxIF.
- Slave can look at the ACKTIM bit of the SSPxCON3 register to determine if the SSPxIF was after or before the ACK.
- 5. Slave reads the address value from SSPxBUF, clearing the BF flag.
- Slave sets ACK value clocked out to the master by setting ACKDT.
- 7. Slave releases the clock by setting CKP.
- 8. SSPxIF is set after an \overline{ACK} , not after a NACK.
- 9. If SEN = 1 the slave hardware will stretch the clock after the ACK.
- 10. Slave clears SSPxIF.

- 11. SSPxIF set and CKP cleared after eighth falling edge of SCLx for a received data byte.
- 12. Slave looks at ACKTIM bit of SSPxCON3 to determine the source of the interrupt.
- 13. Slave reads the received data from SSPxBUF clearing BF.
- 14. Steps 7-14 are the same for each received data byte.
- 15. Communication is ended by either the slave sending an ACK = 1, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSTSTAT register.

Note: SSPxIF is still set after the ninth falling edge of SCLx even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSPxIF not set

20.6.2 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, releases the SCLx pin (SCLx allowed to float high). When the SCLx pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCLx pin is actually sampled high. When the SCLx pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and begins counting. This ensures that the SCLx high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 20-25).

FIGURE 20-25: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION



20.6.3 WCOL STATUS FLAG

If the user writes the SSPxBUF when a Start, Restart, Stop, Receive or Transmit sequence is in progress, the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur). Any time the WCOL bit is set it indicates that an action on SSPxBUF was attempted while the module was not Idle.

Note:	Because queuing of events is not allowed,									
	writing to the lower five bits of SSPxCON2									
	is disabled until the Start condition is									
	complete.									

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20.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- a) SDAx or SCLx are sampled low at the beginning of the Start condition (Figure 20-33).
- b) SCLx is sampled low before SDAx is asserted low (Figure 20-34).

During a Start condition, both the SDAx and the SCLx pins are monitored.

If the SDAx pin is already low, or the SCLx pin is already low, then all of the following occur:

- · the Start condition is aborted,
- · the BCLxIF flag is set and
- the MSSPx module is reset to its Idle state (Figure 20-33).

The Start condition begins with the SDAx and SCLx pins deasserted. When the SDAx pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCLx pin is sampled low while SDAx is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDAx pin is sampled low during this count, the BRG is reset and the SDAx line is asserted early (Figure 20-35). If, however, a '1' is sampled on the

SDAx pin, the SDAx pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCLx pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCLx pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDAx before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion. Repeated Start or Stop conditions.

FIGURE 20-33: BUS COLLISION DURING START CONDITION (SDAX ONLY)



REGISTER 20-2: SSPxCON1: SSPx CONTROL REGISTER 1 (CONTINUED)

- bit 3-0 SSPM<3:0>: Synchronous Serial Port Mode Select bits 1111 = I^2C Slave mode, 10-bit address with Start and Stop bit interrupts enabled $1110 = I^2C$ Slave mode, 7-bit address with Start and Stop bit interrupts enabled 1101 = Reserved 1100 = Reserved $1011 = I^2C$ firmware controlled Master mode (Slave idle) 1010 = SPI Master mode, clock = Fosc/(4 * (SSPxADD+1))⁽⁵⁾ 1001 = Reserved $1000 = I^2C$ Master mode, clock = Fosc/(4 * (SSPxADD+1))⁽⁴⁾ 0111 = I²C Slave mode, 10-bit address $0110 = I^2C$ Slave mode, 7-bit address 0101 = SPI Slave mode, clock = SCKx pin, SSx pin control disabled, SSx can be used as I/O pin 0100 = SPI Slave mode, clock = SCKx pin, SSx pin control enabled 0011 = SPI Master mode, clock = TMR2 output/2 0010 = SPI Master mode, clock = Fosc/64 0001 = SPI Master mode, clock = Fosc/16
 - 0000 = SPI Master mode, clock = Fosc/4
- **Note 1:** In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPxBUF register.
 - 2: When enabled, these pins must be properly configured as input or output.
 - 3: When enabled, the SDAx and SCLx pins must be configured as inputs.
 - 4: SSPxADD values of 0, 1 or 2 are not supported for I²C mode.
 - **5:** SSPxADD value of '0' is not supported. Use SSPM = 0000 instead.

	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
BAUD	Fosc	= 32.00	0 MHz	Foso	: = 20.00	0 MHz	Fosc	: = 18.43	2 MHz	Fosc	= 11.059	92 MHz
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	26666	300.0	0.00	16665	300.0	0.00	15359	300.0	0.00	9215
1200	1200	0.00	6666	1200	-0.01	4166	1200	0.00	3839	1200	0.00	2303
2400	2400	0.01	3332	2400	0.02	2082	2400	0.00	1919	2400	0.00	1151
9600	9604	0.04	832	9597	-0.03	520	9600	0.00	479	9600	0.00	287
10417	10417	0.00	767	10417	0.00	479	10425	0.08	441	10433	0.16	264
19.2k	19.18k	-0.08	416	19.23k	0.16	259	19.20k	0.00	239	19.20k	0.00	143
57.6k	57.55k	-0.08	138	57.47k	-0.22	86	57.60k	0.00	79	57.60k	0.00	47
115.2k	115.9k	0.64	68	116.3k	0.94	42	115.2k	0.00	39	115.2k	0.00	23

TABLE 21-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1												
BAUD	Fos	c = 8.000) MHz	Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fos	Fosc = 1.000 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	
300	300.0	0.00	6666	300.0	0.01	3332	300.0	0.00	3071	300.1	0.04	832	
1200	1200	-0.02	1666	1200	0.04	832	1200	0.00	767	1202	0.16	207	
2400	2401	0.04	832	2398	0.08	416	2400	0.00	383	2404	0.16	103	
9600	9615	0.16	207	9615	0.16	103	9600	0.00	95	9615	0.16	25	
10417	10417	0	191	10417	0.00	95	10473	0.53	87	10417	0.00	23	
19.2k	19.23k	0.16	103	19.23k	0.16	51	19.20k	0.00	47	19.23k	0.16	12	
57.6k	57.14k	-0.79	34	58.82k	2.12	16	57.60k	0.00	15	—	—	—	
115.2k	117.6k	2.12	16	111.1k	-3.55	8	115.2k	0.00	7	—	—	—	

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$					
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions	
		Program Memory Programming Specifications						
D110	VIHH	Voltage on MCLR/VPP pin	8.0	—	9.0	V	(Note 2)	
D111	IDDP	Supply Current during Programming	_	—	10	mA		
D112	VBE	VDD for Bulk Erase	2.7	—	VDDMAX	V		
D113	VPEW	VDD for Write or Row Erase	VDDMIN	—	VDDMAX	V		
D114	IPPPGM	Current on MCLR/VPP during Erase/Write	_	_	1.0	mA		
D115	IDDPGM	Current on VDD during Erase/Write	—	_	5.0	mA		
		Program Flash Memory						
D121	Eр	Cell Endurance	10K	_	_	E/W	-40°C to +85°C (Note 1)	
D122	VPRW	VDD for Read/Write	VDDMIN	—	VDDMAX	V		
D123	Tiw	Self-timed Write Cycle Time	_	2	2.5	ms		
D124	TRETD	Characteristic Retention	-	40	_	Year	Provided no other specifications are violated	
D125	EHEFC	High-Endurance Flash Cell	100K		_	E/W	0°C to +60°C, Lower byte, Last 128 Addresses in Flash Memory	

TABLE 25-5: MEMORY PROGRAMMING SPECIFICATIONS

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Self-write and Block Erase.

2: Required only if single-supply programming is disabled.



FIGURE 25-7: BROWN-OUT RESET TIMING AND CHARACTERISTICS



28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	N	IILLIMETER	S	
Dimensior	n Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	е		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	С	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	_	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5 Datums A & B to be determined at Datum H.

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40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Ν	ILLIMETER	S		
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	Ν		40		
Pitch	е		0.40 BSC		
Overall Height	Α	0.45	0.50	0.55	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3	0.127 REF			
Overall Width	E	5.00 BSC			
Exposed Pad Width	E2	3.60	3.70	3.80	
Overall Length	D		5.00 BSC		
Exposed Pad Length	D2	3.60	3.70	3.80	
Contact Width	b	0.15	0.20	0.25	
Contact Length	L	0.30	0.40	0.50	
Contact-to-Exposed Pad	ĸ	0.20	-	-	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-156A Sheet 2 of 2