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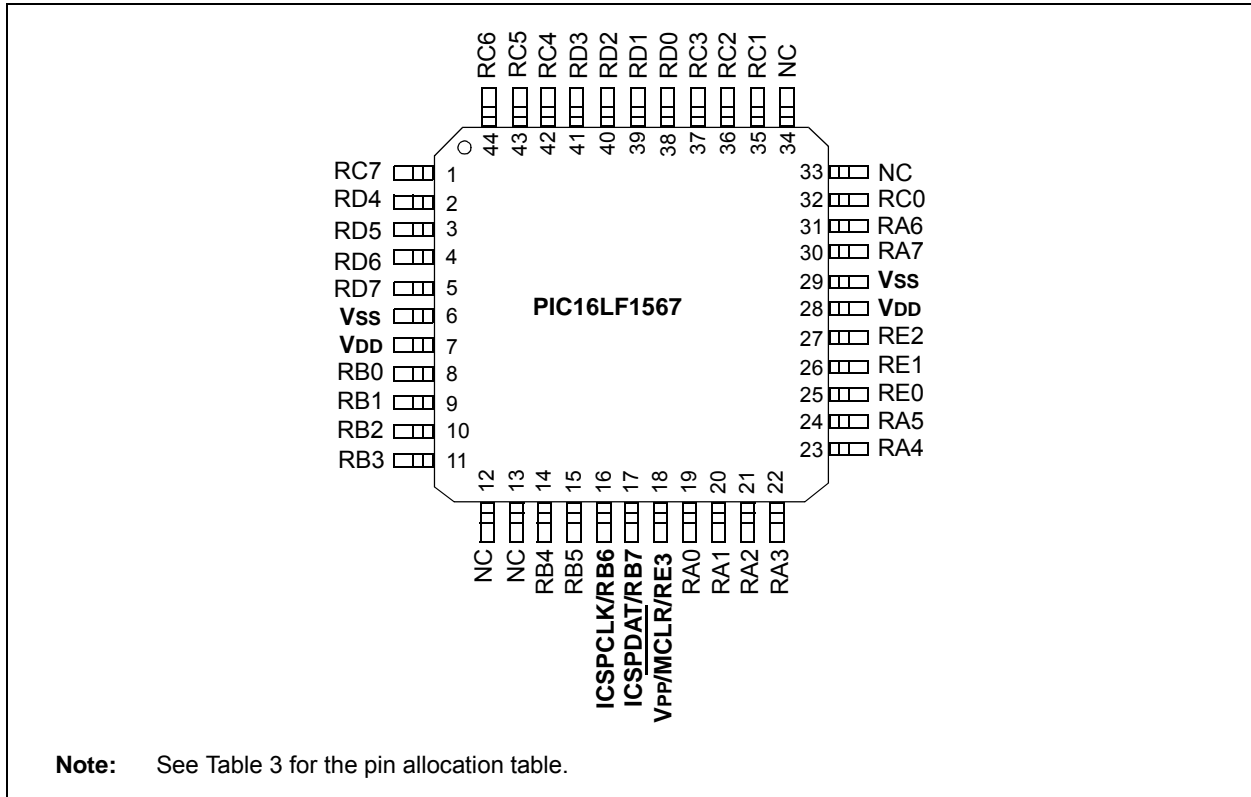
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 34x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1567t-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1567t-i-pt</a>

# PIC16LF1566/1567

**FIGURE 5: 44-PIN TQFP DIAGRAM FOR PIC16LF1567**



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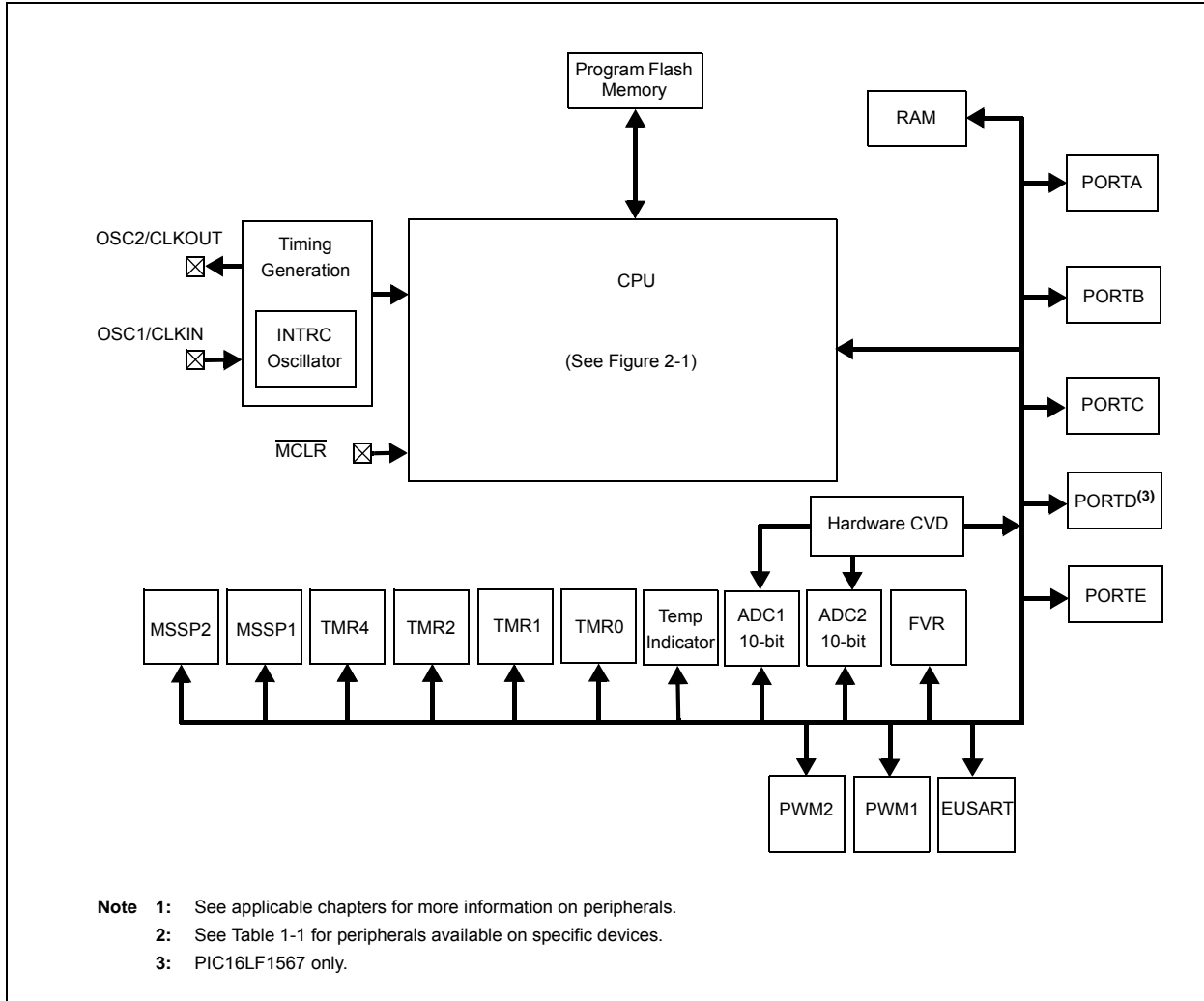
## PIN ALLOCATION TABLES

TABLE 2: 28-PIN ALLOCATION TABLE (PIC16LF1566)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin UQFN	Analog Channel	ADC and CVD	Timers	PWM	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	27	AN20	—	—	PWM10	—	SS1 <sup>(1)</sup>	—	—	—
RA1	3	28	AN10	—	—	PWM11	—	SS2	—	—	—
RA2	4	1	AN0	VREF-	—	PWM12	—	—	—	—	—
RA3	5	2	AN1	VREF+	—	PWM13	—	—	—	—	—
RA4	6	3	AN2	—	T0CKI	—	—	—	—	—	—
RA5	7	4	AN21	—	—	—	—	SS1 <sup>(1)</sup>	—	—	—
RA6	10	7	AN22	ADTRIG	—	—	—	—	—	—	CLKOUT
RA7	9	6	AN11	—	—	—	—	—	—	—	CLKIN
RB0	21	18	AN16	—	—	PWM20	—	—	INT IOC	Y	—
RB1	22	19	AN27	—	—	PWM21	—	—	IOC	Y	—
RB2	23	20	AN17	—	—	PWM22	—	—	IOC	Y	—
RB3	24	21	AN28	—	—	PWM23	—	—	IOC	Y	—
RB4	25	22	AN18	AD1GRDA <sup>(1)</sup> AD2GRDA <sup>(1)</sup>	—	—	—	—	IOC	Y	—
RB5	26	23	AN29	AD1GRDA <sup>(1)</sup> AD2GRDA <sup>(1)</sup>	T1G	—	—	—	IOC	Y	—
RB6	27	24	AN19	AD1GRDB <sup>(1)</sup> AD2GRDB <sup>(1)</sup>	—	—	—	—	IOC	Y	ICSPCLK ICDCLK
RB7	28	25	AN40	AD1GRDB <sup>(1)</sup> AD2GRDB <sup>(1)</sup>	—	—	—	—	IOC	Y	ICSPDAT ICDDAT
RC0	11	8	AN12	—	T1CKI	—	—	SDO2	—	—	—
RC1	12	9	AN23	—	—	PWM2	—	SCL2 SCK2	—	—	—
RC2	13	10	AN13	—	—	PWM1	—	SDA2 SDI2	—	—	—
RC3	14	11	AN24	—	—	—	—	SCL1 SCK1	—	—	—
RC4	15	12	AN14	—	—	—	—	SDA1 SDI1	—	—	—
RC5	16	13	AN25	—	—	—	—	SDO1 I <sup>2</sup> CLVL	—	—	—

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**FIGURE 1-1: PIC16LF1566/1567 BLOCK DIAGRAM<sup>(1,2)</sup>**



# PIC16LF1566/1567

**TABLE 3-11: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)**

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets	
<b>Banks 9-11</b>												
x00h/ x80h	INDF0 <sup>(1)</sup>	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu	
x00h/ x81h	INDF1 <sup>(1)</sup>	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu	
x02h/ x82h	PCL <sup>(1)</sup>	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000	
x03h/ x83h	STATUS <sup>(1)</sup>	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu	
x04h/ x84h	FSR0L <sup>(1)</sup>	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu	
x05h/ x85h	FSR0H <sup>(1)</sup>	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000	
x06h/ x86h	FSR1L <sup>(1)</sup>	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu	
x07h/ x87h	FSR1H <sup>(1)</sup>	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000	
x08h/ x88h	BSR <sup>(1)</sup>	—	—	—	BSR<4:0>				---0 0000	---0 0000		
x09h/ x89h	WREG <sup>(1)</sup>	Working Register								0000 0000	uuuu uuuu	
x0Ah/ x8Ah	PCLATH <sup>(1)</sup>	—	Write Buffer for the upper 7 bits of the Program Counter								-000 0000	-000 0000
x0Bh/ x8Bh	INTCON <sup>(1)</sup>	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 000u	
x0Ch/ x8Ch — x1Fh/ x9Fh	—	Unimplemented								—	—	

**Legend:** x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

- Note**
- 1: These registers can be accessed from any bank.
  - 2: PIC16LF1567.
  - 3: These registers/bits are available at two address locations, in Bank 1 and Bank 14.
  - 4: PIC16LF1566 only.
  - 5: Unimplemented, read as '1'.

## 5.4 Register Definitions: Oscillator Control

**REGISTER 5-1: OSCCON: OSCILLATOR CONTROL REGISTER**

R/W-0/0	R/W-0/0	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-0/0	R/W-0/0
SPLLEN	IRCF<3:0>			—	SCS<1:0>		
bit 7						bit 0	

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7      **SPLLEN:** Software PLL Enable bit  
 1 = 4x PLL is enabled  
 0 = 4x PLL is disabled
- bit 6-3    **IRCF<3:0>:** Internal Oscillator Frequency Select bits  
 1111 = 16 MHz  
 1110 = 8 MHz  
 1101 = 4 MHz  
 1100 = 2 MHz  
 1011 = 1 MHz  
 1010 = 500 kHz<sup>(1)</sup>  
 1001 = 250 kHz<sup>(1)</sup>  
 1000 = 125 kHz<sup>(1)</sup>  
 0111 = 500 kHz (default upon Reset)  
 0110 = 250 kHz  
 0101 = 125 kHz  
 0100 = 62.5 kHz  
 001x = 31.25 kHz  
 000x = 31 kHz (LFINTOSC)
- bit 2      **Unimplemented:** Read as '0'
- bit 1-0    **SCS<1:0>:** System Clock Select bits  
 1x = Internal oscillator block  
 01 = Reserved  
 00 = Clock determined by FOSC<1:0> in Configuration Words

**Note 1:** Duplicate frequency derived from HFINTOSC.

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## 10.6 Register Definitions: Flash Program Memory Control

### REGISTER 10-1: PMDATL: PROGRAM MEMORY DATA LOW BYTE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PMDAT<7:0>							
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                  x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                          '0' = Bit is cleared

bit 7-0                      **PMDAT<7:0>**: Read/write value for Least Significant bits of program memory

### REGISTER 10-2: PMDATH: PROGRAM MEMORY DATA HIGH BYTE REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	PMDAT<13:8>					
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                  x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                          '0' = Bit is cleared

bit 7-6                      **Unimplemented**: Read as '0'

bit 5-0                      **PMDAT<13:8>**: Read/write value for Most Significant bits of program memory

## 12.6 Register Definitions: Interrupt-on-Change Control

**REGISTER 12-1: IOCBP: INTERRUPT-ON-CHANGE PORTB POSITIVE EDGE REGISTER**

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0
bit 7							bit 0

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0      **IOCBP<7:0>:** Interrupt-on-Change PORTB Positive Edge Enable bits  
 1 = Interrupt-on-Change enabled on the pin for a positive-going edge. IOCBFx bit and IOCIF flag will be set upon detecting an edge.  
 0 = Interrupt-on-Change disabled for the associated pin.

**REGISTER 12-2: IOCBN: INTERRUPT-ON-CHANGE PORTB NEGATIVE EDGE REGISTER**

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0
bit 7							bit 0

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0      **IOCBN<7:0>:** Interrupt-on-Change PORTB Negative Edge Enable bits  
 1 = Interrupt-on-Change enabled on the pin for a negative-going edge. IOCBFx bit and IOCIF flag will be set upon detecting an edge.  
 0 = Interrupt-on-Change disabled for the associated pin.

**REGISTER 12-3: IOCBF: INTERRUPT-ON-CHANGE PORTB FLAG REGISTER**

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0
bit 7							bit 0

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-0      **IOCBF<7:0>:** Interrupt-on-Change PORTB Flag bits  
 1 = An enabled change was detected on the associated pin.  
     Set when IOCBPx = 1 and a rising edge was detected on RBx, or when IOCBNx = 1 and a falling edge was detected on RBx.  
 0 = No change was detected, or the user cleared the detected change.



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## REGISTER 16-7: ADxCON2: ADC CONTROL REGISTER 2<sup>(1)</sup>

U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
—	TRIGSEL<2:0>			—	—	—	—
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7            **Unimplemented:** Read as '0'

bit 6-4        **TRIGSEL<2:0>:** Auto-Conversion Trigger Selection bits

111 = ADTRIG Falling Edge

110 = ADTRIG Rising Edge

101 = TMR2 match to PR2<sup>(1)</sup>

100 = Timer1 Overflow<sup>(1)</sup>

011 = Timer0 Overflow<sup>(1)</sup>

010 = TMR4 match to PR4

001 = Reserved

000 = No Auto Conversion Trigger selected

bit 3-0        **Unimplemented:** Read as '0'

**Note 1:** Signal also sets its corresponding interrupt flag.

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## 18.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

## 18.4 Timer1 Operation in Asynchronous Counter Mode

If control bit  $\overline{T1SYNC}$  of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see Section 18.4.1 “Reading and Writing Timer1 in Asynchronous Counter Mode”).

**Note:** When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

### 18.4.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

## 18.5 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 Gate Enable.

Timer1 gate can also be driven by multiple selectable sources.

### 18.5.1 TIMER1 GATE ENABLE

The Timer1 Gate Enable mode is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 Gate Enable mode is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate Enable mode is enabled, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate Enable mode is disabled, no incrementing will occur and Timer1 will hold the current count. See Figure 18-3 for timing details.

**TABLE 18-3: TIMER1 GATE ENABLE SELECTIONS**

T1CLK	T1GPOL	T1G	Timer1 Operation
↑	0	0	Counts
↑	0	1	Holds Count
↑	1	0	Holds Count
↑	1	1	Counts

### 18.5.2 TIMER1 GATE SOURCE SELECTION

Timer1 gate source selections are shown in Table 18-4. Source selection is controlled by the T1GSS bit of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPOL bit of the T1GCON register.

**TABLE 18-4: TIMER1 GATE SOURCES**

T1GSS	Timer1 Gate Source
0	Timer1 Gate pin (T1G)
1	Overflow of Timer0 (T0_overflow) (TMR0 increments from FFh to 00h)

## 18.5.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

## 18.5.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

## 18.5.3 TIMER1 GATE TOGGLE MODE

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal, as opposed to the duration of a single level pulse.

The Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 18-4 for timing details.

Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When the T1GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

<b>Note:</b> Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.
---

## 18.5.4 TIMER1 GATE SINGLE-PULSE MODE

When Timer1 Gate Single-Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer1 Gate Single-Pulse mode is first enabled by setting the T1GSPM bit in the T1GCON register. Next, the T1GGO/DONE bit in the T1GCON register must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T1GGO/DONE bit will automatically be cleared. No other gate events will be allowed to increment Timer1 until the T1GGO/DONE bit is once again set in software. See Figure 18-5 for timing details.

If the Single Pulse Gate mode is disabled by clearing the T1GSPM bit in the T1GCON register, the T1GGO/DONE bit should also be cleared.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1 gate source to be measured. See Figure 18-6 for timing details.

## 18.5.5 TIMER1 GATE VALUE STATUS

When Timer1 Gate Value Status is utilized, it is possible to read the most current level of the gate control value. The value is stored in the T1GVAL bit in the T1GCON register. The T1GVAL bit is valid even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

## 18.5.6 TIMER1 GATE EVENT INTERRUPT

When Timer1 Gate Event Interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of T1GVAL occurs, the TMR1GIF flag bit in the PIR1 register will be set. If the TMR1GIE bit in the PIE1 register is set, then an interrupt will be recognized.

The TMR1GIF flag bit operates even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

## 20.4.5 START CONDITION

The I<sup>2</sup>C specification defines a Start condition as a transition of SDAx from a high to a low state while SCLx line is high. A Start condition is always generated by the master and signifies the transition of the bus from an Idle to an Active state. Figure 20-12 shows wave forms for Start and Stop conditions.

A bus collision can occur on a Start condition if the module samples the SDAx line low before asserting it low. This does not conform to the I<sup>2</sup>C Specification that states no bus collision can occur on a Start.

## 20.4.6 STOP CONDITION

A Stop condition is a transition of the SDAx line from low-to-high state while the SCLx line is high.

**Note:** At least one SCLx low time must appear before a Stop is valid, therefore, if the SDAx line goes low then high again while the SCLx line stays high, only the Start condition is detected.

## 20.4.7 RESTART CONDITION

A Restart is valid any time that a Stop would be valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave. Figure 20-13 shows the wave form for a Restart condition.

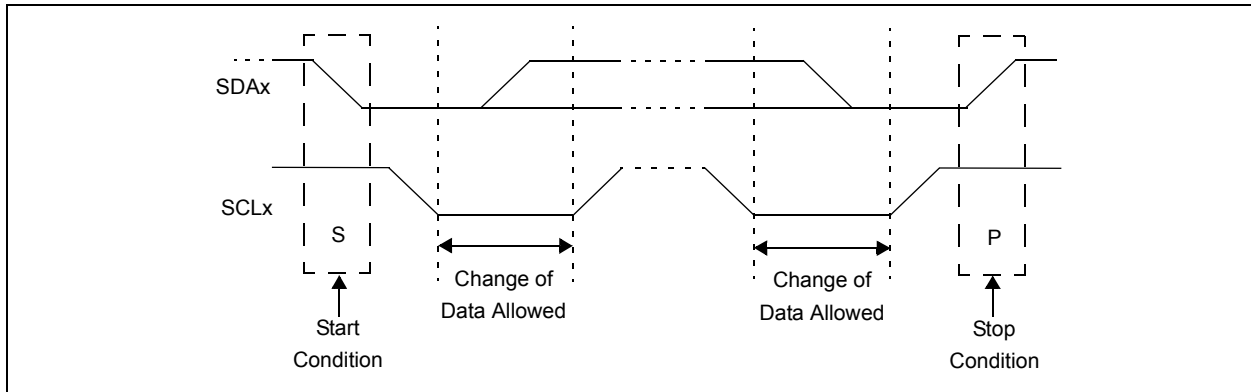
In 10-bit Addressing Slave mode a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes, the master can issue a Restart and the high address byte with the R/W bit set. The slave logic will then hold the clock and prepare to clock out data.

After a full match with R/W clear in 10-bit mode, a prior match flag is set and maintained. Until a Stop condition, a high address with R/W clear, or high address match fails.

## 20.4.8 START/STOP CONDITION INTERRUPT MASKING

The SCIE and PCIE bits of the SSPxCON3 register can enable the generation of an interrupt in Slave modes that do not typically support this function. Slave modes where interrupt on Start and Stop detect are already enabled, these bits will have no effect.

**FIGURE 20-12: I<sup>2</sup>C START AND STOP CONDITIONS**



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## 20.5.2 SLAVE RECEPTION

When the  $\overline{R/W}$  bit of a matching received address byte is clear, the  $\overline{R/W}$  bit of the SSPxSTAT register is cleared. The received address is loaded into the SSPxBUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF of the SSPxSTAT register is set, or bit SSPOV of the SSPxCON1 register is set. The BOEN bit of the SSPxCON3 register modifies this operation. For more information see Register 20-4.

An MSSPx interrupt is generated for each transferred data byte. Flag bit, SSPxIF, must be cleared by software.

When the SEN bit of the SSPxCON2 register is set, SCLx will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit of the SSPxCON1 register, except sometimes in 10-bit mode. See **Section 20.2.3 “SPI Master Mode”** for more detail.

### 20.5.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSPx module configured as an I<sup>2</sup>C slave in 7-bit Addressing mode. Figure 20-14 and Figure 20-15 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I<sup>2</sup>C communication.

1. Start bit detected.
2. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
3. Matching address with  $\overline{R/W}$  bit clear is received.
4. The slave pulls SDAx low sending an  $\overline{ACK}$  to the master, and sets SSPxIF bit.
5. Software clears the SSPxIF bit.
6. Software reads received address from SSPxBUF clearing the BF flag.
7. If SEN = 1; Slave software sets CKP bit to release the SCLx line.
8. The master clocks out a data byte.
9. Slave drives SDAx low sending an  $\overline{ACK}$  to the master, and sets SSPxIF bit.
10. Software clears SSPxIF.
11. Software reads the received byte from SSPxBUF clearing BF.
12. Steps 8-12 are repeated for all received bytes from the master.
13. Master sends Stop condition, setting P bit of SSPxSTAT, and the bus goes idle.

### 20.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the eighth falling edge of SCLx. These additional interrupts allow the slave software to decide whether it wants to  $\overline{ACK}$  the receive address or data byte, rather than the hardware. This functionality adds support for PMBus™ that was not present on previous versions of this module.

This list describes the steps that need to be taken by slave software to use these options for I<sup>2</sup>C communication. Figure 20-16 displays a module using both address and data holding. Figure 20-17 includes the operation with the SEN bit of the SSPxCON2 register set.

1. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
2. Matching address with  $\overline{R/W}$  bit clear is clocked in. SSPxIF is set and CKP cleared after the eighth falling edge of SCLx.
3. Slave clears the SSPxIF.
4. Slave can look at the ACKTIM bit of the SSPxCON3 register to determine if the SSPxIF was after or before the  $\overline{ACK}$ .
5. Slave reads the address value from SSPxBUF, clearing the BF flag.
6. Slave sets  $\overline{ACK}$  value clocked out to the master by setting ACKDT.
7. Slave releases the clock by setting CKP.
8. SSPxIF is set after an  $\overline{ACK}$ , not after a NACK.
9. If SEN = 1 the slave hardware will stretch the clock after the  $\overline{ACK}$ .
10. Slave clears SSPxIF.

**Note:** SSPxIF is still set after the ninth falling edge of SCLx even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSPxIF not set

11. SSPxIF set and CKP cleared after eighth falling edge of SCLx for a received data byte.
12. Slave looks at ACKTIM bit of SSPxCON3 to determine the source of the interrupt.
13. Slave reads the received data from SSPxBUF clearing BF.
14. Steps 7-14 are the same for each received data byte.
15. Communication is ended by either the slave sending an  $\overline{ACK} = 1$ , or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSTAT register.

## 20.5.3.3 7-bit Transmission with Address Hold Enabled

Setting the AHEN bit of the SSPxCON3 register enables additional clock stretching and interrupt generation after the eighth falling edge of a received address. Once a matching address has been clocked in, CKP is cleared and the SSPxIF interrupt is set.

Figure 20-19 displays a standard waveform of a 7-bit Address Slave Transmission with AHEN enabled.

1. Bus starts Idle.
2. Master sends Start condition; the S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
3. Master sends matching address with  $\overline{R/\overline{W}}$  bit set. After the eighth falling edge of the SCLx line the CKP bit is cleared and SSPxIF interrupt is generated.
4. Slave software clears SSPxIF.
5. Slave software reads the  $\overline{ACKTIM}$  bit of SSPxCON3 register, and  $\overline{R/\overline{W}}$  and  $\overline{D/\overline{A}}$  of the SSPxSTAT register to determine the source of the interrupt.
6. Slave reads the address value from the SSPxBUF register clearing the BF bit.
7. Slave software decides from this information if it wishes to  $\overline{ACK}$  or not  $\overline{ACK}$  and sets the ACKDT bit of the SSPxCON2 register accordingly.
8. Slave sets the CKP bit releasing SCLx.
9. Master clocks in the  $\overline{ACK}$  value from the slave.
10. Slave hardware automatically clears the CKP bit and sets SSPxIF after the  $\overline{ACK}$  if the  $\overline{R/\overline{W}}$  bit is set.
11. Slave software clears SSPxIF.
12. Slave loads value to transmit to the master into SSPxBUF setting the BF bit.

**Note:** SSPxBUF cannot be loaded until after the  $\overline{ACK}$ .

13. Slave sets CKP bit releasing the clock.
14. Master clocks out the data from the slave and sends an  $\overline{ACK}$  value on the ninth SCLx pulse.
15. Slave hardware copies the  $\overline{ACK}$  value into the ACKSTAT bit of the SSPxCON2 register.
16. Steps 10-15 are repeated for each byte transmitted to the master from the slave.
17. If the master sends a not  $\overline{ACK}$  the slave releases the bus allowing the master to send a Stop and end the communication.

**Note:** Master must send a not  $\overline{ACK}$  on the last byte to ensure that the slave releases the SCLx line to receive a Stop.

## 20.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCLx line low effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCLx.

The CKP bit of the SSPxCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCLx line to go low and then hold it. Setting CKP will release SCLx and allow more communication.

### 20.5.6.1 Normal Clock Stretching

Following an  $\overline{\text{ACK}}$  if the R/W bit of SSPxSTAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPxBUF with data to transfer to the master. If the SEN bit of SSPxCON2 is set, the slave hardware will always stretch the clock after the  $\overline{\text{ACK}}$  sequence. Once the slave is ready; CKP is set by software and communication resumes.

- Note 1:** The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSPxBUF was read before the ninth falling edge of SCLx.
- 2:** Previous versions of the module did not stretch the clock for a transmission if SSPxBUF was loaded before the ninth falling edge of SCLx. It is now always cleared for read requests.

### 20.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set, the clock is always stretched. This is the only time the SCLx is stretched without CKP being cleared. SCLx is released immediately after a write to SSPxADD.

**Note:** Previous versions of the module did not stretch the clock if the second address byte did not match.

### 20.5.6.3 Byte NACKing

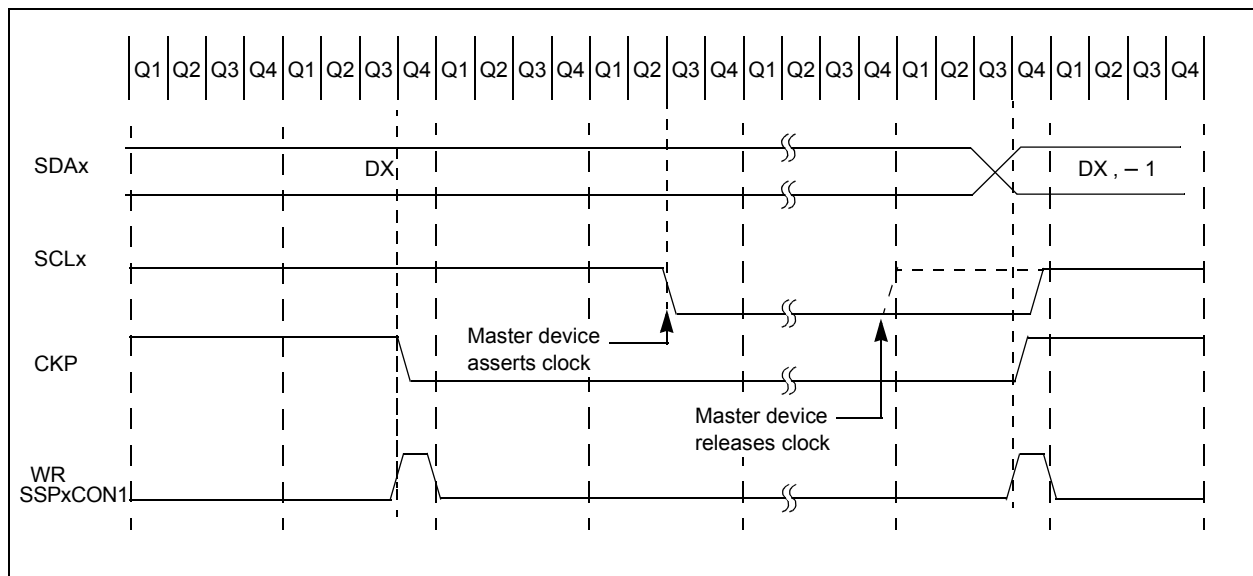
When the AHEN bit of SSPxCON3 is set; CKP is cleared by hardware after the eighth falling edge of SCLx for a received matching address byte. When the DHEN bit of SSPxCON3 is set; CKP is cleared after the eighth falling edge of SCLx for received data.

Stretching after the eighth falling edge of SCLx allows the slave to look at the received address or data and decide if it wants to ACK the received data.

## 20.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCLx line to go low and then hold it. However, clearing the CKP bit will not assert the SCLx output low until the SCLx output is already sampled low. Therefore, the CKP bit will not assert the SCLx line until an external I<sup>2</sup>C master device has already asserted the SCLx line. The SCLx output will remain low until the CKP bit is set and all other devices on the I<sup>2</sup>C bus have released SCLx. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCLx (see Figure 20-23).

**FIGURE 20-23: CLOCK SYNCHRONIZATION TIMING**



## 20.6.7 I<sup>2</sup>C MASTER MODE RECEPTION

Master mode reception (Figure 20-29) is enabled by programming the Receive Enable bit, RCEN bit of the SSPxCON2 register.

**Note:** The MSSPx module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCLx pin changes (high-to-low/low-to-high) and data is shifted into the SSPxSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPxSR are loaded into the SSPxBUF, the BF flag bit is set, the SSPxIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCLx low. The MSSPx is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPxCON2 register.

### 20.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPxBUF from SSPxSR. It is cleared when the SSPxBUF register is read.

### 20.6.7.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when eight bits are received into the SSPxSR and the BF flag bit is already set from a previous reception.

### 20.6.7.3 WCOL Status Flag

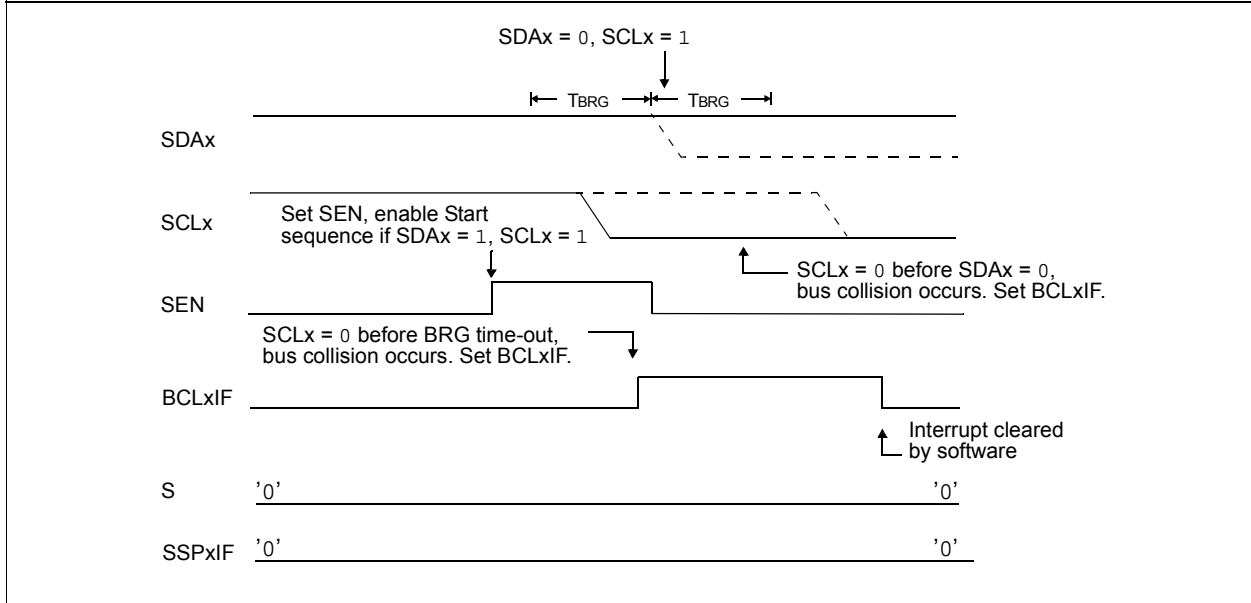
If the user writes the SSPxBUF when a receive is already in progress (i.e., SSPxSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

### 20.6.7.4 Typical Receive Sequence:

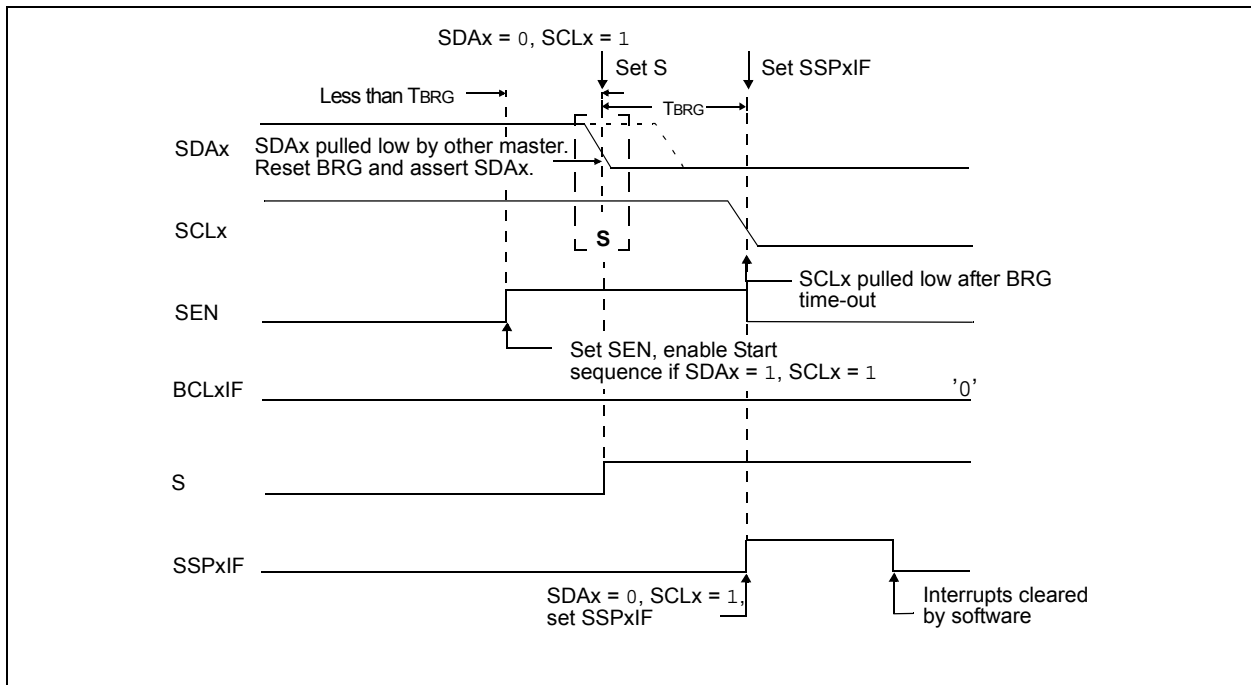
1. The user generates a Start condition by setting the SEN bit of the SSPxCON2 register.
2. SSPxIF is set by hardware on completion of the Start.
3. SSPxIF is cleared by software.
4. User writes SSPxBUF with the slave address to transmit and the R/W bit set.
5. Address is shifted out the SDAx pin until all eight bits are transmitted. Transmission begins as soon as SSPxBUF is written to.
6. The MSSPx module shifts in the  $\overline{\text{ACK}}$  bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
7. The MSSPx module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
8. User sets the RCEN bit of the SSPxCON2 register and the master clocks in a byte from the slave.
9. After the eighth falling edge of SCLx, SSPxIF and BF are set.
10. Master clears SSPxIF and reads the received byte from SSPxUF, clears BF.
11. Master sets  $\overline{\text{ACK}}$  value sent to slave in ACKDT bit of the SSPxCON2 register and initiates the  $\overline{\text{ACK}}$  by setting the ACKEN bit.
12. Masters  $\overline{\text{ACK}}$  is clocked out to the slave and SSPxIF is set.
13. User clears SSPxIF.
14. Steps 8-13 are repeated for each received byte from the slave.
15. Master sends a not  $\overline{\text{ACK}}$  or Stop to end communication.



**FIGURE 20-34: BUS COLLISION DURING START CONDITION (SCLX = 0)**



**FIGURE 20-35: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION**



## 25.3 DC Characteristics

**TABLE 25-1: SUPPLY VOLTAGE**

PIC16LF1566/1567		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
D001	VDD	Supply Voltage (VDDMIN, VDDMAX)	1.8	—	3.6	V	Fosc ≤ 16 MHz: Fosc ≤ 32 MHz
			2.5	—	3.6	V	
D002*	VDR	RAM Data Retention Voltage <sup>(1)</sup>	1.5	—	—	V	Device in Sleep mode
D002A*	VPOR*	Power-on Reset Release Voltage	—	1.6	—	V	
D002B*	VPORR*	Power-on Reset Rearm Voltage	—	0.8	—	V	
D003	VADFVR	Fixed Voltage Reference Voltage for ADC, Initial Accuracy	-7	—	6	%	1.024V, VDD ≥ 2.5V, 85°C (Note 2) 1.024V, VDD ≥ 2.5V, 125°C (Note 2) 2.048V, VDD ≥ 2.5V, 85°C 2.048V, VDD ≥ 2.5V, 125°C
			-8	—	6		
			-7	—	6		
			-8	—	6		
D003C*	TCVFVR	Temperature Coefficient, Fixed Voltage Reference	—	-130	—	ppm/°C	
D003D*	$\frac{\Delta V_{FVR}}{\Delta V_{IN}}$	Line Regulation, Fixed Voltage Reference	—	0.270	—	%/V	
D004*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See Section 6.1 “Power-on Reset (POR)” for details.
D005*	VI <sup>2</sup> CLVL	I <sup>2</sup> CLVL Voltage	TBD	—	VDD	V	—

\* These parameters are characterized but not tested.

† Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.
- Note 2:** For proper operation, the minimum value of the ADC positive voltage reference must be 1.8V or greater. When selecting the FVR or the VREF+ pin as the source of the ADC positive voltage reference, be aware that the voltage must be 1.8V or greater.

**TABLE 25-6: THERMAL CHARACTERISTICS**

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$					
Param. No.	Sym.	Characteristic	Typ.	Units	Conditions
TH01	$\theta_{JA}$	Thermal Resistance Junction to Ambient	60.0	$^{\circ}\text{C}/\text{W}$	28-pin SPDIP package
			80.3	$^{\circ}\text{C}/\text{W}$	28-pin SOIC package
			90.0	$^{\circ}\text{C}/\text{W}$	28-pin SSOP package
			48.0	$^{\circ}\text{C}/\text{W}$	28-pin UQFN (4x4 mm) package
			47.2	$^{\circ}\text{C}/\text{W}$	40-pin PDIP package
			46.0	$^{\circ}\text{C}/\text{W}$	44-pin TQFP package
			41.0	$^{\circ}\text{C}/\text{W}$	40-pin UQFN (5x5 mm) package
TH02	$\theta_{JC}$	Thermal Resistance Junction to Case	31.4	$^{\circ}\text{C}/\text{W}$	28-pin SPDIP package
			24.0	$^{\circ}\text{C}/\text{W}$	28-pin SOIC package
			24.0	$^{\circ}\text{C}/\text{W}$	28-pin SSOP package
			12.0	$^{\circ}\text{C}/\text{W}$	28-pin UQFN (4x4 mm) package
			24.7	$^{\circ}\text{C}/\text{W}$	40-pin PDIP package
			14.5	$^{\circ}\text{C}/\text{W}$	44-pin TQFP package
			50.5	$^{\circ}\text{C}/\text{W}$	40-pin UQFN (5x5 mm) package
TH03	$T_{JMAX}$	Maximum Junction Temperature	150	$^{\circ}\text{C}$	
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}^{(1)}$
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \sum (I_{OL} * V_{OL}) + \sum (I_{OH} * (V_{DD} - V_{OH}))$
TH07	$P_{DER}$	Derated Power	—	W	$P_{DER} = P_{D_{MAX}} (T_J - T_A) / \theta_{JA}^{(2)}$

**Note 1:**  $I_{DD}$  is current to run the chip alone without driving any load on the output pins.

**2:**  $T_A$  = Ambient Temperature;  $T_J$  = Junction Temperature.

# PIC16LF1566/1567

## 25.4 AC Characteristics

Timing Parameter Symbolology has been created with one of the following formats:

1. TppS2ppS
2. TppS

<b>T</b>			
F	Frequency	T	Time

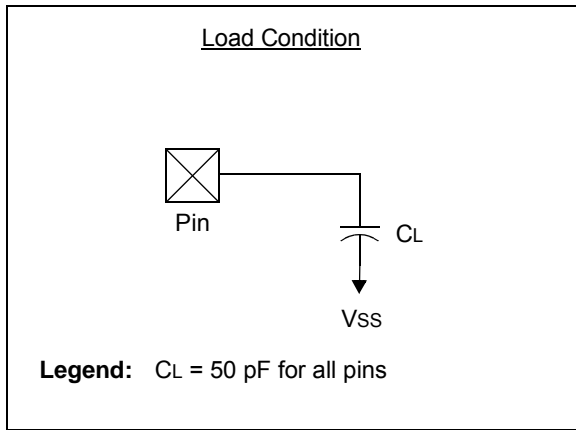
Lowercase letters (pp) and their meanings:

<b>pp</b>			
cc	CCP1	osc	CLKIN
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDIx	sc	SCKx
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O PORT	t1	T1CKI
mc	MCLR	wr	$\overline{WR}$

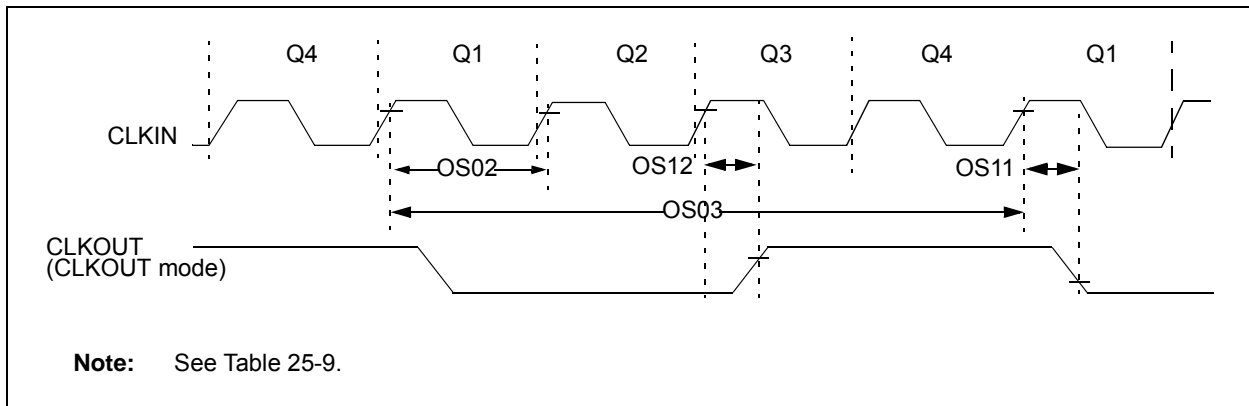
Uppercase letters and their meanings:

<b>S</b>			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

**FIGURE 25-3: LOAD CONDITIONS**



**FIGURE 25-4: CLOCK TIMING**



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