Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFBGA, CSPBGA
Supplier Device Package	36-CSP (3.02x2.89)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg350f32g-b-csp36

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG350 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32HG350F32G-B-CSP36	32	8	25	1.98 - 3.8	-40 - 85	CSP36
EFM32HG350F64G-B-CSP36	64	8	25	1.98 - 3.8	-40 - 85	CSP36

Adding the suffix 'R' to the part number (e.g. EFM32HG350F32G-B-CSP36R) denotes tape and reel.

Visit **www.silabs.com** for information on global distributors and representatives.

2.1.20 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 3 external pins and 6 internal signals.

2.1.21 Current Digital to Analog Converter (IDAC)

The current digital to analog converter can source or sink a configurable constant current, which can be output on, or sinked from pin or ADC. The current is configurable with several ranges of various step sizes.

2.1.22 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.23 General Purpose Input/Output (GPIO)

In the EFM32HG350, there are 22 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 10 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32HG350 is a subset of the feature set described in the EFM32HG Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO,
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
USB	Full configuration	USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA and I2S	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration with I2S and IrDA	US1_TX, US1_RX, US1_CLK, US1_CS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		194	208	µA/ MHz
I_{EM1}	EM1 current	24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		64	68	µA/ MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		67	71	µA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		85	91	µA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		86	92	µA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		51	55	µA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		52	56	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		53	57	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		54	58	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		56	59	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		57	61	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		58	61	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		59	63	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		64	68	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		67	71	µA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		106	114	µA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		114	126	µA/ MHz
I_{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768		0.9	1.35	µA

Figure 3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz

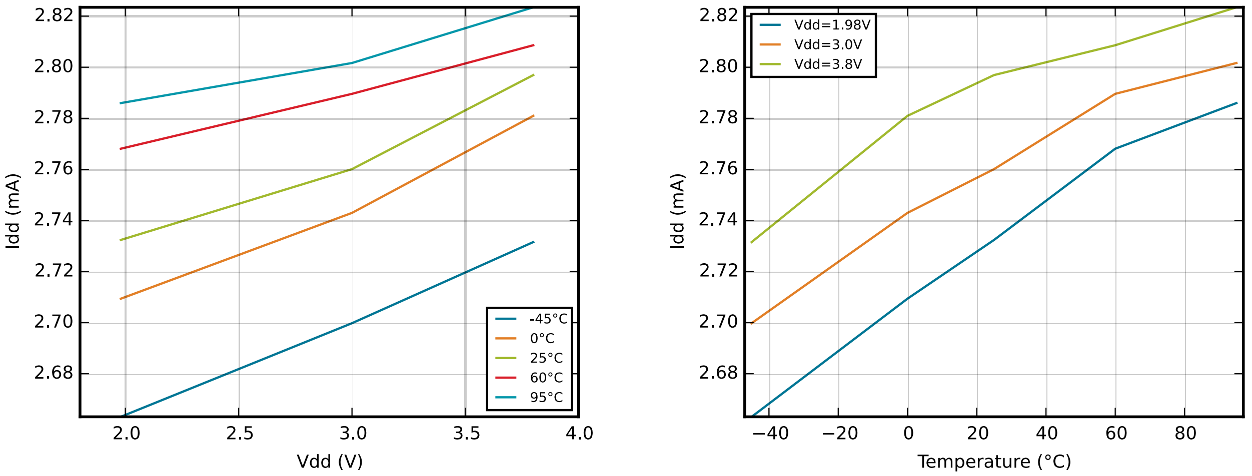


Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz

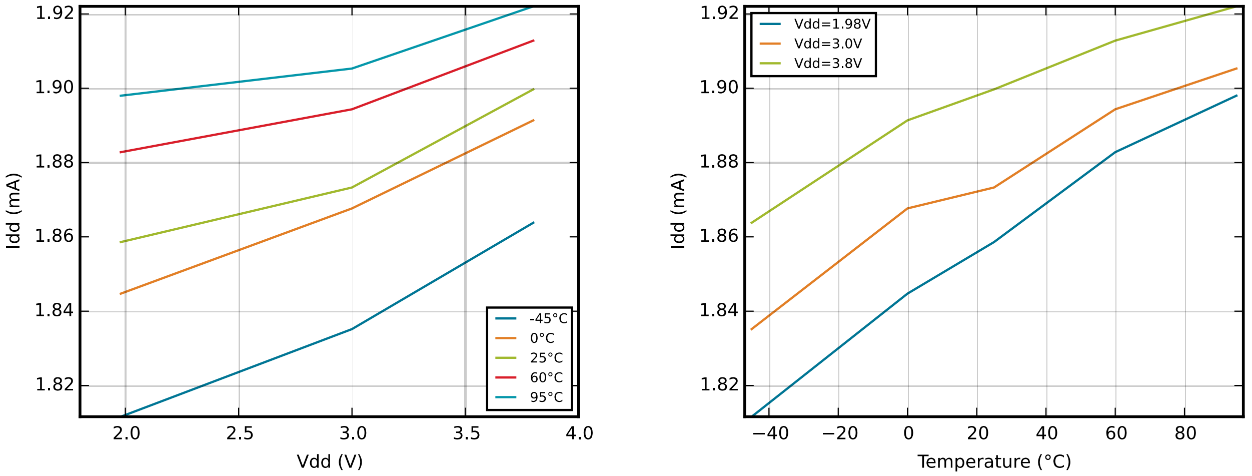


Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz

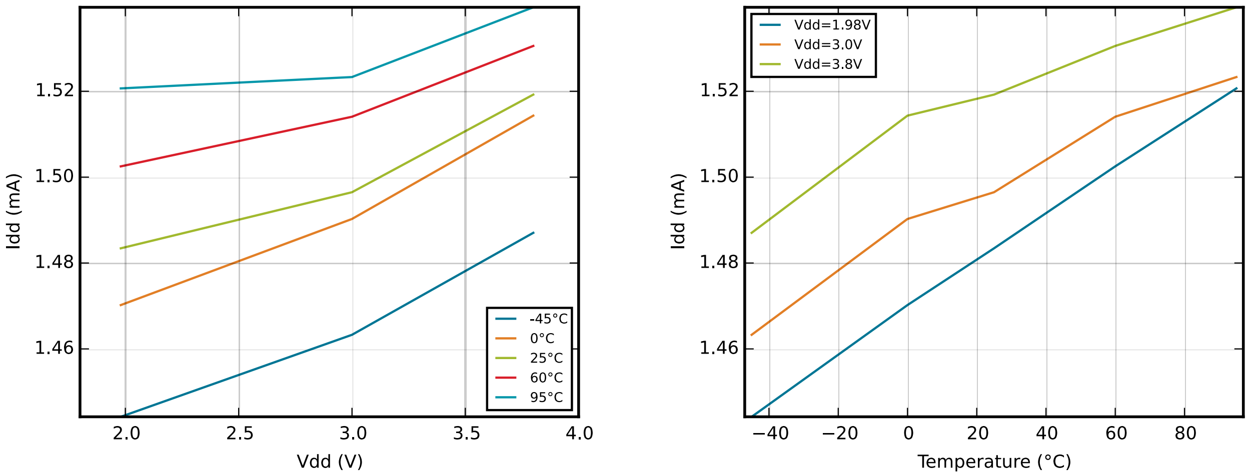
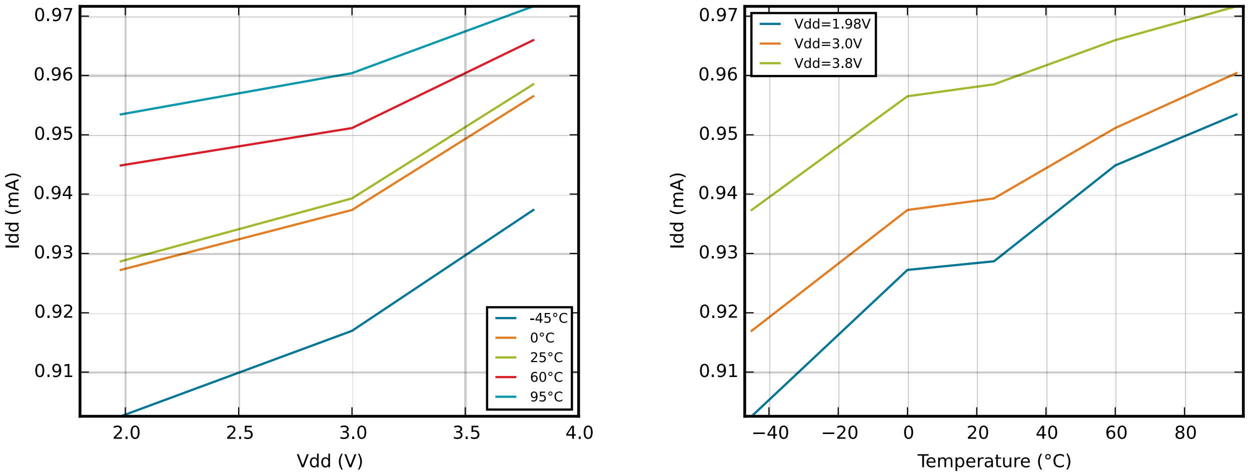


Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 6.6 MHz



3.4.2 EM1 Current Consumption

Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 24 MHz

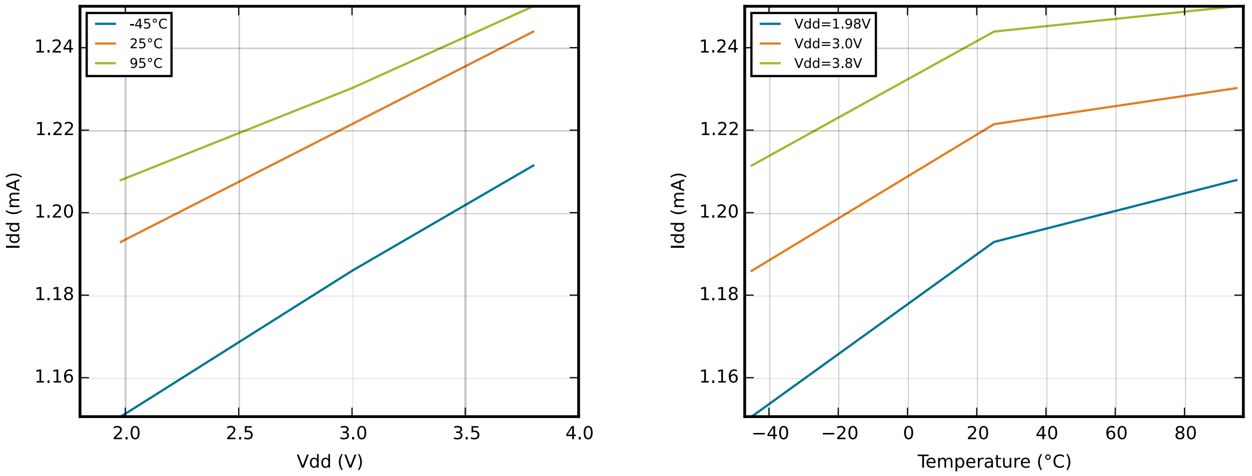


Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz

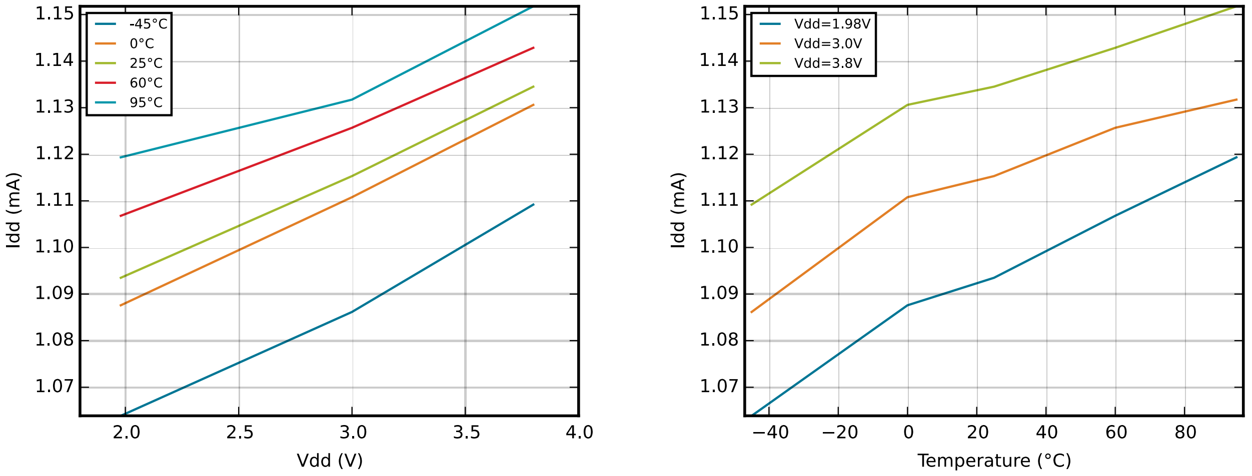
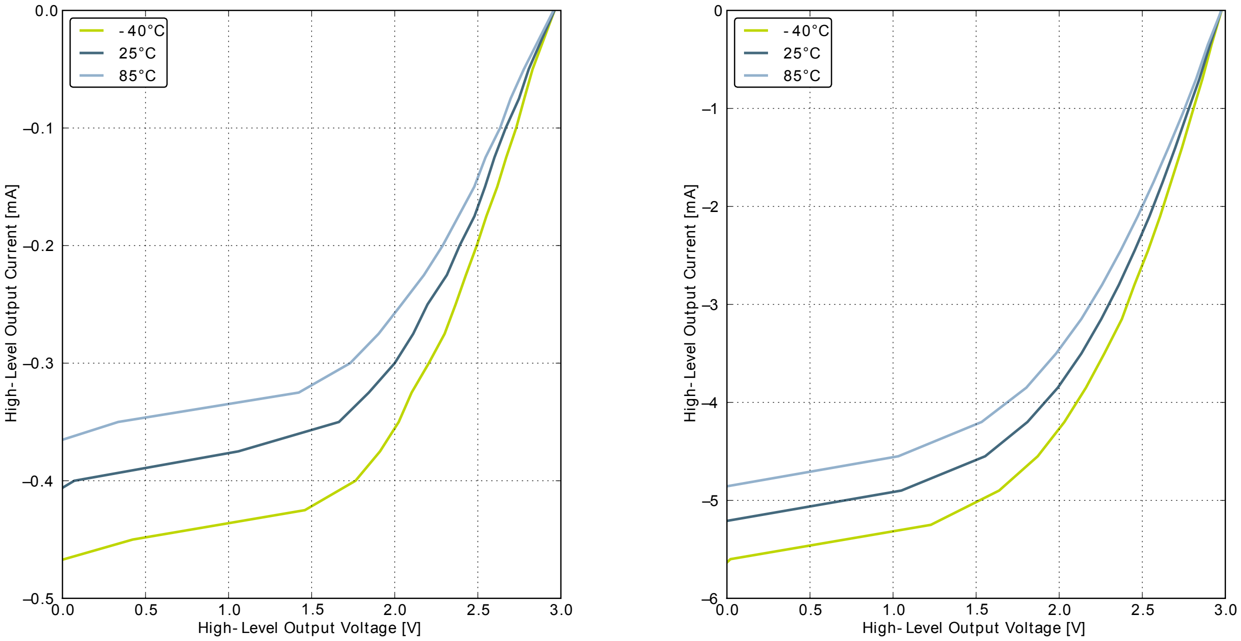
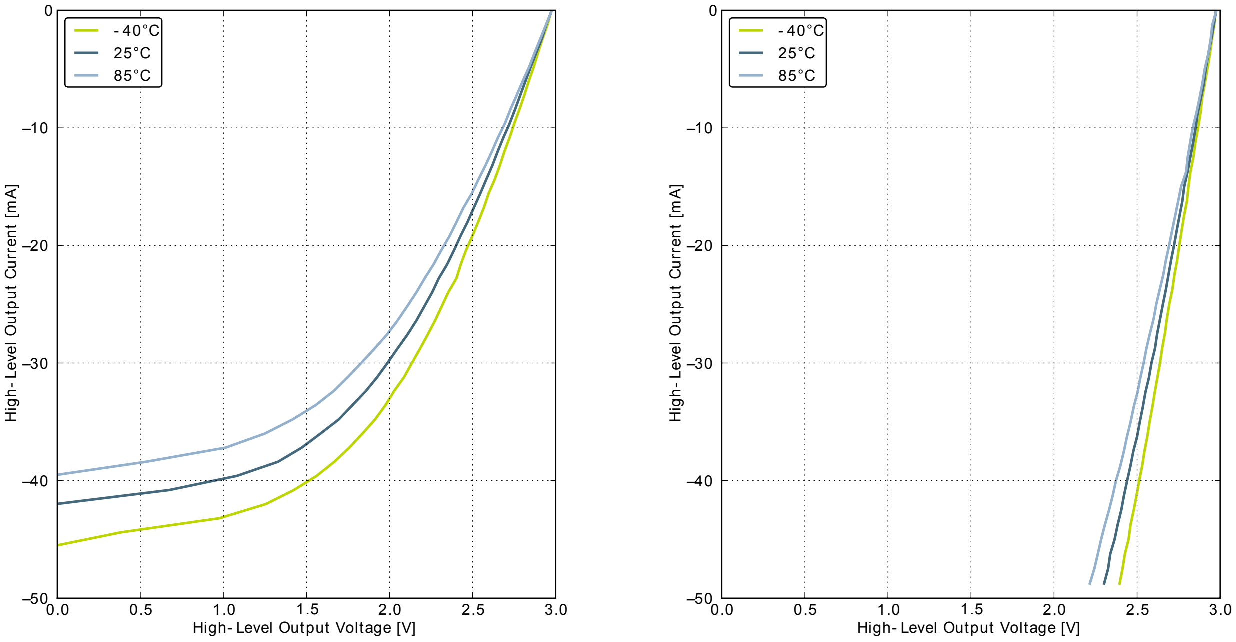


Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

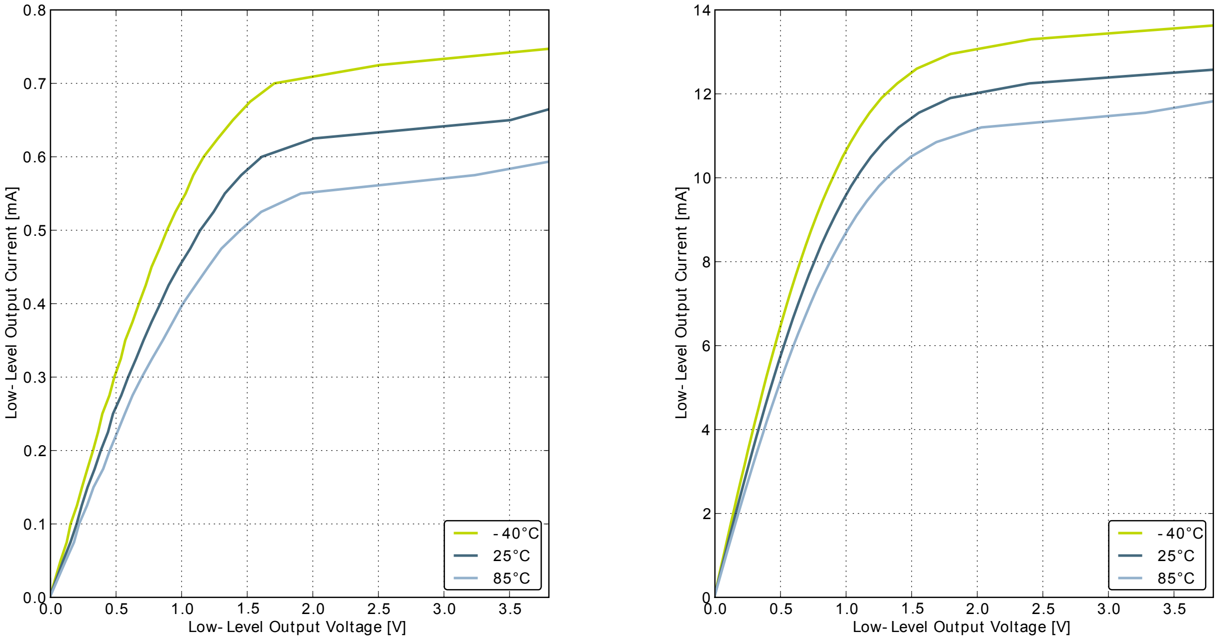
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

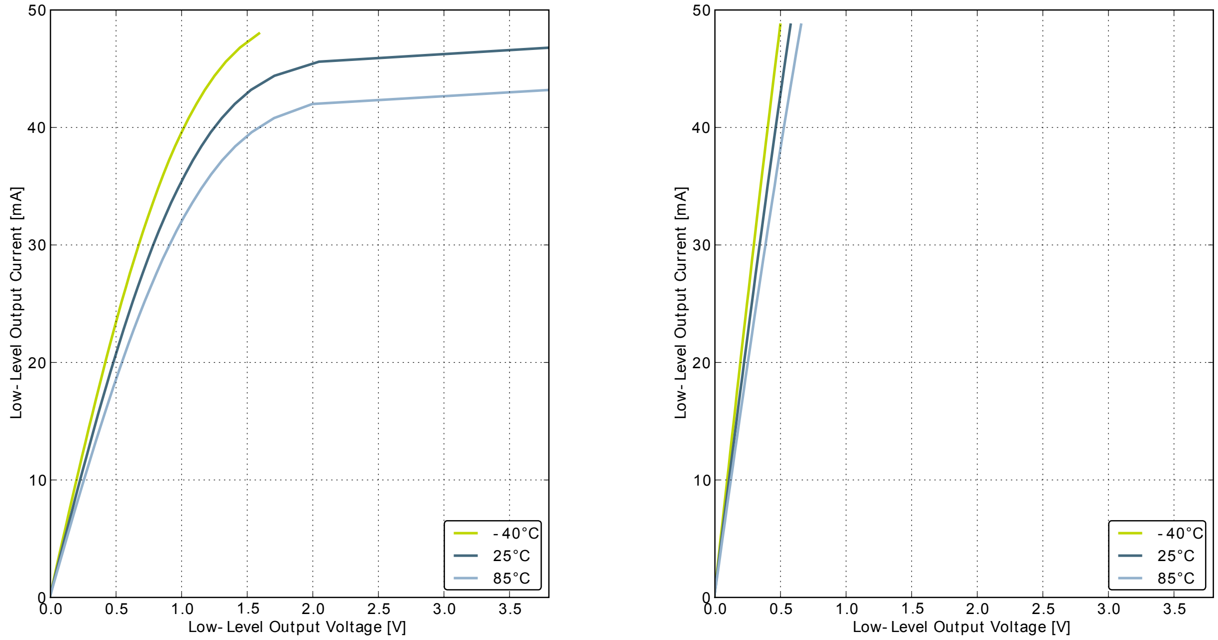
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

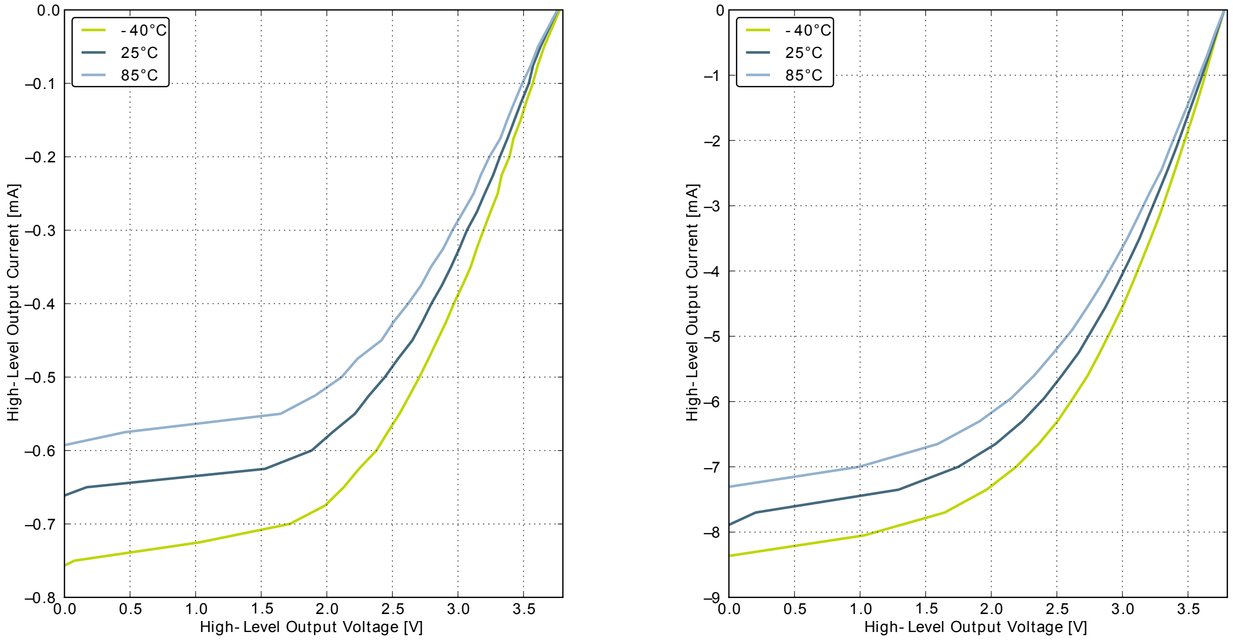
GPIO_Px_CTRL DRIVEMODE = LOW



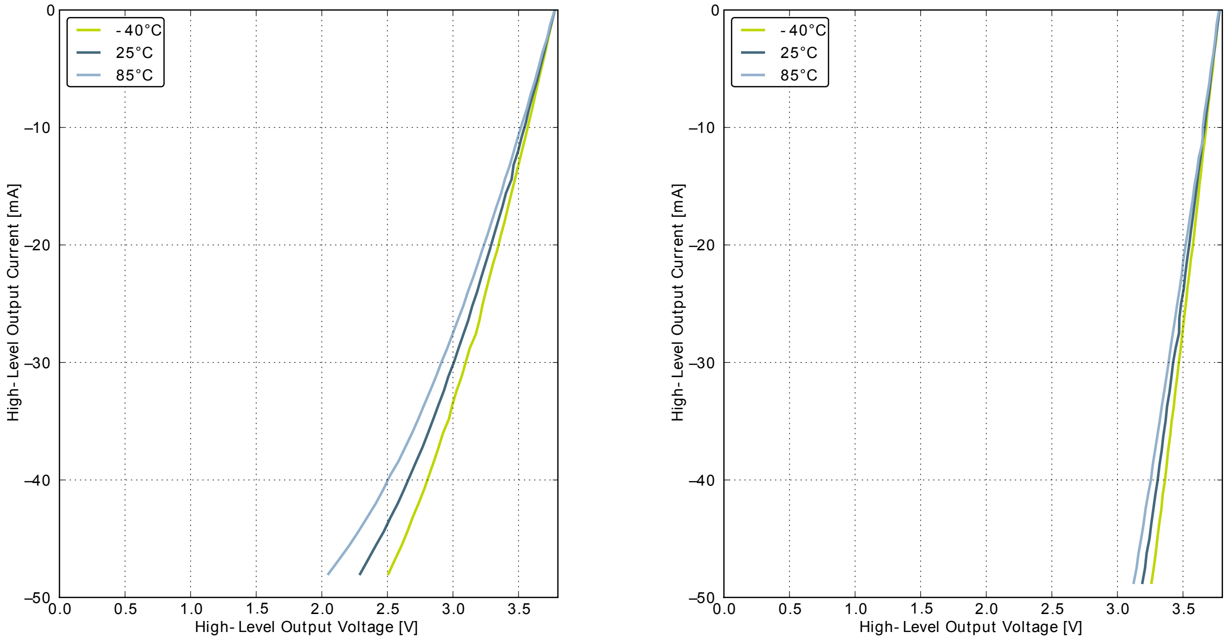
GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		5		25	pF
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		1100		ms

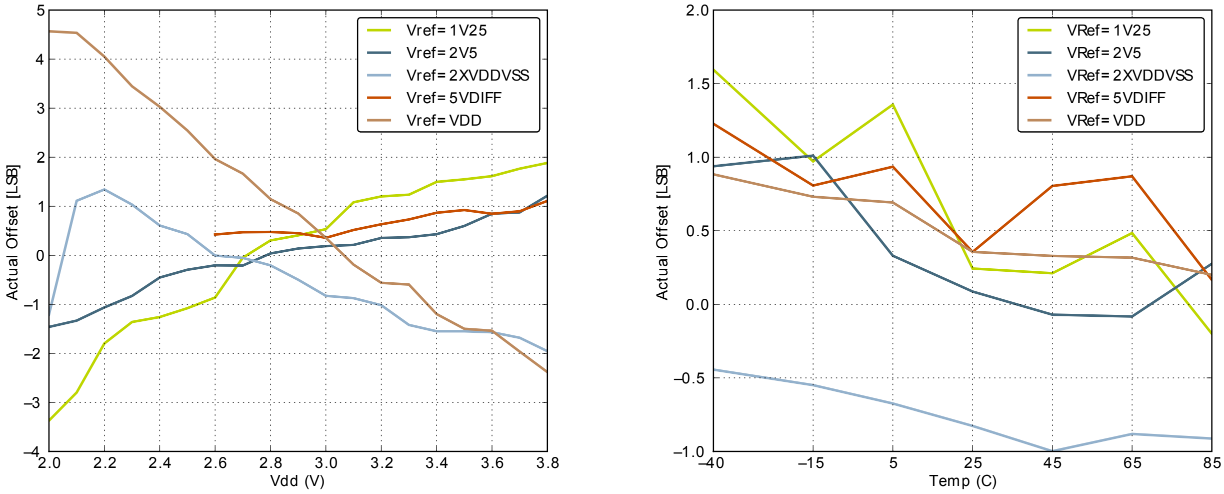
For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported frequency, any mode		4		25	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 25 MHz		30	100	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		25 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	25 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		785		µs

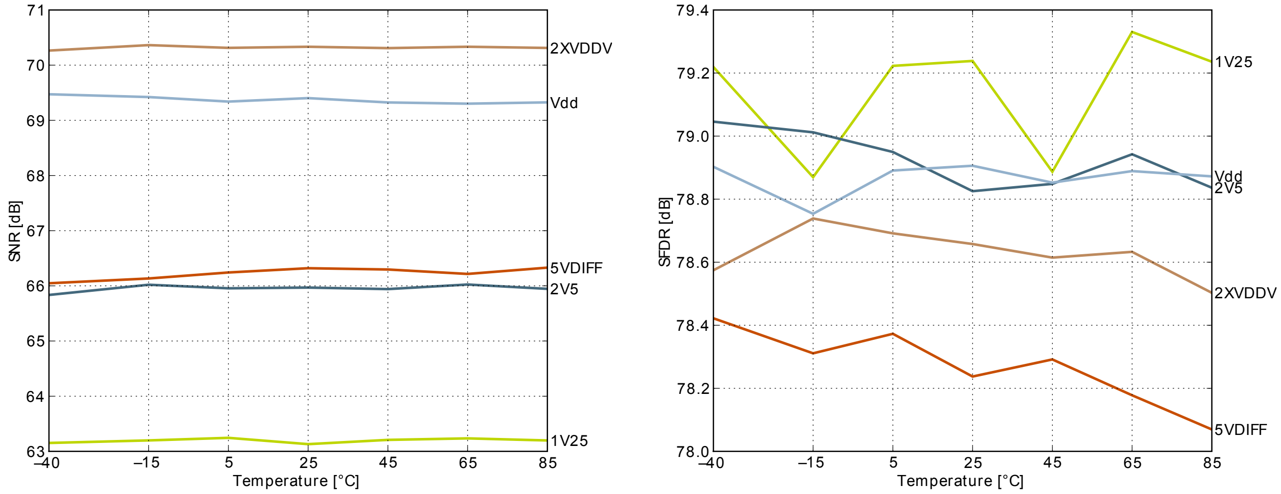
Figure 3.31. ADC Absolute Offset, Common Mode = Vdd /2



Offset vs Supply Voltage, Temp = 25°C

Offset vs Temperature, Vdd = 3V

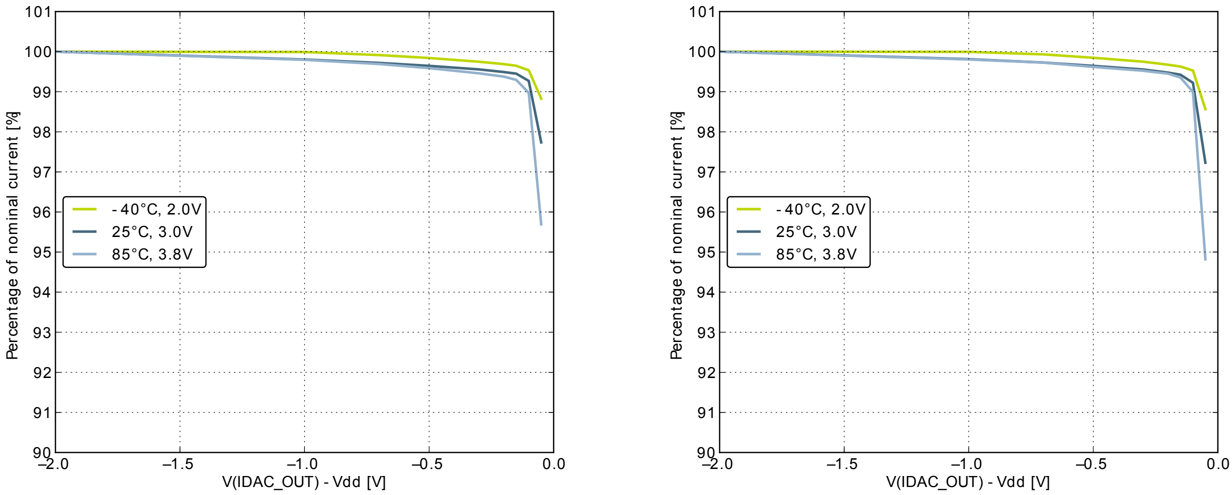
Figure 3.32. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V



Signal to Noise Ratio (SNR)

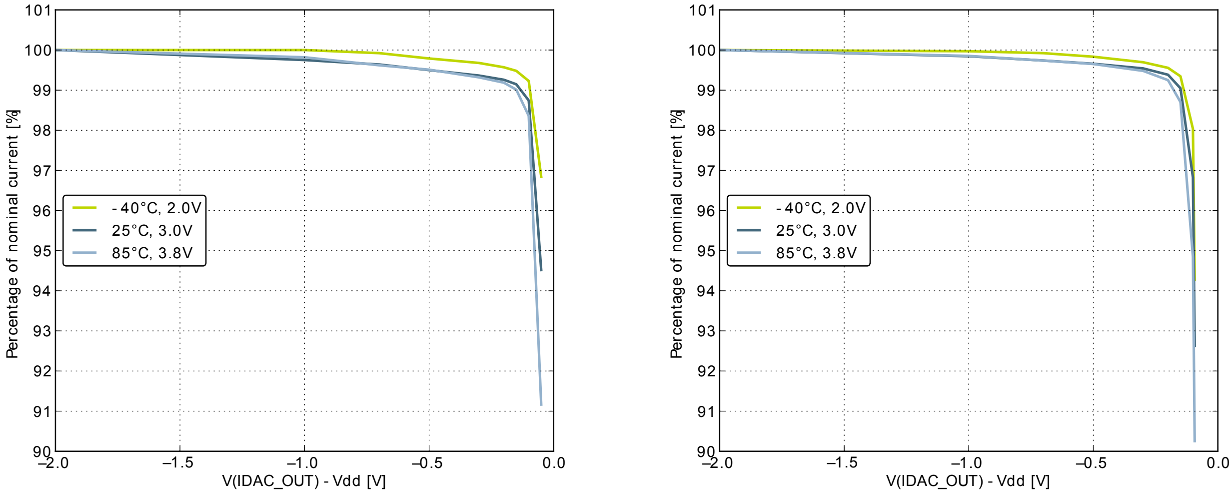
Spurious-Free Dynamic Range (SFDR)

Figure 3.34. IDAC Source Current as a function of voltage on IDAC_OUT



Range 0

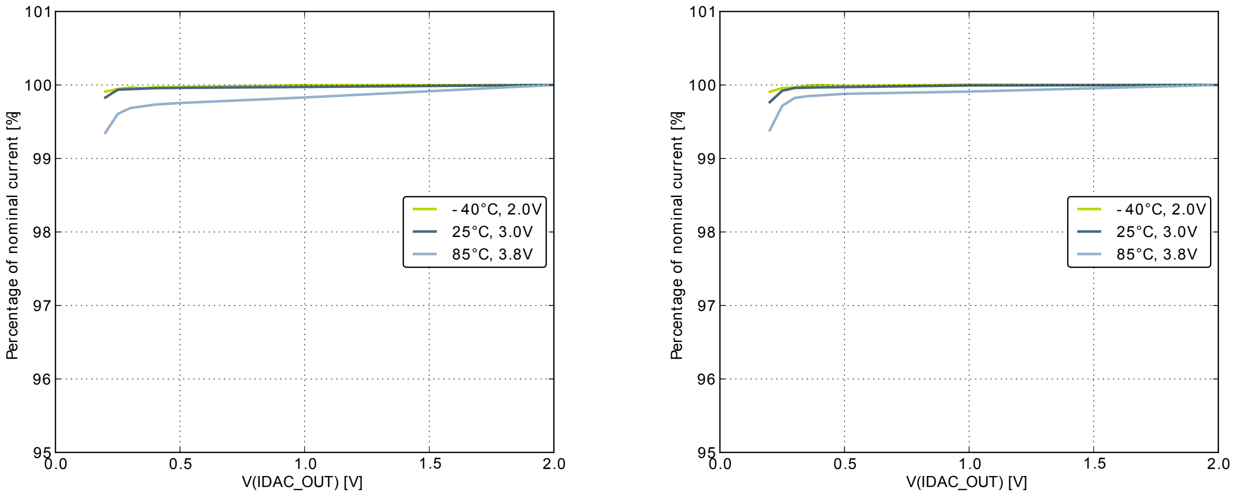
Range 1



Range 2

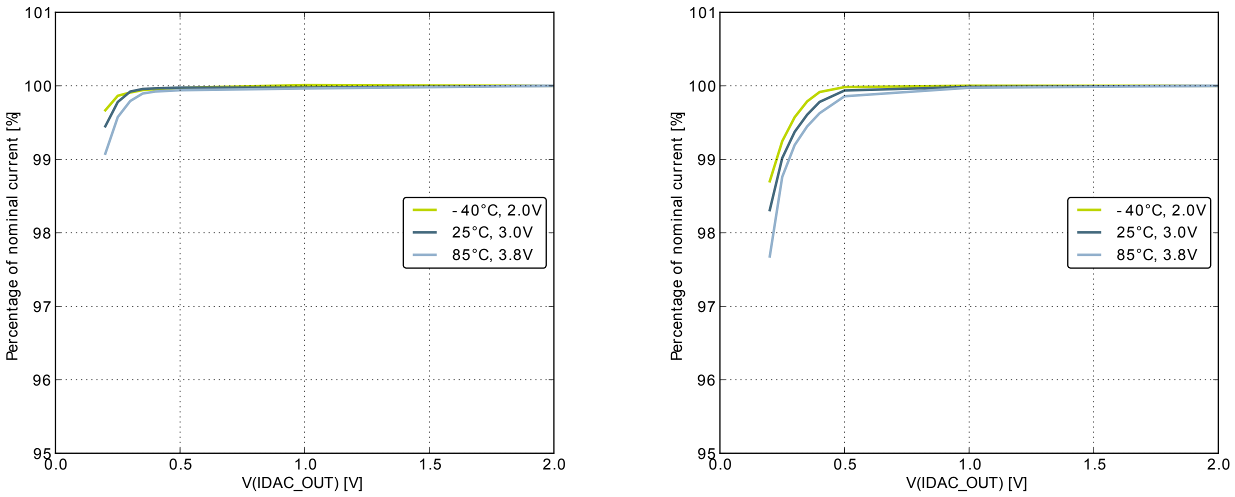
Range 3

Figure 3.35. IDAC Sink Current as a function of voltage from IDAC_OUT



Range 0

Range 1



Range 2

Range 3

Figure 3.36. IDAC linearity

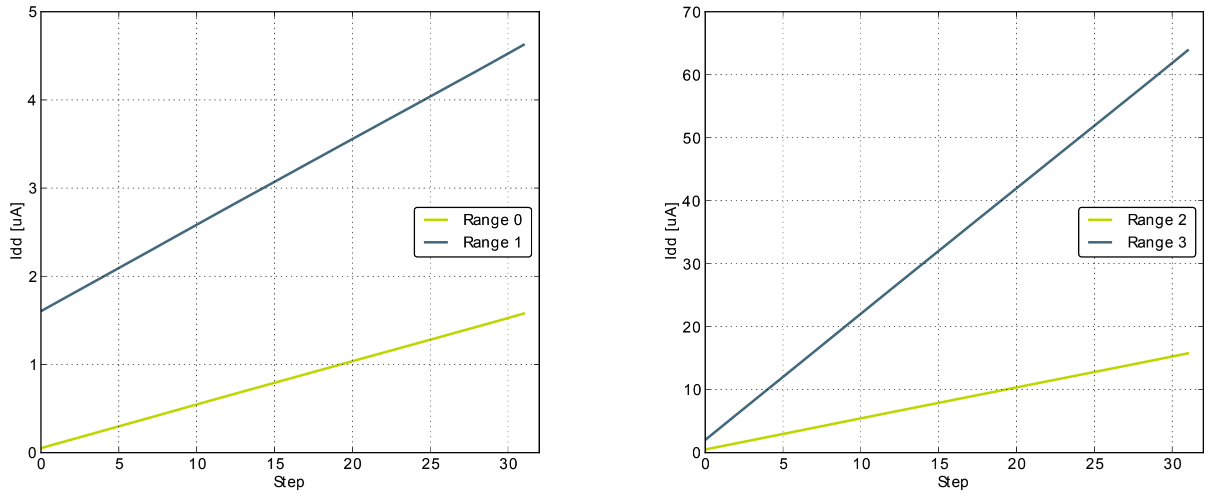
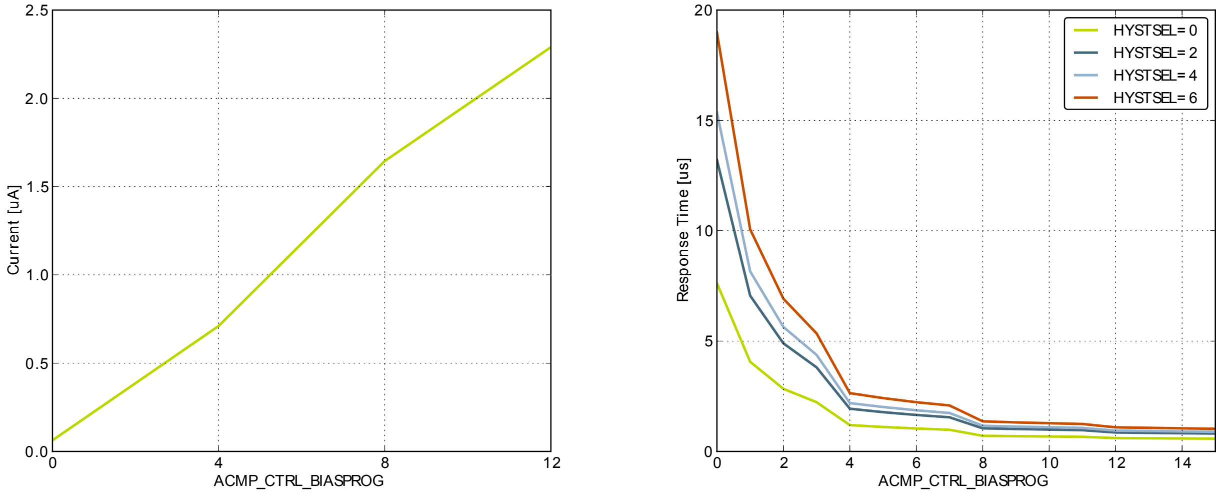
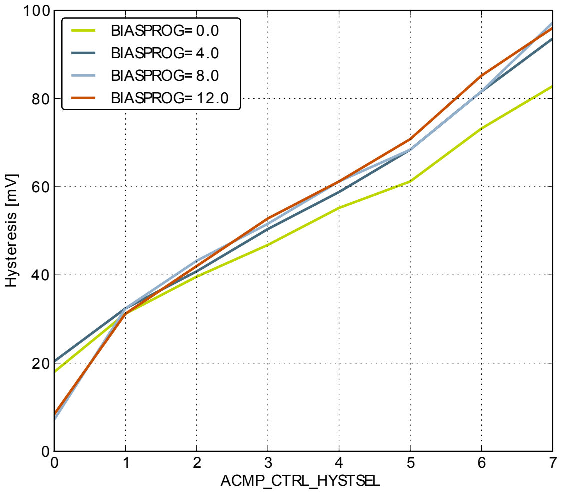


Figure 3.37. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4

Response time , V_{cm} = 1.25V, CP+ to CP- = 100mV



Hysteresis

3.16 Digital Peripherals

Table 3.31. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		7.5		µA/ MHz
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		6.25		µA/ MHz
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		µA/ MHz
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I_{RTC}	RTC current	RTC idle current, clock enabled		100		nA
I_{AES}	AES current	AES idle current, clock enabled		2.5		µA/ MHz
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		5.31		µA/ MHz
I_{PRS}	PRS current	PRS idle current		2.81		µA/ MHz
I_{DMA}	DMA current	Clock enable		8.12		µA/ MHz

CSP36 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
		To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
E6	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
F1	PD5	ADC0_CH5		LEU0_RX #0	
F2	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
F3	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	
F4	AVDD_1	Analog power supply 1.			
F5	PB11	IDAC0_OUT	TIM1_CC2 #3 PCNT0_S1IN #4	US1_CLK #4	CMU_CLK1 #3 ACMP0_O #3
F6	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 54). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13		PD6	PB11				Analog comparator ACMP0, digital output.
ADC0_CH0	PE12							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PE13							Analog to digital converter ADC0, input channel number 1.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0	PA2		PD7	PF2				Clock Management Unit, clock output number 0.
CMU_CLK1	PA1		PE12	PB11				Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0							Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1							Debug-interface Serial Wire data input / output.

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. CSP36 PCB Land Pattern

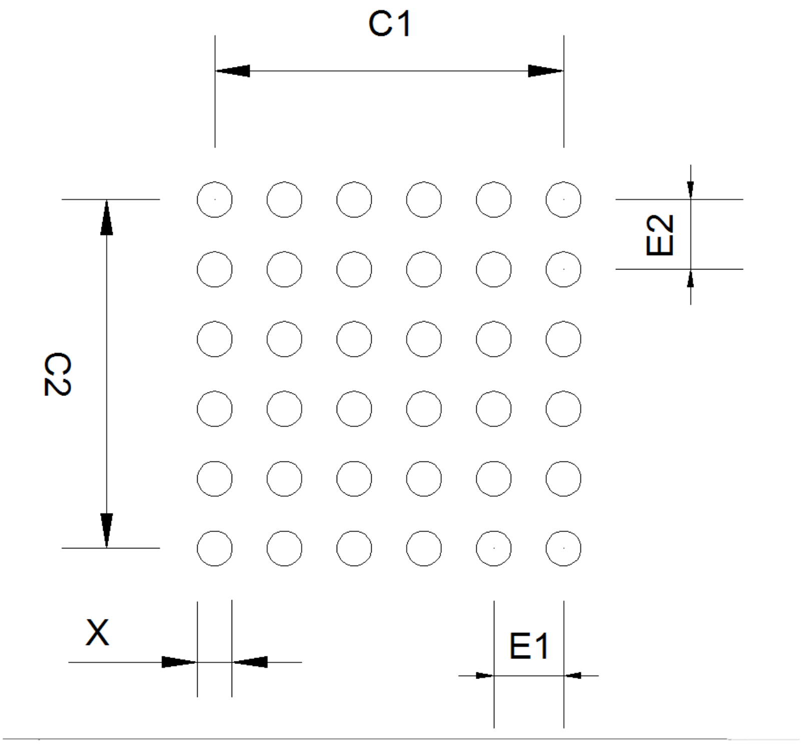


Table 5.1. CSP36 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
X	0.20
C1	2.00
C2	2.00
E1	0.40
E2	0.40

Figure 5.3. CSP36 PCB Stencil Design

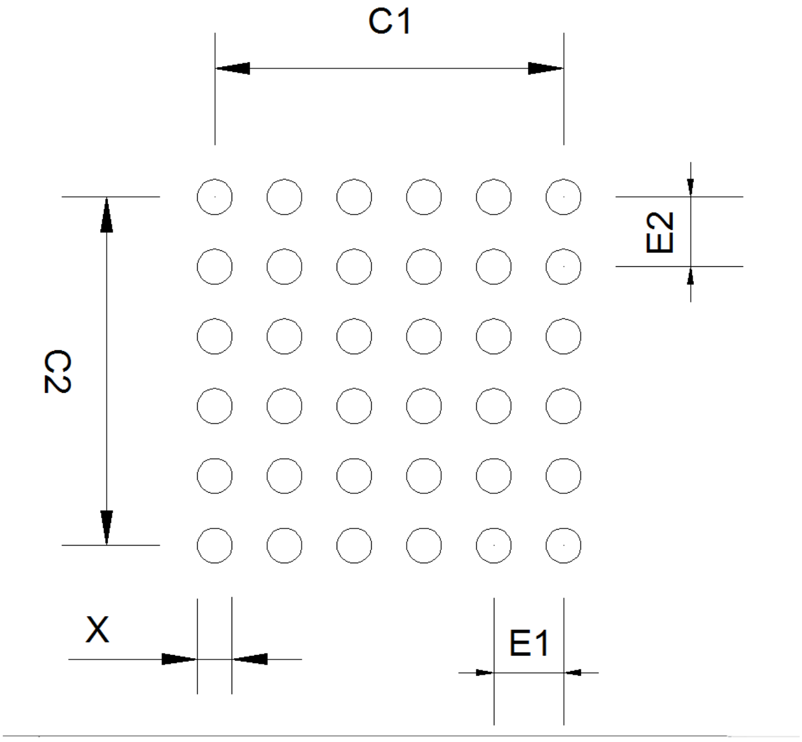


Table 5.3. CSP36 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
X	0.20
C1	2.00
C2	2.00
E1	0.40
E2	0.40

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.075 mm (3 mils).
6. For detailed pin-positioning, see Figure 4.2 (p. 57) .

5.2 Soldering Information

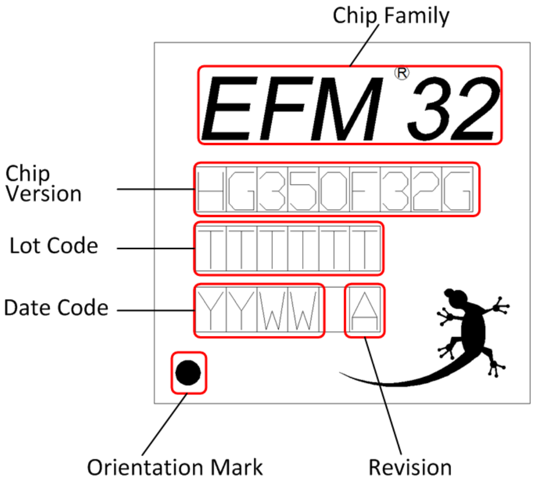
The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 61) .

6.3 Errata

Please see the errata document for EFM32HG350 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

B Contact Information

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701

Please visit the Silicon Labs Technical Support web page:
http://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.