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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 25MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 22 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 4x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 36-UFBGA, CSPBGA |
| Supplier Device Package | 36-CSP (3.02x2.89) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32hg350f32g-b-csp36r |

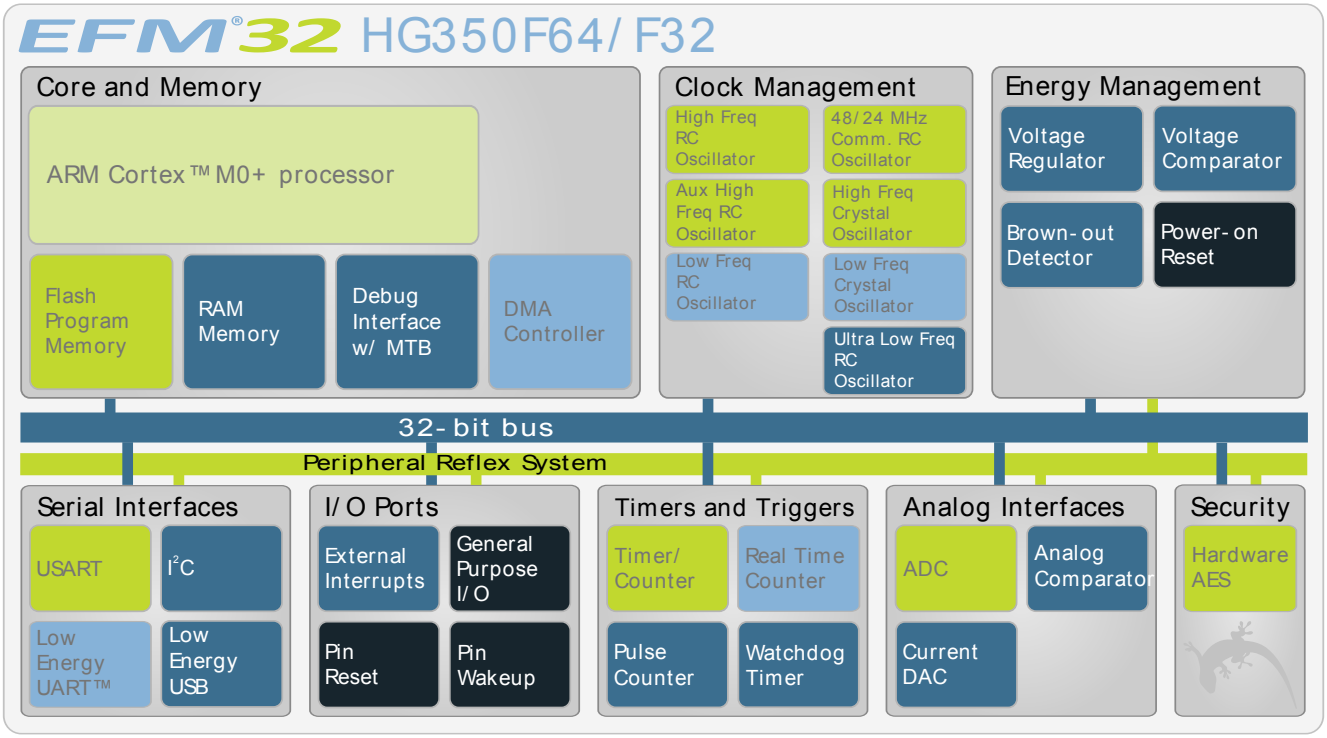
# 2 System Summary

## 2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0+, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32HG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32HG350 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32HG Reference Manual*.

A block diagram of the EFM32HG350 is shown in Figure 2.1 (p. 3) .

***Figure 2.1. Block Diagram***




### 2.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

### 2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and a Micro Trace Buffer (MTB) for data/instruction tracing.

### 2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32HG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits.

There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

### 2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

### 2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32HG.

### 2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32HG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

### 2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32HG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

### 2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

### 2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

### 2.1.10 Low Energy USB

The unique Low Energy USB peripheral provides a full-speed USB 2.0 compliant device controller and PHY with ultra-low current consumption. The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation, and includes a dedicated USB oscillator with clock recovery mechanism for crystal-free operation. No external components are required. The Low Energy Mode ensures the current consumption is optimized and enables USB communication on a strict power budget. The USB device includes an internal dedicated descriptor-based Scatter/Gather DMA and supports up to 3 OUT endpoints and 3 IN endpoints, in addition to endpoint 0. The on-chip PHY includes software controllable pull-up and pull-down resistors.

### 2.1.11 Inter-Integrated Circuit Interface (I2C)

The $I^2C$ module provides an interface between the MCU and a serial $I^2C$-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s.

### 2.1.20 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 3 external pins and 6 internal signals.

### 2.1.21 Current Digital to Analog Converter (IDAC)

The current digital to analog converter can source or sink a configurable constant current, which can be output on, or sinked from pin or ADC. The current is configurable with several ranges of various step sizes.

### 2.1.22 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

### 2.1.23 General Purpose Input/Output (GPIO)

In the EFM32HG350, there are 22 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 10 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

## 2.2 Configuration Summary

The features of the EFM32HG350 is a subset of the feature set described in the EFM32HG Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

***Table 2.1. Configuration Summary***

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S and IrDA | US1_TX, US1_RX, US1_CLK, US1_CS |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 194 | 208 | µA/MHz |
| $I_{EM1}$ | EM1 current | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 64 | 68 | µA/MHz |
| | | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 67 | 71 | µA/MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 85 | 91 | µA/MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 86 | 92 | µA/MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 51 | 55 | µA/MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 52 | 56 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 53 | 57 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 54 | 58 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 56 | 59 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 57 | 61 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 58 | 61 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 59 | 63 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 64 | 68 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 67 | 71 | µA/MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 106 | 114 | µA/MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 114 | 126 | µA/MHz |
| $I_{EM2}$ | EM2 current | EM2 current with RTC prescaled to 1 Hz, 32.768 | | 0.9 | 1.35 | µA |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | | | |
| | | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 1.6 | 3.50 | µA |
| $I_{EM3}$ | EM3 current | EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.6 | 0.90 | µA |
| | | EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 1.2 | 2.65 | µA |
| $I_{EM4}$ | EM4 current | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.02 | 0.035 | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 0.18 | 0.480 | µA |

## 3.4.1 EM0 Current Consumption

***Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 24 MHz***

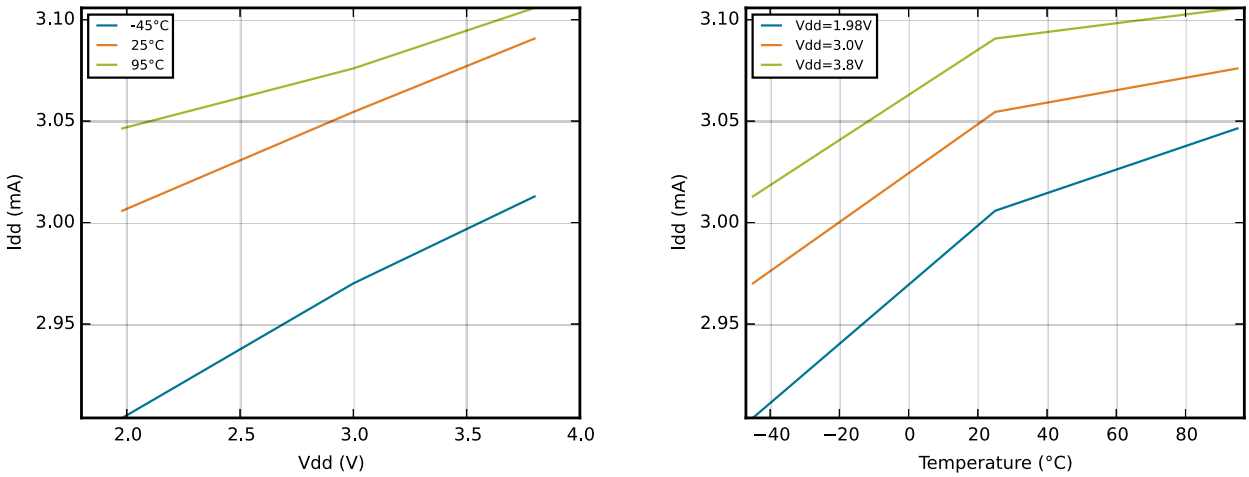


***Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz***

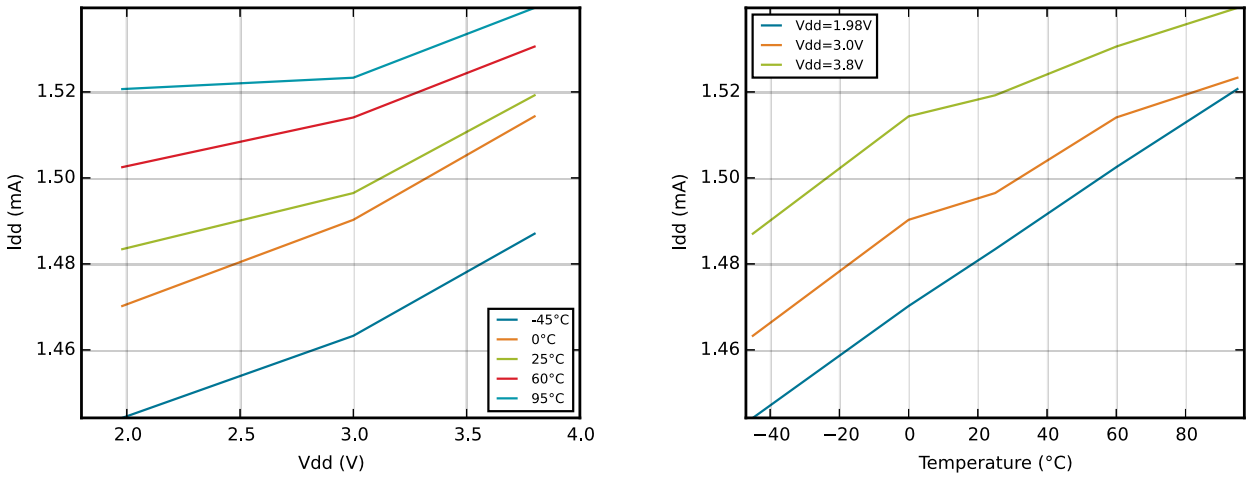
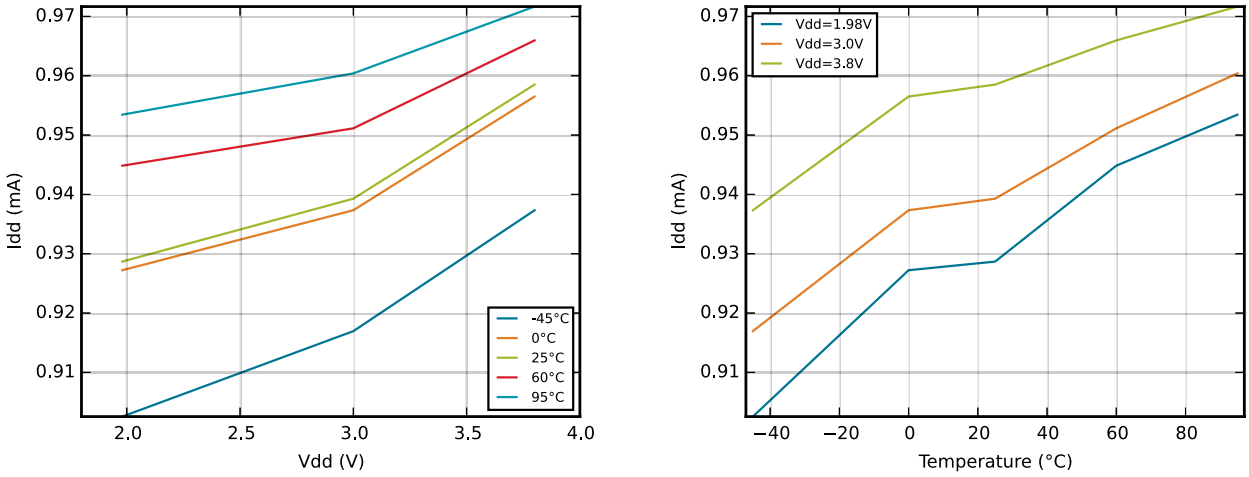
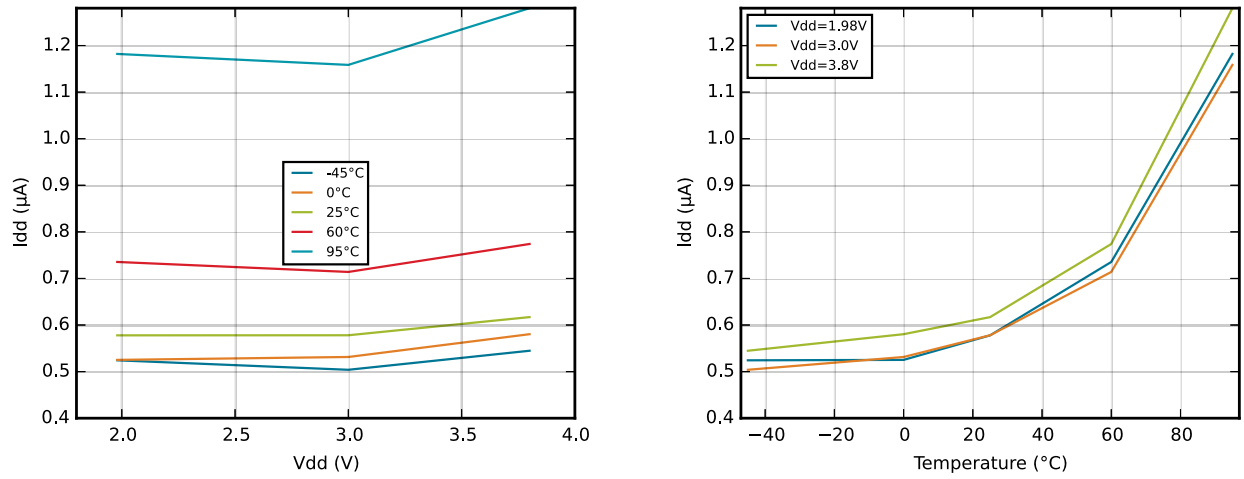



***Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 6.6 MHz***



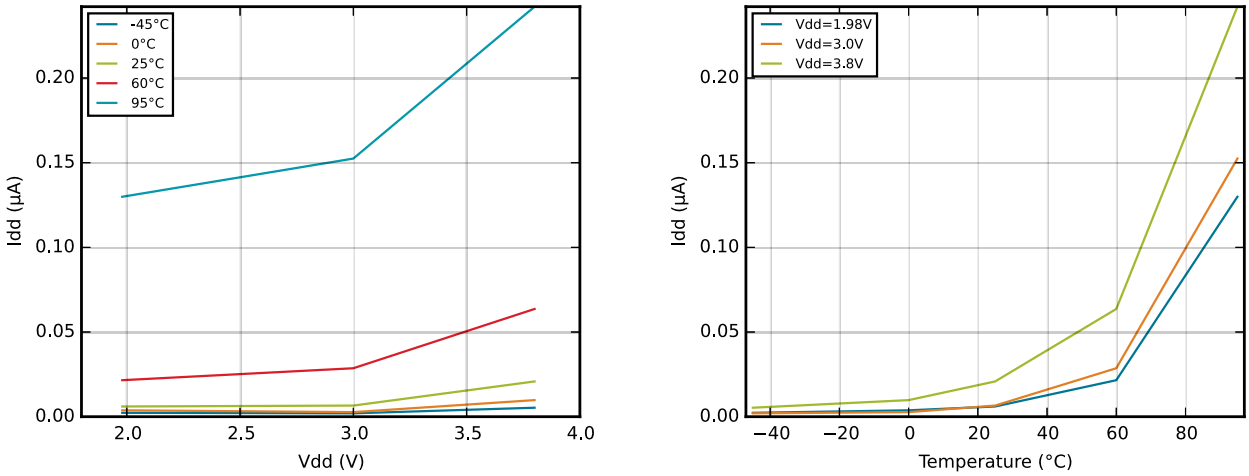
### 3.4.4 EM3 Current Consumption

***Figure 3.12. EM3 current consumption.***




### 3.4.5 EM4 Current Consumption

***Figure 3.13. EM4 current consumption.***



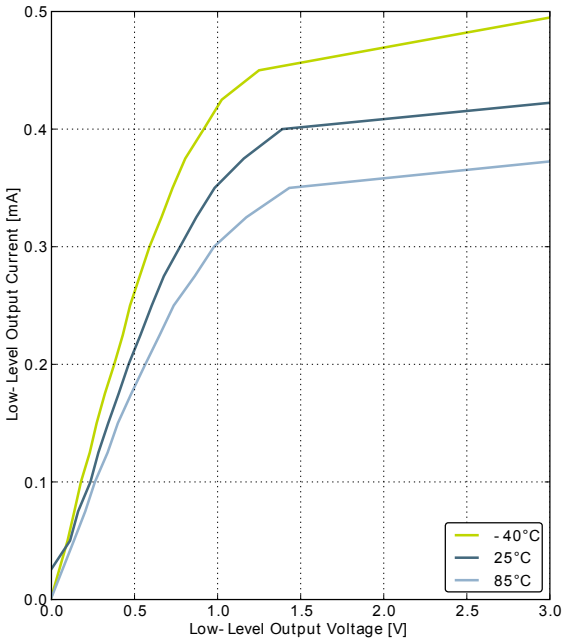

## 3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

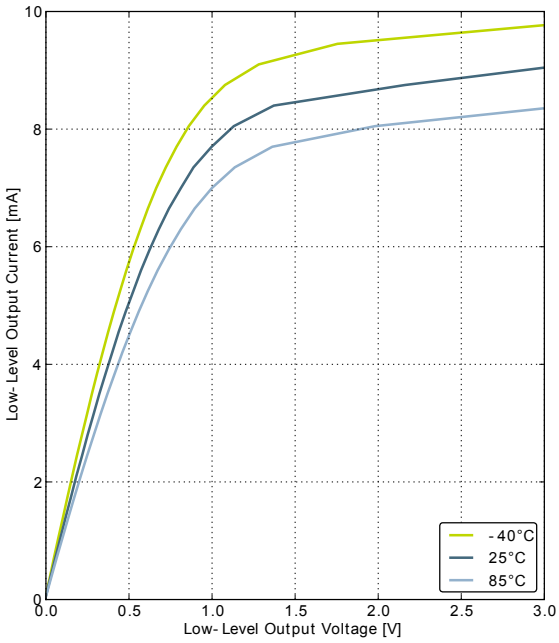
***Table 3.4. Energy Modes Transitions***

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{EM10}$ | Transition time from EM1 to EM0 | | 0 | | HF-CORE-CLK cycles |
| $t_{EM20}$ | Transition time from EM2 to EM0 | | 2 | | µs |
| $t_{EM30}$ | Transition time from EM3 to EM0 | | 2 | | µs |
| $t_{EM40}$ | Transition time from EM4 to EM0 | | 163 | | µs |

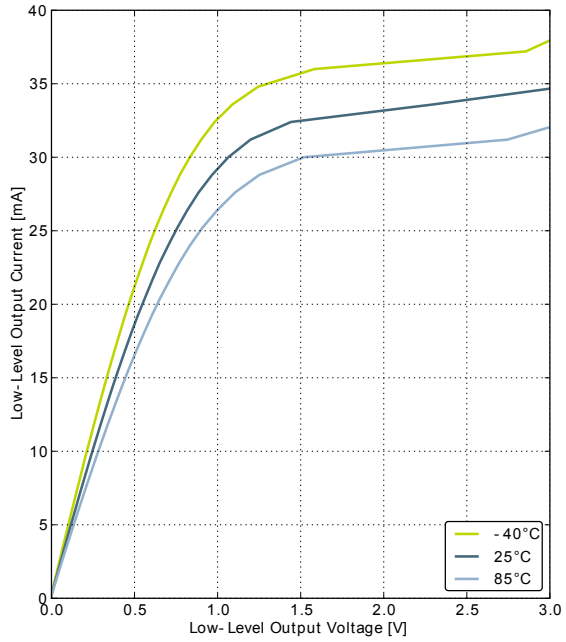
***Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage***



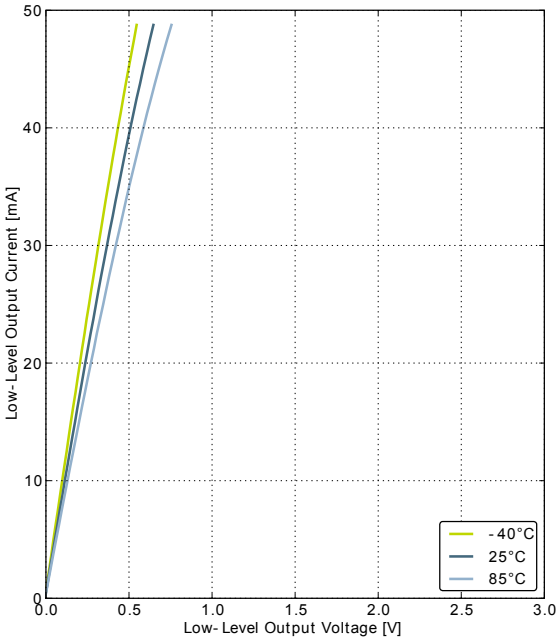

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

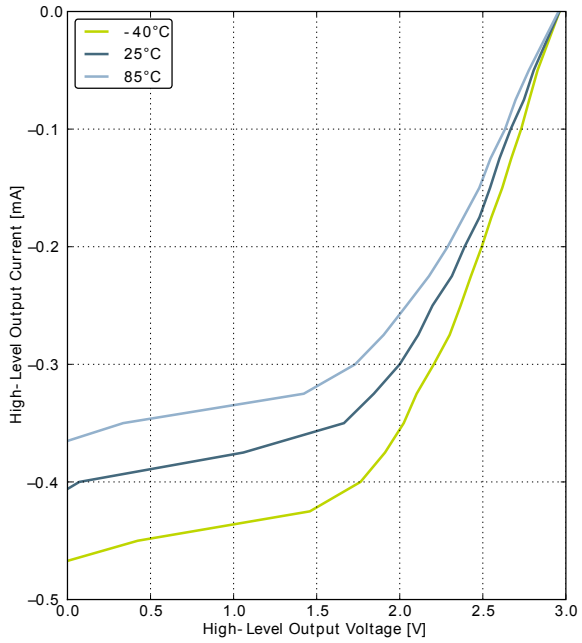



GPIO_Px_CTRL DRIVEMODE = STANDARD

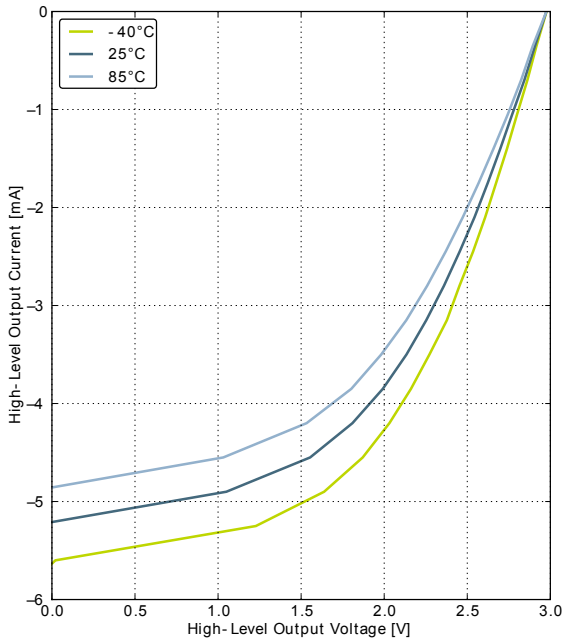



GPIO_Px_CTRL DRIVEMODE = HIGH

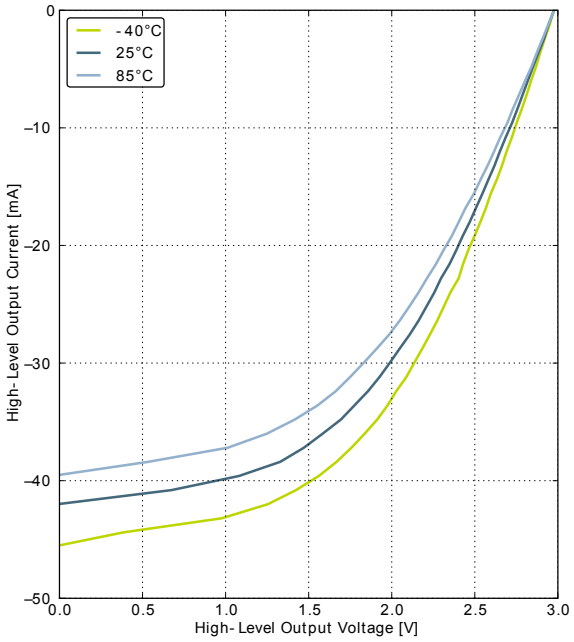
***Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage***



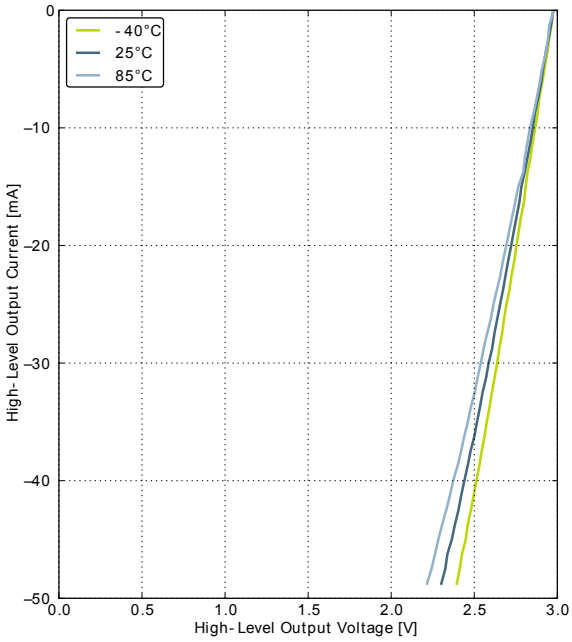

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

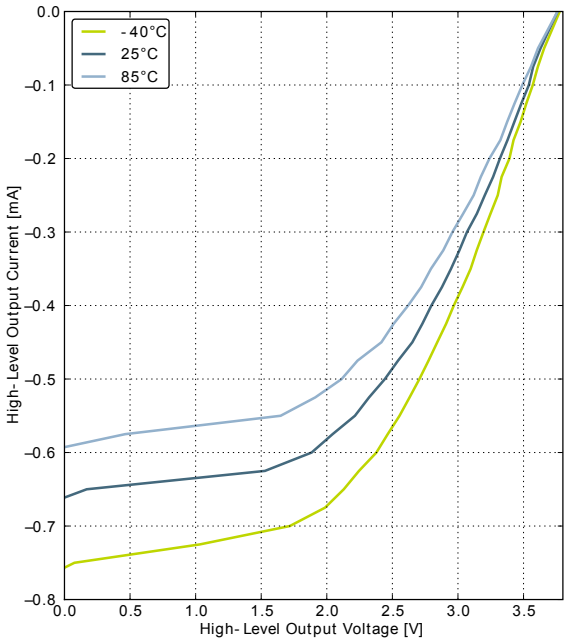



GPIO_Px_CTRL DRIVEMODE = STANDARD

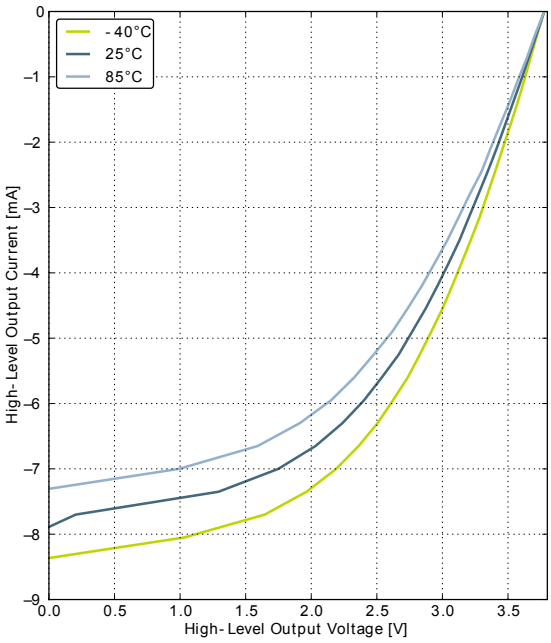



GPIO_Px_CTRL DRIVEMODE = HIGH

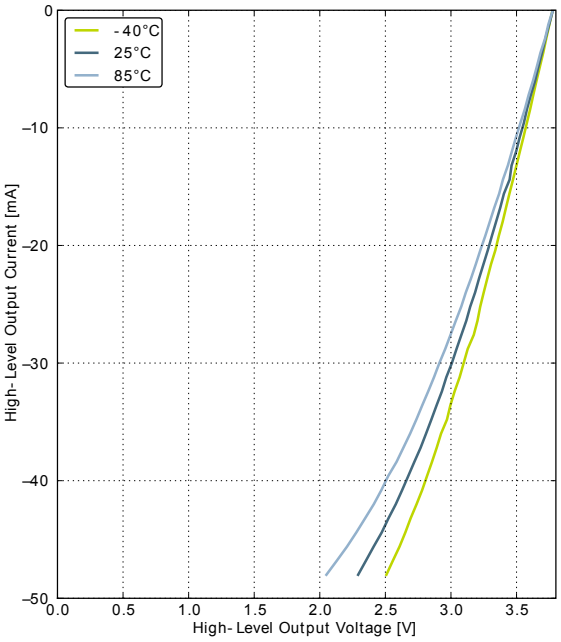
***Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage***



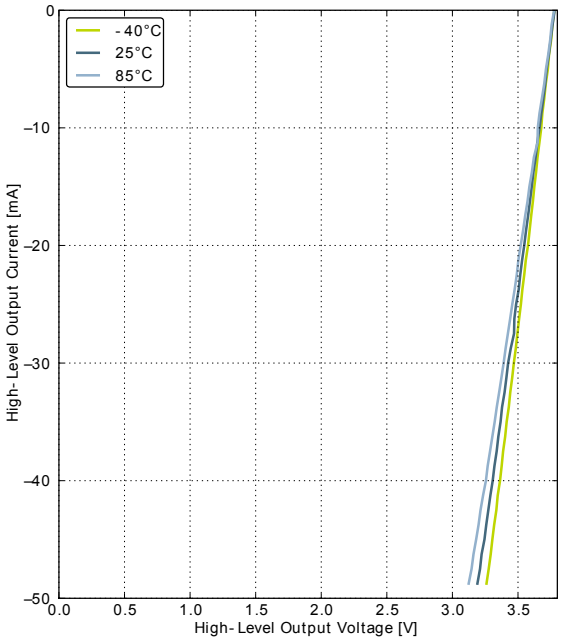

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW




GPIO_Px_CTRL DRIVEMODE = STANDARD




GPIO_Px_CTRL DRIVEMODE = HIGH

***Figure 3.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature***

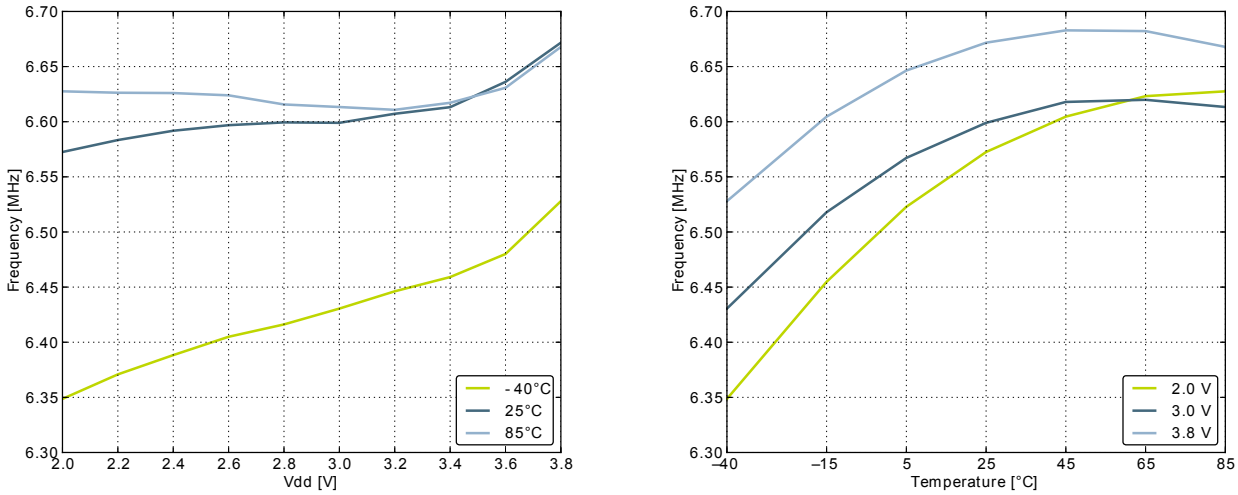



***Figure 3.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature***

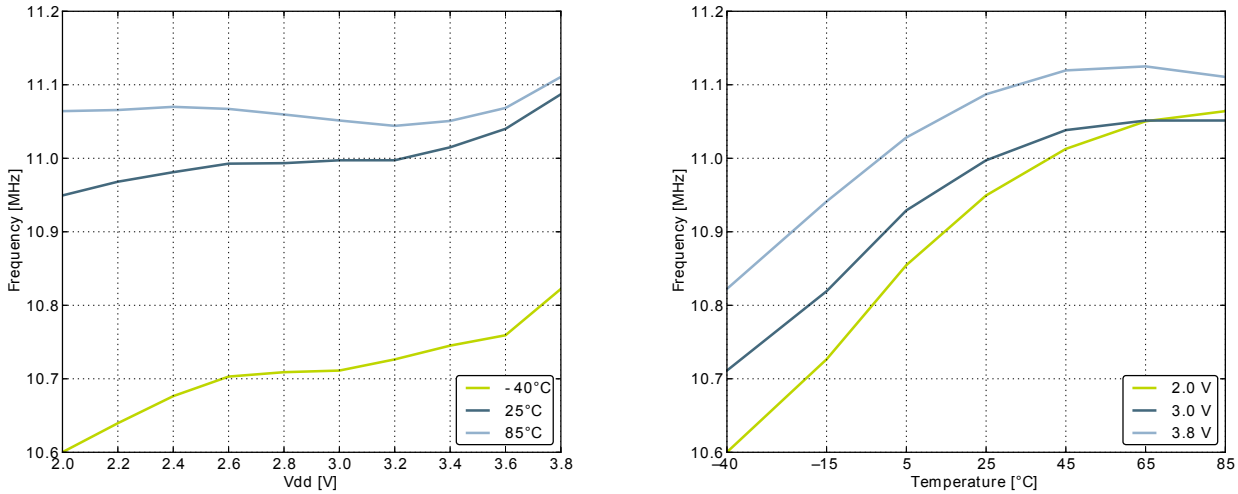
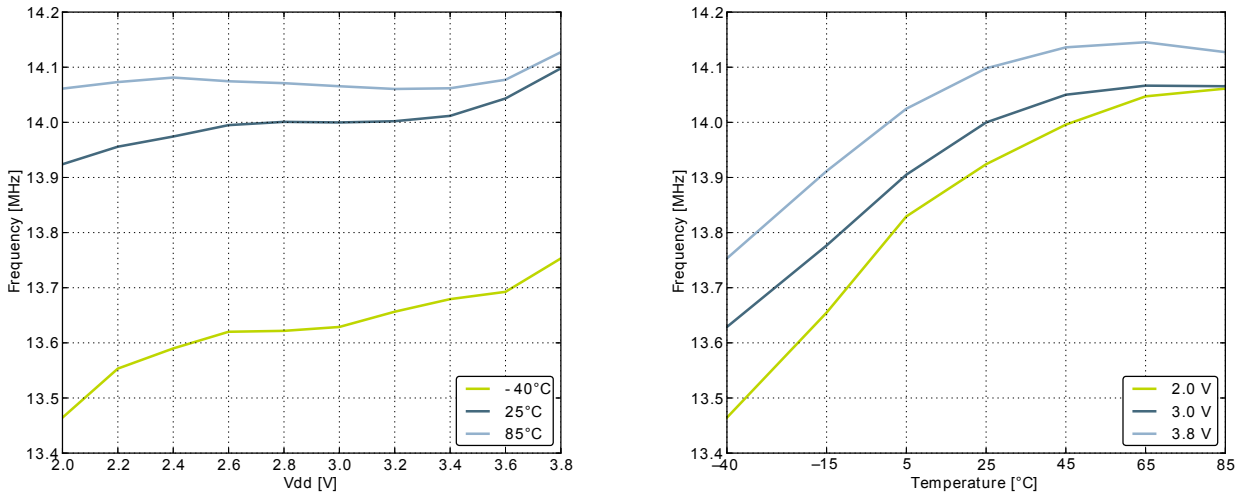



***Figure 3.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature***



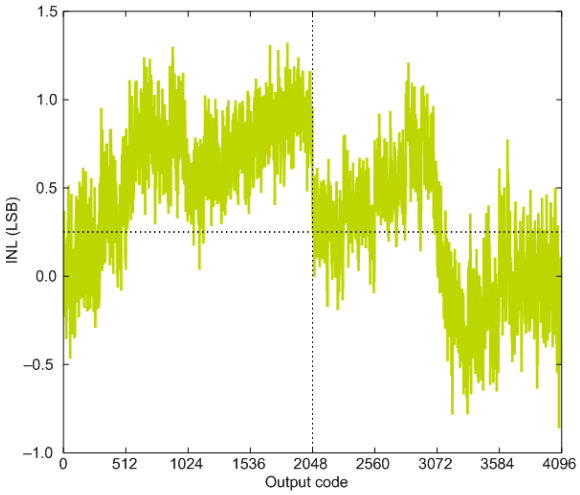
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCREFIN\_CH6}$ | Input range of external positive reference voltage on channel 6 | See $V_{ADCREFIN}$ | 0.625 | | $V_{DD}$ | V |
| $V_{ADCCMIN}$ | Common mode input range | | 0 | | $V_{DD}$ | V |
| $I_{ADCIN}$ | Input current | 2pF sampling capacitors | | <100 | | nA |
| $CMRR_{ADC}$ | Analog input common mode rejection ratio | | | 65 | | dB |
| $I_{ADC}$ | Average active current | 1 MSamples/s, 12 bit, external reference | | 392 | 510 | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00 | | 67 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01 | | 63 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b10 | | 64 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b11 | | 244 | | µA |
| $I_{ADCREF}$ | Current consumption of internal voltage reference | Internal voltage reference | | 65 | | µA |
| $C_{ADCIN}$ | Input capacitance | | | 2 | | pF |
| $R_{ADCIN}$ | Input ON resistance | | 1 | | | MOhm |
| $R_{ADCFILT}$ | Input RC filter resistance | | | 10 | | kOhm |
| $C_{ADCFILT}$ | Input RC filter/decoupling capacitance | | | 250 | | fF |
| $f_{ADCCLK}$ | ADC Clock Frequency | | | | 13 | MHz |
| $t_{ADCCONV}$ | Conversion time | 6 bit | 7 | | | ADCCLK Cycles |
| | | 8 bit | 11 | | | ADCCLK Cycles |
| | | 12 bit | 13 | | | ADCCLK Cycles |
| $t_{ADCACQ}$ | Acquisition time | Programmable | 1 | | 256 | ADCCLK Cycles |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 76 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 78 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 68 | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 79 | | dBc |
| $V_{ADCOFFSET}$ | Offset voltage | After calibration, single ended | -4 | 0.3 | 4 | mV |
| | | After calibration, differential | | 0.3 | | mV |
| $TGRAD_{ADCTH}$ | Thermometer output gradient | | | -1.92 | | mV/°C |
| | | | | -6.3 | | ADC Codes/ °C |
| $DNL_{ADC}$ | Differential non-linearity (DNL) | $V_{DD}$= 3.0 V, external 2.5V reference | -1 | ±0.7 | 4 | LSB |
| $INL_{ADC}$ | Integral non-linearity (INL), End point method | | | ±1.6 | ±3 | LSB |
| $MC_{ADC}$ | No missing codes | | 11.999[1] | 12 | | bits |
| $VREF_{ADC}$ | ADC Internal Voltage Reference | Internal 1.25V, $V_{DD}$ = 3V, 25°C | 1.248 | 1.254 | 1.262 | V |
| | | Internal 1.25V, Full temperature and supply range | 1.188 | 1.254 | 1.302 | V |
| | | Internal 2.5V, $V_{DD}$ = 3V, 25°C | 2.492 | 2.506 | 2.520 | V |
| | | Internal 2.5V, Full temperature and supply range | 2.402 | 2.506 | 2.600 | V |

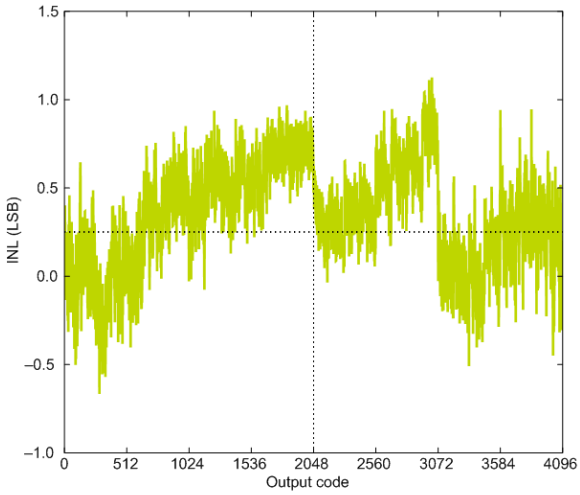
[1]On the average every ADC will have one missing code, most likely to appear around 2048 ± n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.26 (p. 37) and Figure 3.27 (p. 37) , respectively.

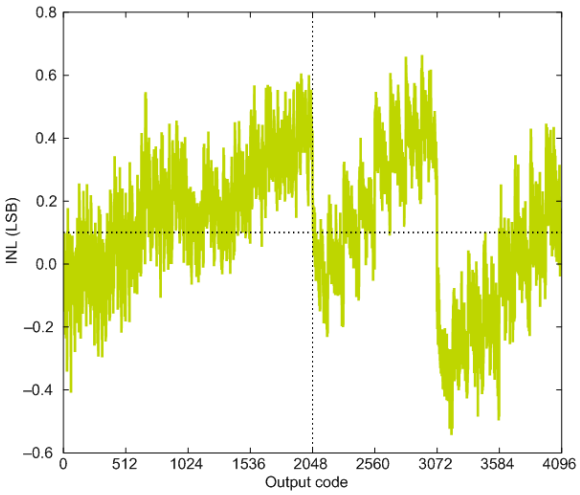
***Figure 3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C***



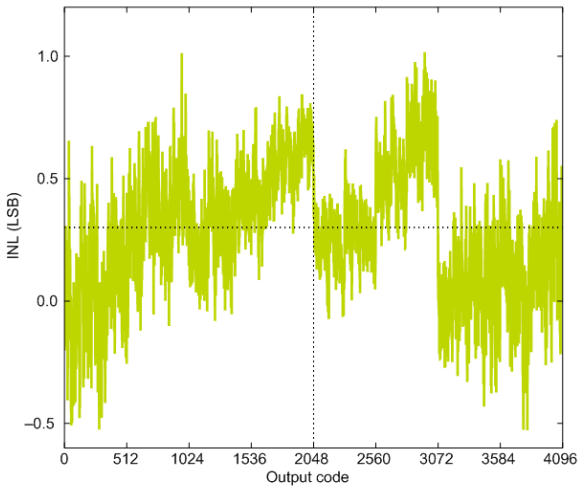

1.25V Reference



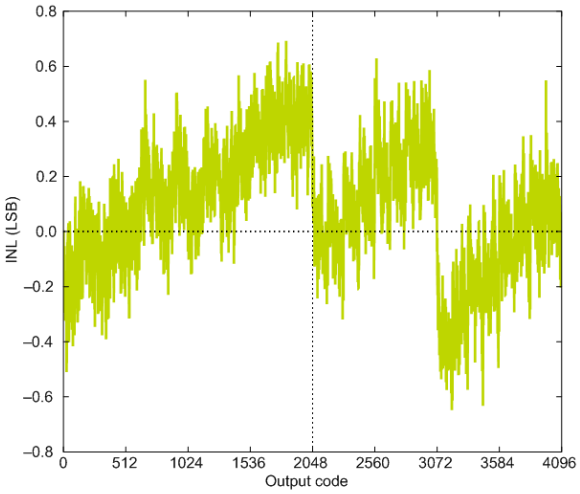

2.5V Reference




2XVDDVSS Reference

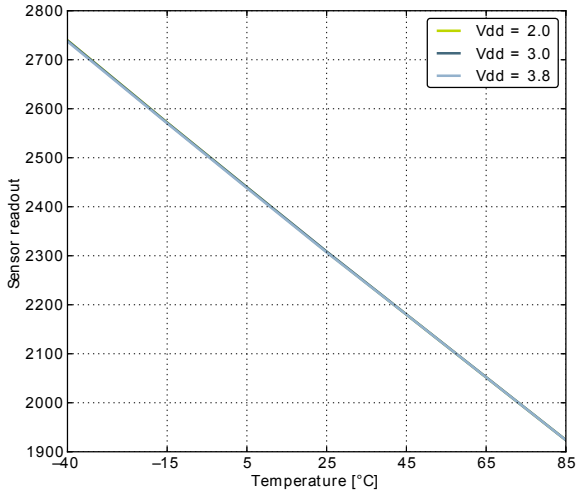



5VDIFF Reference




VDD Reference

*Figure 3.33. ADC Temperature sensor readout*




# 3.11 Current Digital Analog Converter (IDAC)

*Table 3.16. IDAC Range 0 Source*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 13.0 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 0.85 | | µA |
| $I_{STEP}$ | Step size | | | 0.05 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = $V_{DD}$ - 100mV | | 0.79 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0V, STEPSEL=0x10 | | 0.3 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 11.7 | | nA/V |

*Table 3.17. IDAC Range 0 Sink*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 15.1 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 0.85 | | µA |
| $I_{STEP}$ | Step size | | | 0.05 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 0.30 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.2 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 12.5 | | nA/V |

*Table 3.28. I2C Fast-mode (Fm)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 400[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 1.3 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 0.6 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 100 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | 900[2,3] | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 0.6 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 0.6 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 0.6 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 1.3 | | | µs |

[1]For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32HG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 5).

*Table 3.29. I2C Fast-mode Plus (Fm+)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 1000[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 0.5 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 0.26 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 50 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 0.26 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 0.26 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 0.26 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 0.5 | | | µs |

[1]For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32HG Reference Manual.

## 3.15 USB

The USB hardware in the EFM32HG350 passes all tests for USB 2.0 Full Speed certification. The test report will be distributed with application note "AN0046 - USB Hardware Design Guide" when ready.

*Table 3.30. USB*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{USBOUT}$ | USB regulator output voltage | | 3.1 | 3.4 | 3.7 | V |
| $I_{USBOUT}$ | USB regulator output current | BIASPROG=0, $T_{AMB}$=25°C | 55.7 | 79.4 | 104.1 | mA |
| | | BIASPROG=1, $T_{AMB}$=25°C | 66.0 | 95.9 | 126.4 | mA |
| | | BIASPROG=2, $T_{AMB}$=25°C | 94.6 | 146.5 | 188.1 | mA |
| | | BIASPROG=3, $T_{AMB}$=25°C | 80.4 | 128.3 | 176.0 | mA |

| CSP36 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| | | | | LEU0_RX #5<br>USB_DP | |
| A3 | VSS | Ground. | | | |
| A4 | IOVDD_5 | Digital IO power supply 5. | | | |
| A5 | PE12 | ADC0_CH0 | TIM1_CC2 #1<br>TIM2_CC1 #3 | US0_RX #3<br>US0_CLK #0/6<br>I2C0_SDA #6 | CMU_CLK1 #2<br>PRS_CH1 #3 |
| A6 | PA0 | | TIM0_CC1 #6<br>TIM0_CC0 #0/1/4<br>PCNT0_S0IN #4 | USB_DMPU #0<br>US1_RX #4<br>LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>PRS_CH3 #3<br>GPIO_EM4WU0 |
| B1 | USB_VREGI | | | | |
| B2 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| B3 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |
| B4 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | PRS_CH2 #2 |
| B5 | PE13 | ADC0_CH1 | TIM2_CC2 #3 | US0_TX #3<br>US0_CS #0/6<br>I2C0_SCL #6 | ACMP0_O #0<br>PRS_CH2 #3<br>GPIO_EM4WU5 |
| B6 | PA1 | | TIM0_CC0 #6<br>TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| C1 | USB_VREGO | | | | |
| C2 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| C3 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| C4 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | PRS_CH3 #2 |
| C5 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| C6 | IOVDD_0 | Digital IO power supply 0. | | | |
| D1 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| D2 | VSS_DREG | Ground for on-chip voltage regulator. | | | |
| D3 | PD6 | ADC0_CH6 | TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2/3<br>I2C0_SDA #1 | ACMP0_O #2 |
| D4 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| D5 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| D6 | VSS | Ground. | | | |
| E1 | PD7 | ADC0_CH7 | TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2/3<br>I2C0_SCL #1 | CMU_CLK0 #2 |
| E2 | VSS | Ground. | | | |
| E3 | AVSS_0 | Analog ground 0. | | | |
| E4 | AVDD_0 | Analog power supply 0. | | | |
| E5 | RESETn | Reset input, active low. | | | |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PC14 | | | | | | | USB D- pin. |
| USB_DMPU | PA0 | | | | | | | USB D- Pullup control. |
| USB_DP | PC15 | | | | | | | USB D+ pin. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

## 4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32HG350* is shown in Table 4.3 (p. 56) . Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

***Table 4.3. GPIO Pinout***

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

*Figure 5.3. CSP36 PCB Stencil Design*

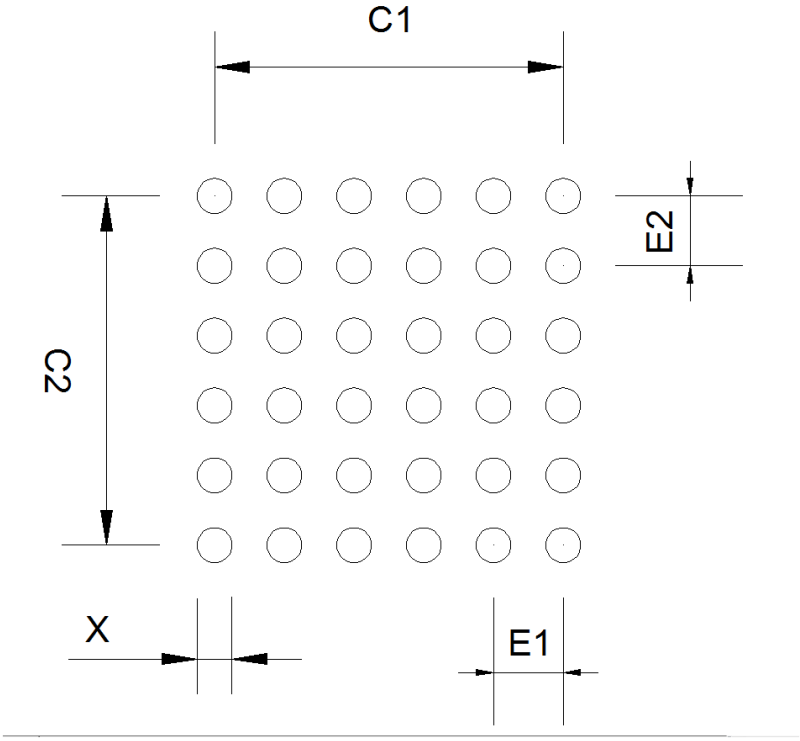



*Table 5.3. CSP36 PCB Stencil Design Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) |
|---|---|
| X | 0.20 |
| C1 | 2.00 |
| C2 | 2.00 |
| E1 | 0.40 |
| E2 | 0.40 |

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.075 mm (3 mils).
6. For detailed pin-positioning, see Figure 4.2 (p. 57) .

## 5.2 Soldering Information

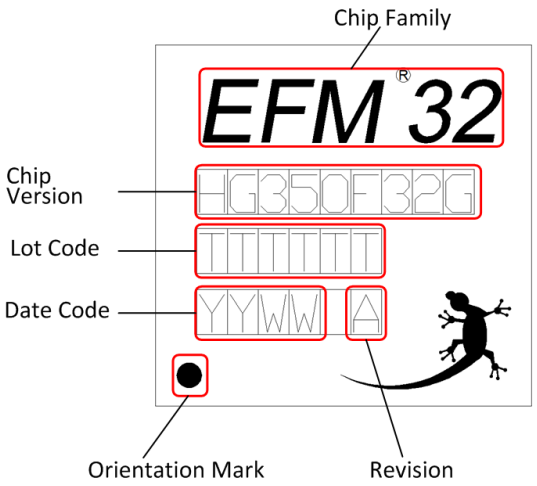
The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

# 6 Chip Marking, Revision and Errata

## 6.1 Chip Marking

In the illustration below package fields and position are shown.

***Figure 6.1. Example Chip Marking (top view)***




## 6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 61) .

## 6.3 Errata

Please see the errata document for EFM32HG350 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit