Silicon Labs - EFM32HG350F64G-B-CSP36 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFBGA, CSPBGA
Supplier Device Package	36-CSP (3.02x2.89)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg350f64g-b-csp36

There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32HG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32HG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32HG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Low Energy USB

The unique Low Energy USB peripheral provides a full-speed USB 2.0 compliant device controller and PHY with ultra-low current consumption. The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation, and includes a dedicated USB oscillator with clock recovery mechanism for crystal-free operation. No external components are required. The Low Energy Mode ensures the current consumption is optimized and enables USB communication on a strict power budget. The USB device includes an internal dedicated descriptor-based Scatter/Gather DMA and supports up to 3 OUT endpoints and 3 IN endpoints, in addition to endpoint 0. The on-chip PHY includes software controllable pull-up and pull-down resistors.

2.1.11 Inter-Integrated Circuit Interface (I2C)

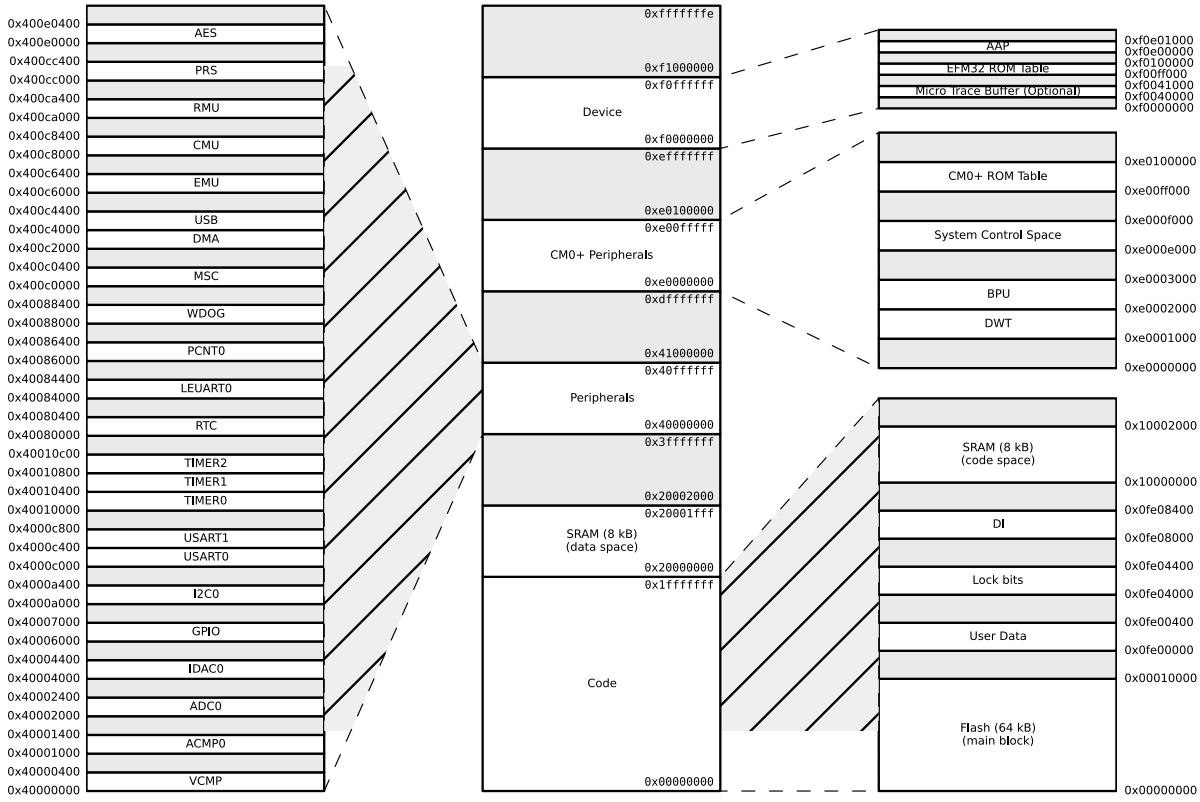
The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s.

Module	Configuration	Pin Connections
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:5]
IDAC0	Full configuration	IDAC0_OUT
AES	Full configuration	NA
GPIO	22 pins	Available pins are shown in Table 4.3 (p. 56)

2.3 Memory Map

The *EFM32HG350* memory map is shown in Figure 2.2 (p. 7), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32HG350 Memory Map with largest RAM and Flash sizes

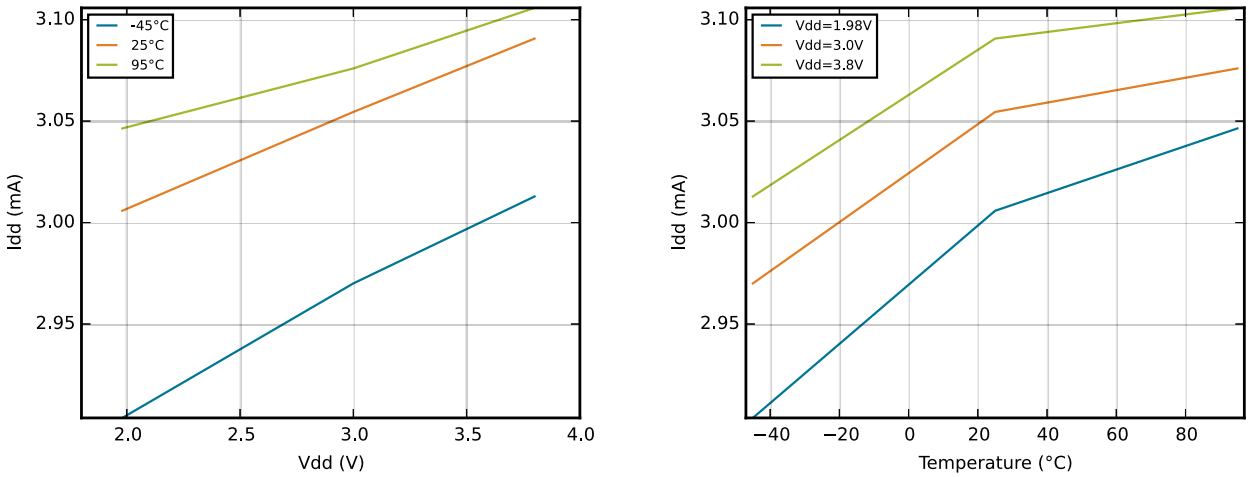


Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		194	208	µA/MHz
I_{EM1}	EM1 current	24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		64	68	µA/MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		67	71	µA/MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		85	91	µA/MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		86	92	µA/MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		51	55	µA/MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		52	56	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		53	57	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		54	58	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		56	59	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		57	61	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		58	61	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		59	63	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		64	68	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		67	71	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		106	114	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		114	126	µA/MHz
I_{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768		0.9	1.35	µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25°C				
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85°C		1.6	3.50	µA
I_{EM3}	EM3 current	EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V_{DD}= 3.0 V, T_{AMB}=25°C		0.6	0.90	µA
		EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V_{DD}= 3.0 V, T_{AMB}=85°C		1.2	2.65	µA
I_{EM4}	EM4 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.02	0.035	µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		0.18	0.480	µA

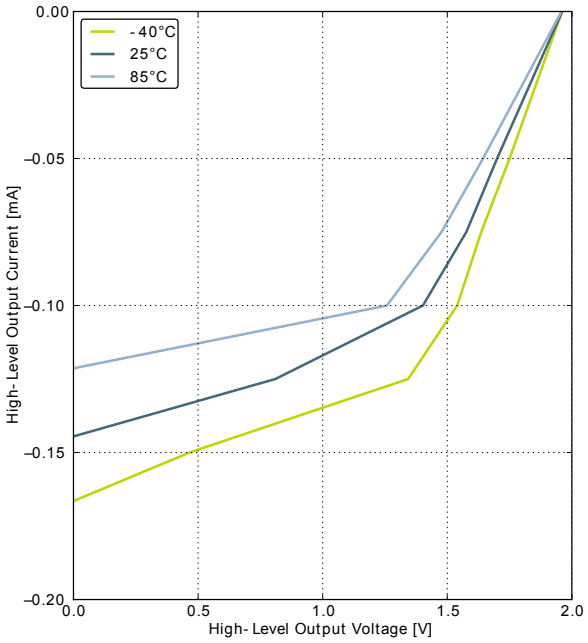
3.4.1 EM0 Current Consumption

Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 24 MHz

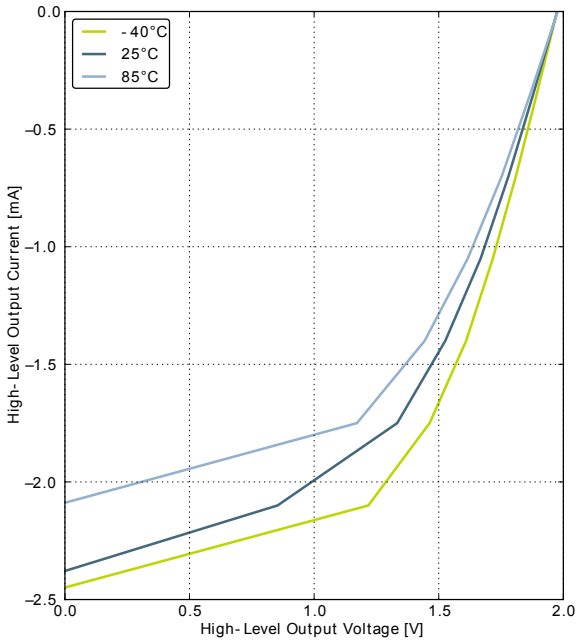


Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sinking 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.25V_{DD}	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or Vdd		±0.1	±40	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C_L=12.5-25pF.	20+0.1C_L		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C_L=350-600pF	20+0.1C_L		250	ns
V_{IOHYST}	I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{DD} = 1.98 - 3.8 V	0.1V_{DD}			V

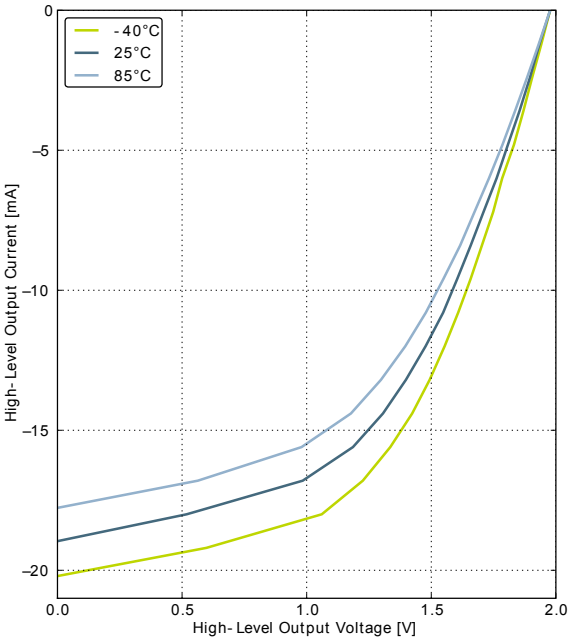
Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage



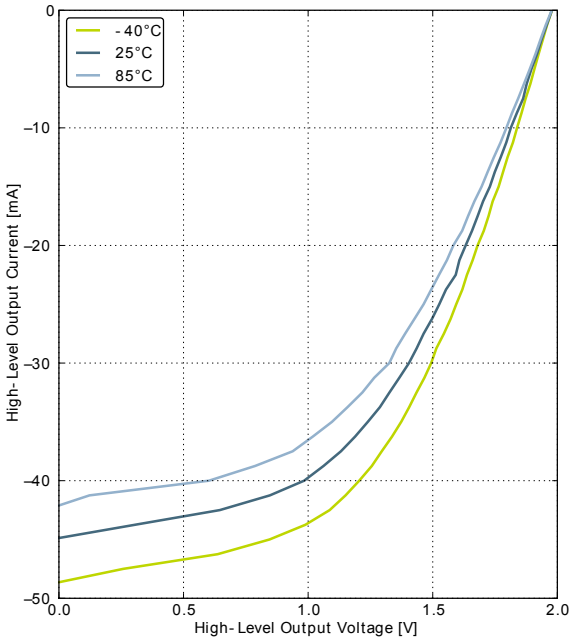
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

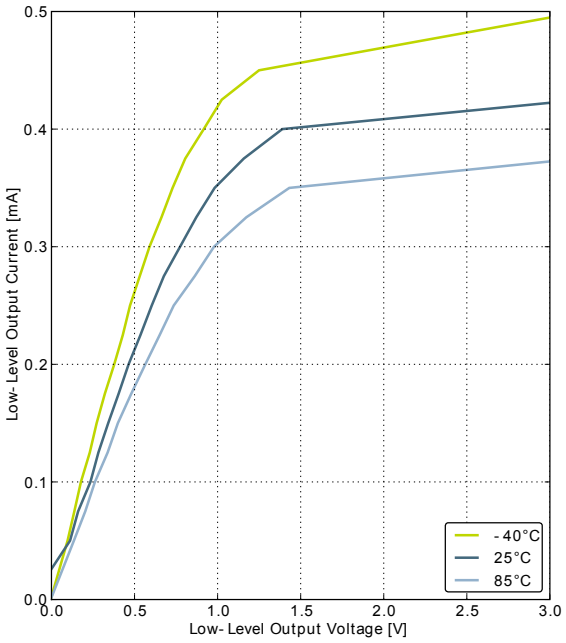


GPIO_Px_CTRL DRIVEMODE = STANDARD

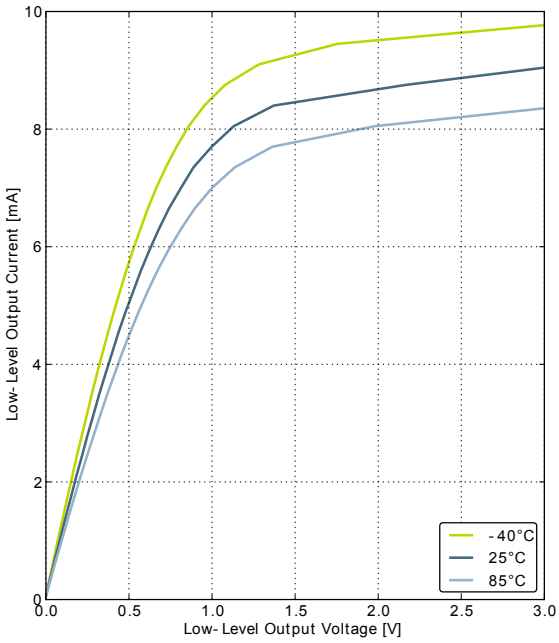


GPIO_Px_CTRL DRIVEMODE = HIGH

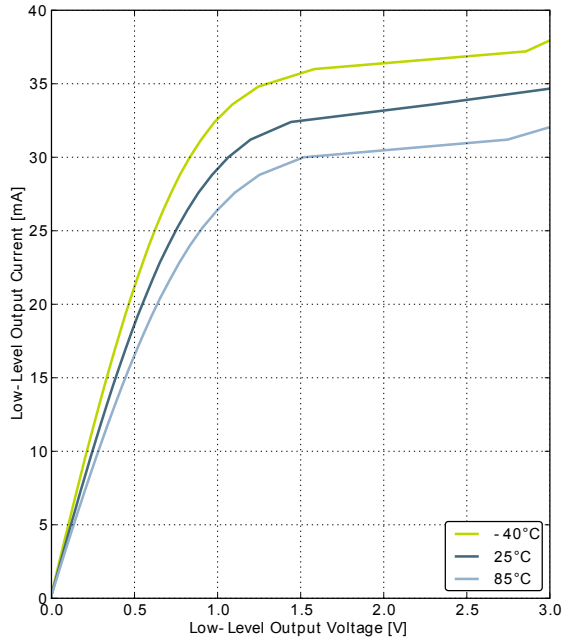
Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage



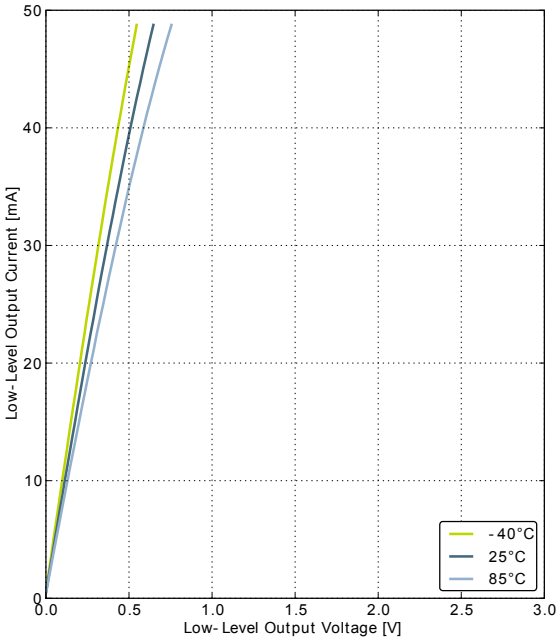
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



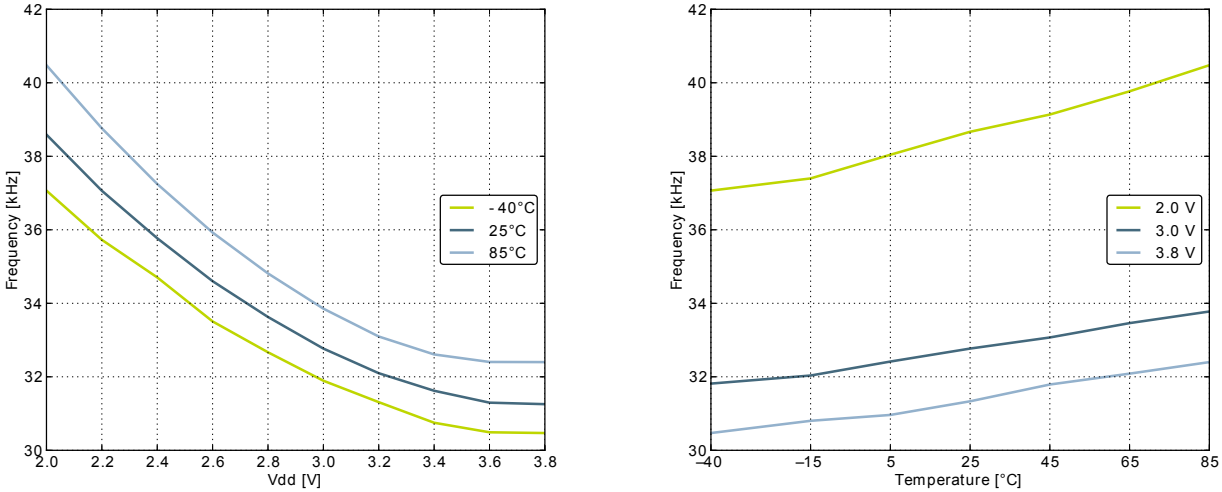
GPIO_Px_CTRL DRIVEMODE = HIGH

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25°C		31.3	32.768	34.3	kHz
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			361	492	nA
$TUNESTEP_{LFRCO}$	Frequency step for LSB change in TUNING value			202		Hz

Figure 3.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



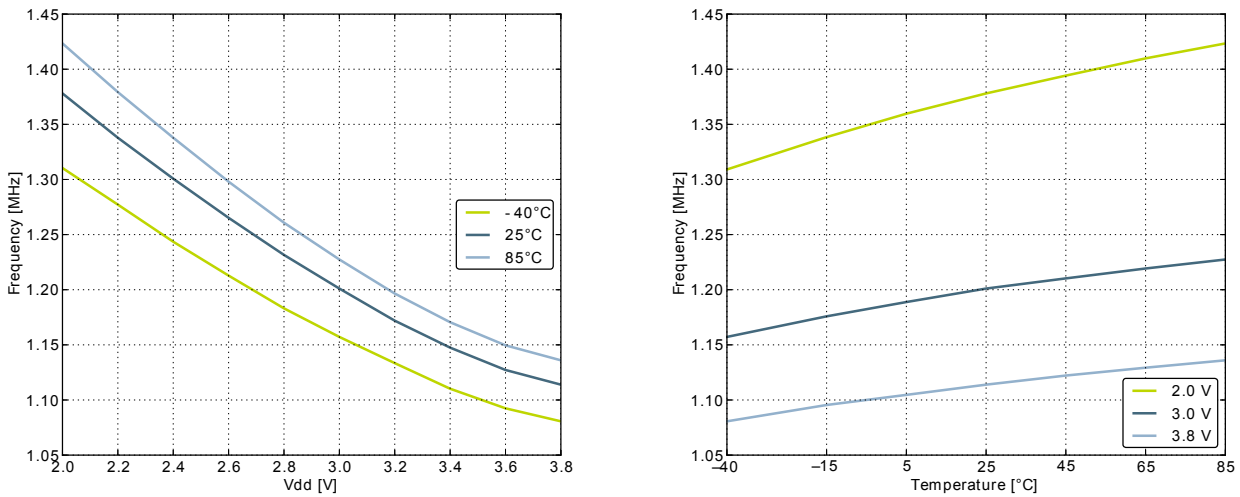
3.9.4 HFRCO

Table 3.11. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	24 MHz frequency band	23.28	24.0	24.72	MHz
		21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40	6.60	6.80	MHz
		1 MHz frequency band	1.15	1.20	1.25	MHz
$t_{HFRCO\_settling}$	Settling time after start-up	f_{HFRCO} = 14 MHz		0.6		Cycles
I_{HFRCO}	Current consumption	f_{HFRCO} = 24 MHz		158	184	µA
		f_{HFRCO} = 21 MHz		143	175	µA
		f_{HFRCO} = 14 MHz		113	140	µA
		f_{HFRCO} = 11 MHz		101	125	µA
		f_{HFRCO} = 6.6 MHz		84	105	µA
		f_{HFRCO} = 1.2 MHz		27	40	µA
$TUNESTEP_{H-FRCO}$	Frequency step for LSB change in TUNING value	24 MHz frequency band		66.8[1]		kHz
		21 MHz frequency band		52.8[1]		kHz
		14 MHz frequency band		36.9[1]		kHz
		11 MHz frequency band		30.1[1]		kHz
		7 MHz frequency band		18.0[1]		kHz
		1 MHz frequency band		3.4		kHz

[1]The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 21 MHz across operating conditions.

Figure 3.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature



Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, 2xV_{DD} reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		69		dB
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, 2xV_{DD} reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc

Table 3.18. IDAC Range 1 Source

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		14.4		µA
		Duty-cycled		10		nA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			3.2		µA
I_{STEP}	Step size			0.1		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = V_{DD} - 100mV		0.75		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		0.7		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		38.4		nA/V

Table 3.19. IDAC Range 1 Sink

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		19.4		µA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			3.2		µA
I_{STEP}	Step size			0.1		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = 200 mV		0.32		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		0.7		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		40.9		nA/V

Table 3.20. IDAC Range 2 Source

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		17.3		µA
		Duty-cycled		10		nA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			8.5		µA
I_{STEP}	Step size			0.5		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = V_{DD} - 100mV		1.22		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		2.8		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		96.6		nA/V

Table 3.21. IDAC Range 2 Sink

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		29.3		µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			8.5		µA
I_{STEP}	Step size			0.5		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = 200 mV		0.62		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		2.8		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		94.4		nA/V

Table 3.22. IDAC Range 3 Source

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		18.7		µA
		Duty-cycled		10		nA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			33.9		µA
I_{STEP}	Step size			2.0		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = V_{DD} - 100 mV		3.54		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		10.9		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		159.5		nA/V

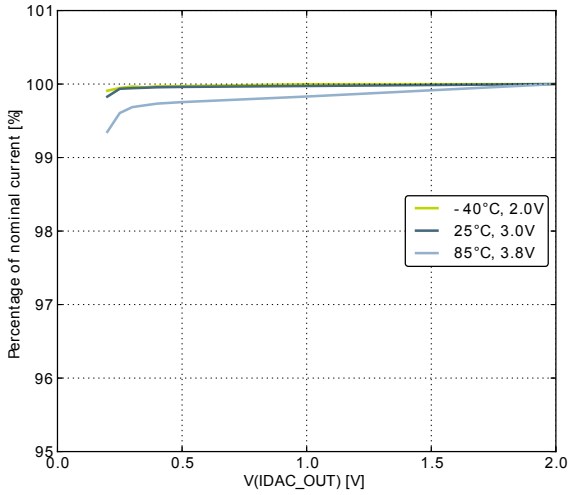
Table 3.23. IDAC Range 3 Sink

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		62.5		µA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			34.1		µA
I_{STEP}	Step size			2.0		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = 200 mV		1.75		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		10.9		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		148.6		nA/V

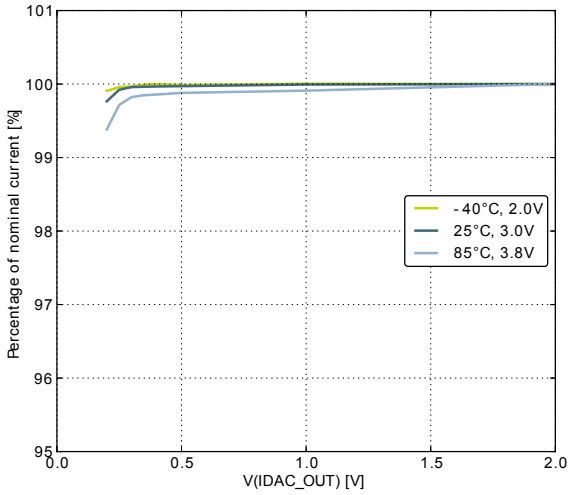
Table 3.24. IDAC

Symbol	Parameter	Min	Typ	Max	Unit
$t_{IDACSTART}$	Start-up time, from enabled to output settled		40		µs

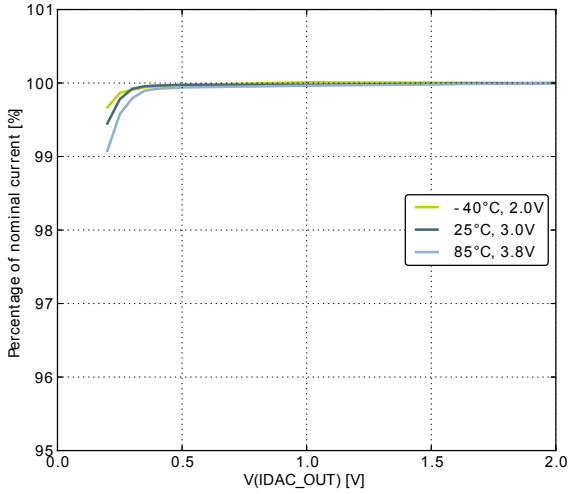
Figure 3.35. IDAC Sink Current as a function of voltage from IDAC_OUT



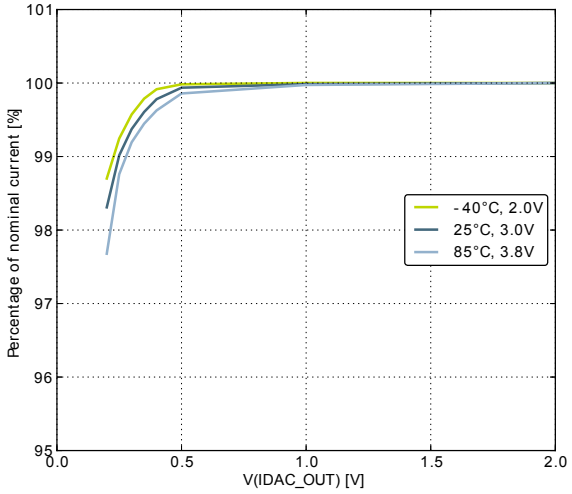
Range 0



Range 1

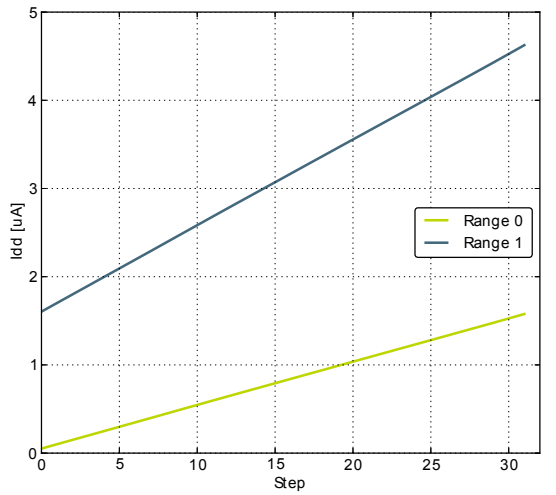


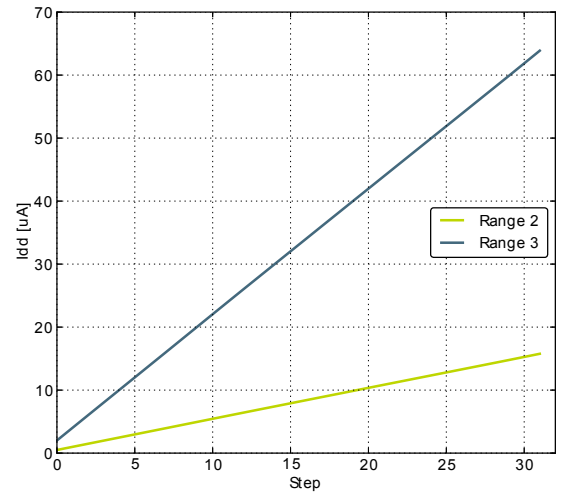
Range 2



Range 3

Figure 3.36. IDAC linearity





3.12 Analog Comparator (ACMP)

Table 3.25. ACMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.4	µA
		BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	15	µA
		BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	µA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		µA
		Internal voltage reference		5		µA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		40		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		70		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		101		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		132		kOhm
$t_{ACMPSTART}$	Startup time				10	µs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 47) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

3.13 Voltage Comparator (VCMP)

Table 3.26. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCMPIN}	Input voltage range			V_{DD}		V
V_{VCMPCM}	VCMP Common Mode voltage range			V_{DD}		V
I_{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.2	0.8	µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	35	µA
$t_{VCMPREF}$	Startup time reference generator	NORMAL		10		µs
$V_{VCMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{VCMPHYST}$	VCMP hysteresis			17		mV
$t_{VCMPSTART}$	Startup time				10	µs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD\ Trigger\ Level}=1.667V+0.034 \times TRIGLEVEL \quad (3.2)$$

3.14 I2C

Table 3.27. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		100[1]	kHz
t_{LOW}	SCL clock low time	4.7			µs
t_{HIGH}	SCL clock high time	4.0			µs
$t_{SU,DAT}$	SDA set-up time	250			ns
$t_{HD,DAT}$	SDA hold time	8		3450[2,3]	ns
$t_{SU,STA}$	Repeated START condition set-up time	4.7			µs
$t_{HD,STA}$	(Repeated) START condition hold time	4.0			µs
$t_{SU,STO}$	STOP condition set-up time	4.0			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs

[1]For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32HG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 5).

CSP36 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
				LEU0_RX #5 USB_DP	
A3	VSS	Ground.			
A4	IOVDD_5	Digital IO power supply 5.			
A5	PE12	ADC0_CH0	TIM1_CC2 #1 TIM2_CC1 #3	US0_RX #3 US0_CLK #0/6 I2C0_SDA #6	CMU_CLK1 #2 PRS_CH1 #3
A6	PA0		TIM0_CC1 #6 TIM0_CC0 #0/1/4 PCNT0_S0IN #4	USB_DMPU #0 US1_RX #4 LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
B1	USB_VREGI				
B2	PF0		TIM0_CC0 #5	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0 BOOT_TX
B3	PF2		TIM0_CC2 #5/6 TIM2_CC0 #3	US1_TX #4 LEU0_TX #4	CMU_CLK0 #3 PRS_CH0 #3 GPIO_EM4WU4
B4	PE10		TIM1_CC0 #1	US0_TX #0	PRS_CH2 #2
B5	PE13	ADC0_CH1	TIM2_CC2 #3	US0_TX #3 US0_CS #0/6 I2C0_SCL #6	ACMP0_O #0 PRS_CH2 #3 GPIO_EM4WU5
B6	PA1		TIM0_CC0 #6 TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
C1	USB_VREGO				
C2	VDD_DREG	Power supply for on-chip voltage regulator.			
C3	PF1		TIM0_CC1 #5	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0 GPIO_EM4WU3 BOOT_RX
C4	PE11		TIM1_CC1 #1	US0_RX #0	PRS_CH3 #2
C5	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
C6	IOVDD_0	Digital IO power supply 0.			
D1	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
D2	VSS_DREG	Ground for on-chip voltage regulator.			
D3	PD6	ADC0_CH6	TIM1_CC0 #4 PCNT0_S0IN #3	US1_RX #2/3 I2C0_SDA #1	ACMP0_O #2
D4	PC1	ACMP0_CH1	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5/6 US1_TX #5 US1_RX #0 I2C0_SCL #4	PRS_CH3 #0
D5	PC0	ACMP0_CH0	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5/6 US1_TX #0 US1_CS #5 I2C0_SDA #4	PRS_CH2 #0
D6	VSS	Ground.			
E1	PD7	ADC0_CH7	TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2/3 I2C0_SCL #1	CMU_CLK0 #2
E2	VSS	Ground.			
E3	AVSS_0	Analog ground 0.			
E4	AVDD_0	Analog power supply 0.			
E5	RESETn	Reset input, active low.			

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
US1_CS	PB8		PF1	PC14	PC14	PC0		USART1 chip select input / output.
US1_RX	PC1		PD6	PD6	PA0			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0		PD7	PD7	PF2	PC1		USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PC14							USB D- pin.
USB_DMPU	PA0							USB D- Pullup control.
USB_DP	PC15							USB D+ pin.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

4.3 GPIO Pinout Overview

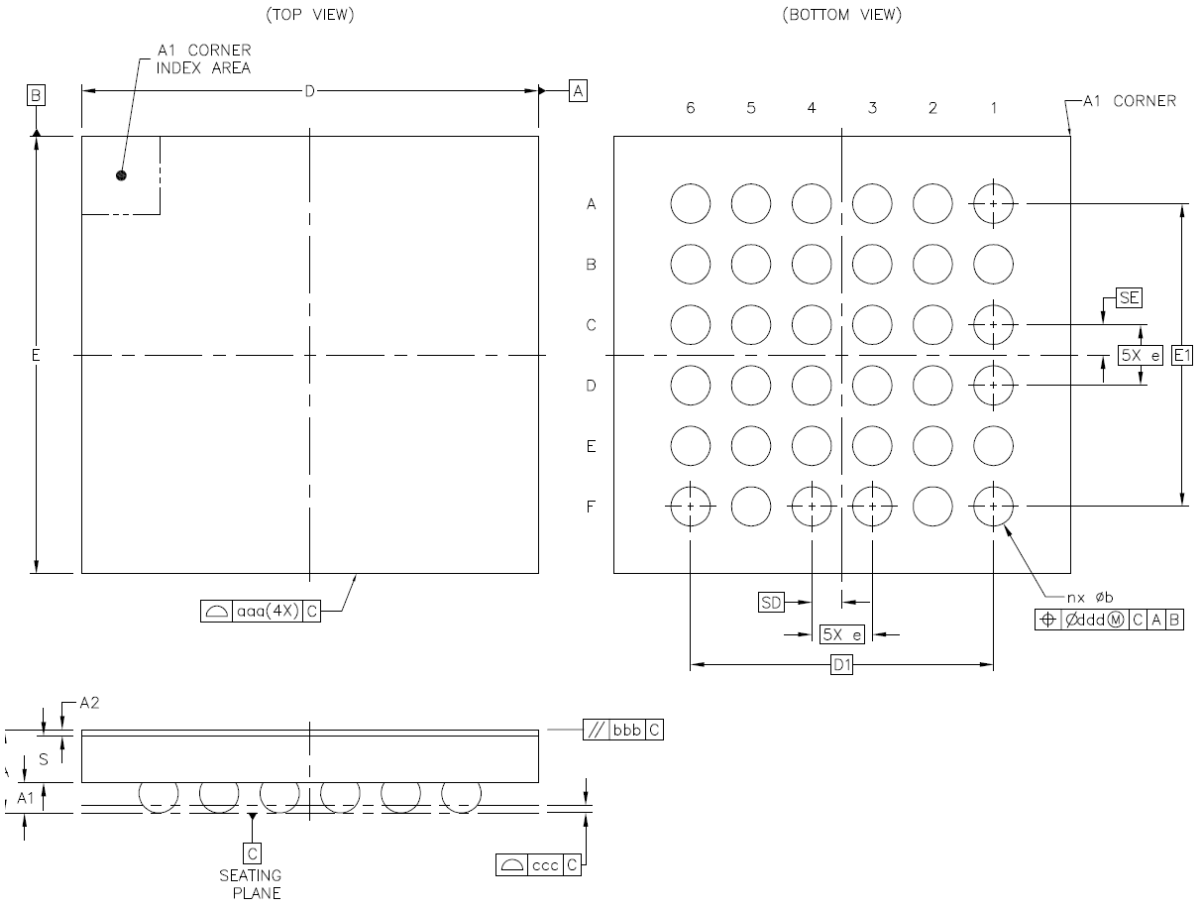
The specific GPIO pins available in *EFM32HG350* is shown in Table 4.3 (p. 56) . Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	PA2	PA1	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	-	-	-	-	-	-	-	-	-	-	-	-	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	PD5	-	-	-	-	-
Port E	-	-	PE13	PE12	PE11	PE10	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	-	PF2	PF1	PF0

4.4 CSP36 Package

Figure 4.2. CSP36



Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Primary datum “C” and seating plane are defined by the spherical crowns of the solder balls.
4. Dimension “b” is measured at the maximum solder bump diameter, parallel to primary datum “C”.
5. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Table 4.4. CSP36 (Dimensions in mm)

Symbol	A	A1	A2	b	S	D	E	e	D1	E1	SD	SE	n	aaa	bbb	ccc	ddd
Min	0.491	0.17	0.036	0.23	0.3075	3.016 BSC.	2.891 BSC.	0.40 BSC.	2.00 BSC.	2.00 BSC.	0.2	0.2	36	0.03	0.06	0.05	0.015
Nom	0.55	-	0.040	-	0.31												
Max	0.609	0.23	0.044	0.29	0.3125												

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx

List of Tables

List of Equations