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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 25MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 22 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 4x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 36-UFBGA, CSPBGA |
| Supplier Device Package | 36-CSP (3.02x2.89) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32hg350f64g-b-csp36r |

There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

### 2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

### 2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32HG.

### 2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32HG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

### 2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32HG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

### 2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

### 2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

### 2.1.10 Low Energy USB

The unique Low Energy USB peripheral provides a full-speed USB 2.0 compliant device controller and PHY with ultra-low current consumption. The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation, and includes a dedicated USB oscillator with clock recovery mechanism for crystal-free operation. No external components are required. The Low Energy Mode ensures the current consumption is optimized and enables USB communication on a strict power budget. The USB device includes an internal dedicated descriptor-based Scatter/Gather DMA and supports up to 3 OUT endpoints and 3 IN endpoints, in addition to endpoint 0. The on-chip PHY includes software controllable pull-up and pull-down resistors.

### 2.1.11 Inter-Integrated Circuit Interface (I2C)

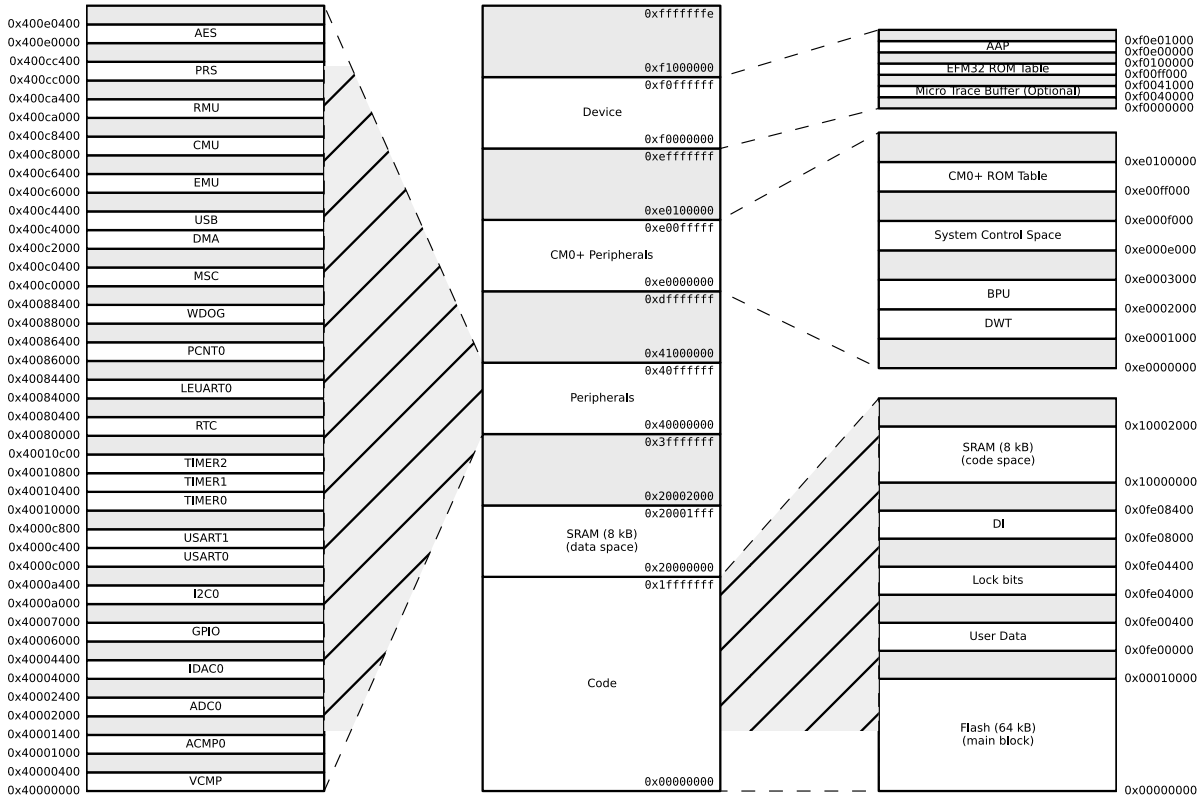
The $I^2C$ module provides an interface between the MCU and a serial $I^2C$-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s.

| Module | Configuration | Pin Connections |
|---|---|---|
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:5] |
| IDAC0 | Full configuration | IDAC0_OUT |
| AES | Full configuration | NA |
| GPIO | 22 pins | Available pins are shown in Table 4.3 (p. 56) |

## 2.3 Memory Map

The *EFM32HG350* memory map is shown in Figure 2.2 (p. 7), with RAM and Flash sizes for the largest memory configuration.

***Figure 2.2. EFM32HG350 Memory Map with largest RAM and Flash sizes***



in plastic, they are susceptible to mechanical damage and may be sensitive to light. When WLCSPs must be used in an environment exposed to light, it may be necessary to cover the top and sides with an opaque material.

## 3.4 Current Consumption

***Table 3.3. Current Consumption***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{EM0}$ | EM0 current. No prescaling. Running prime number calculation code from Flash. | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 148 | 158 | µA/MHz |
| | | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 153 | 163 | µA/MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 161 | 172 | µA/MHz |
| | | 24 MHz USHFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 163 | 174 | µA/MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 127 | 137 | µA/MHz |
| | | 24 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 129 | 139 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 131 | 140 | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 134 | 143 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 134 | 143 | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 137 | 145 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 136 | 144 | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 139 | 148 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 142 | 150 | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 146 | 154 | µA/MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 184 | 196 | µA/MHz |

## 3.4.2 EM1 Current Consumption

***Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 24 MHz***

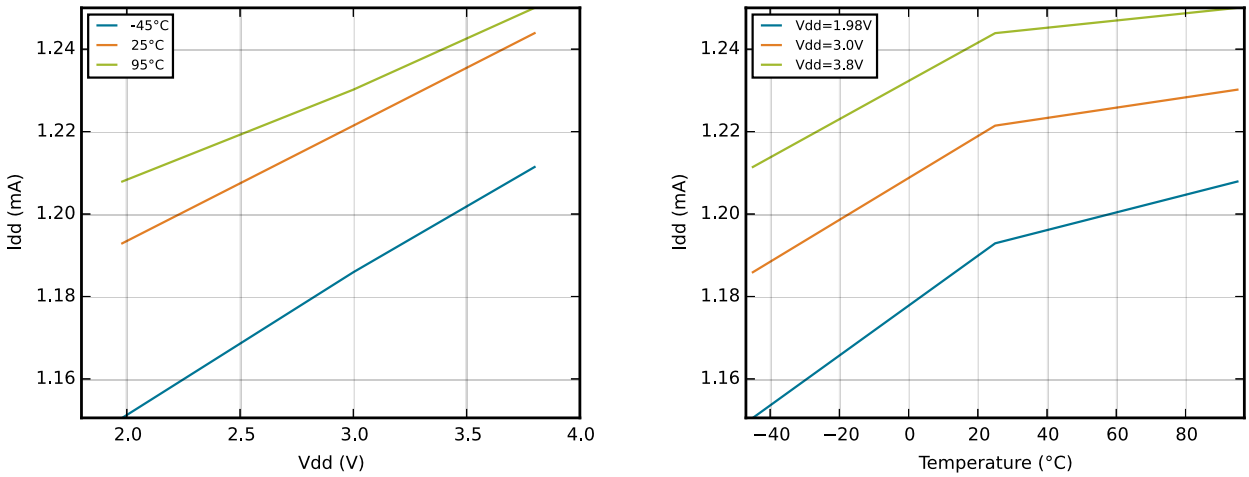



***Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz***

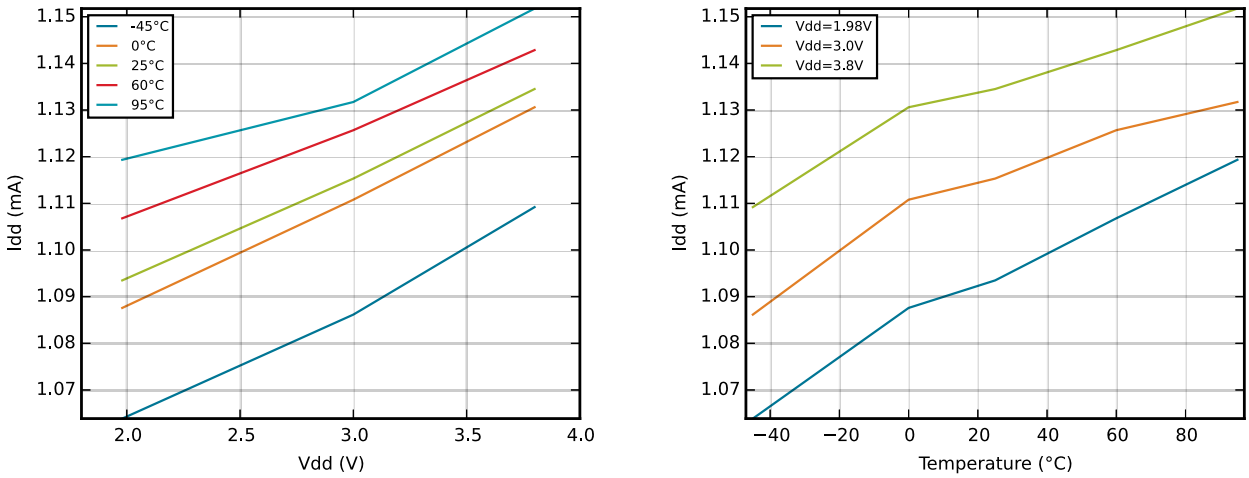
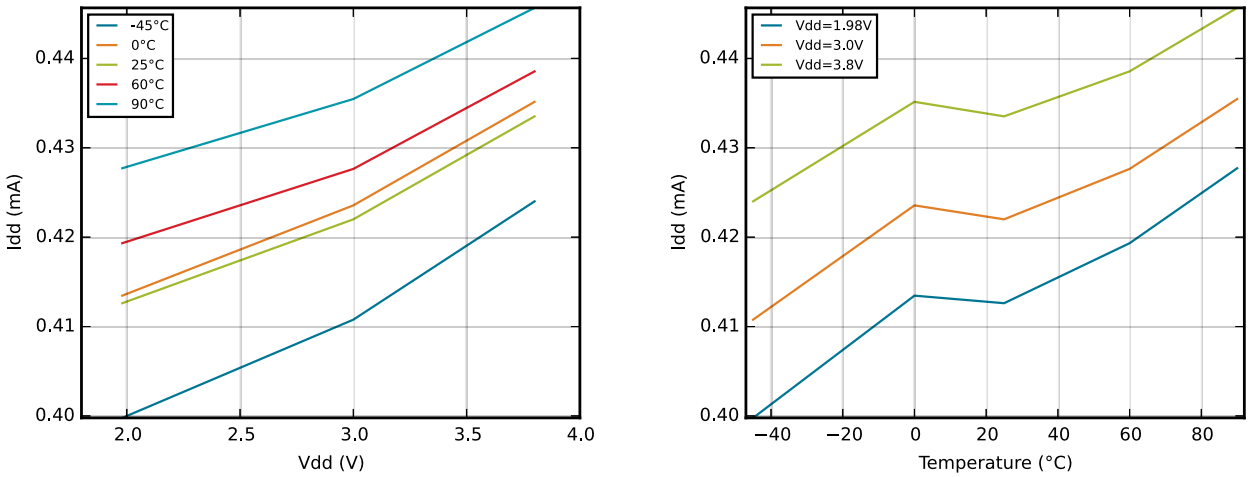


***Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6 MHz***




## 3.4.3 EM2 Current Consumption

***Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.***

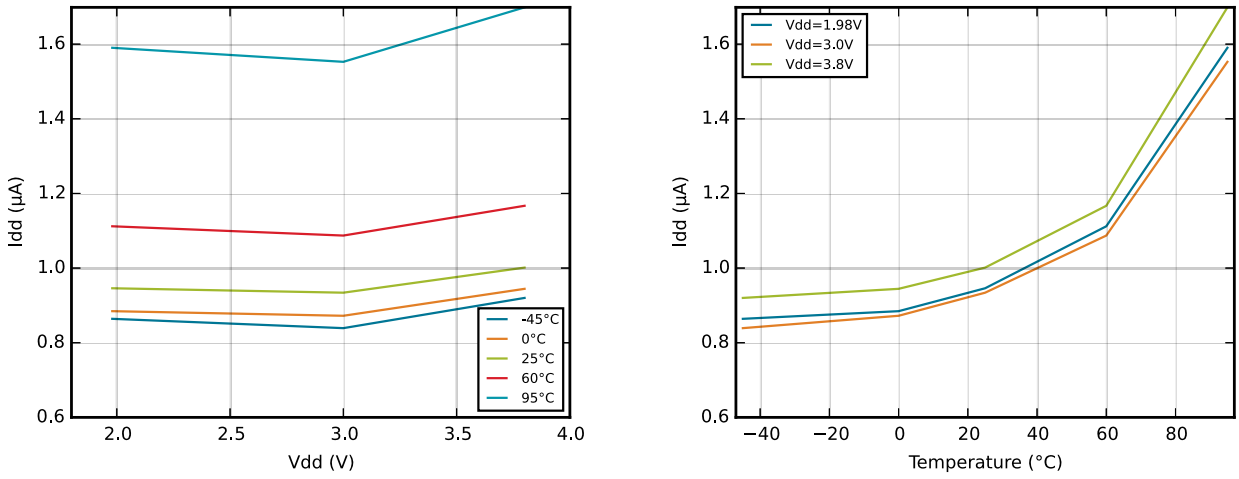
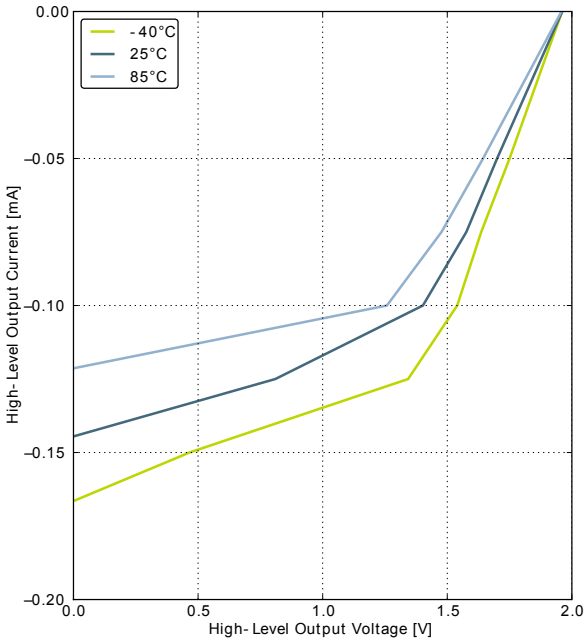
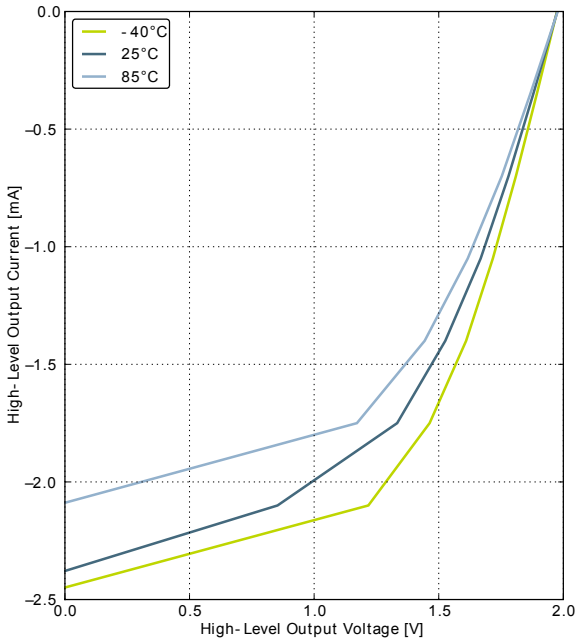


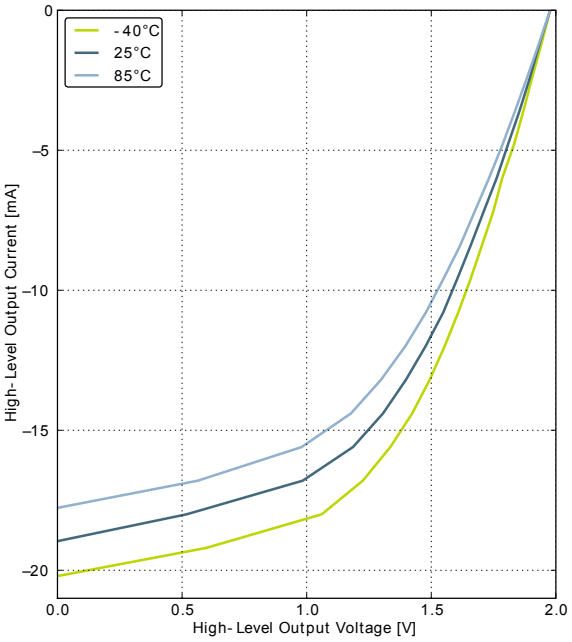
***Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage***



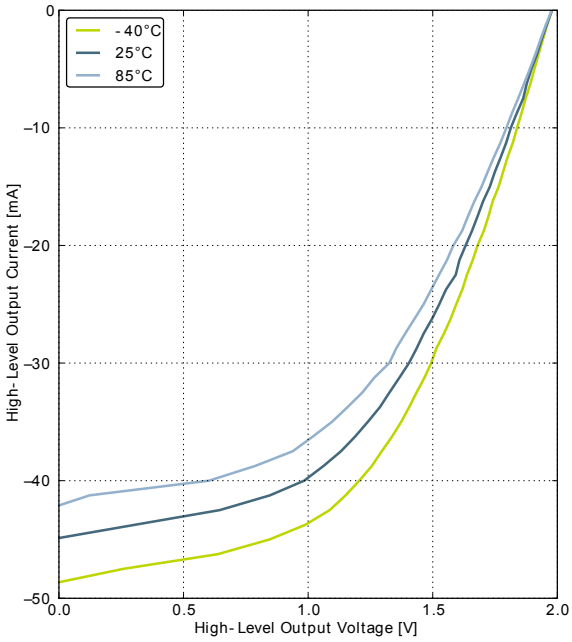

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

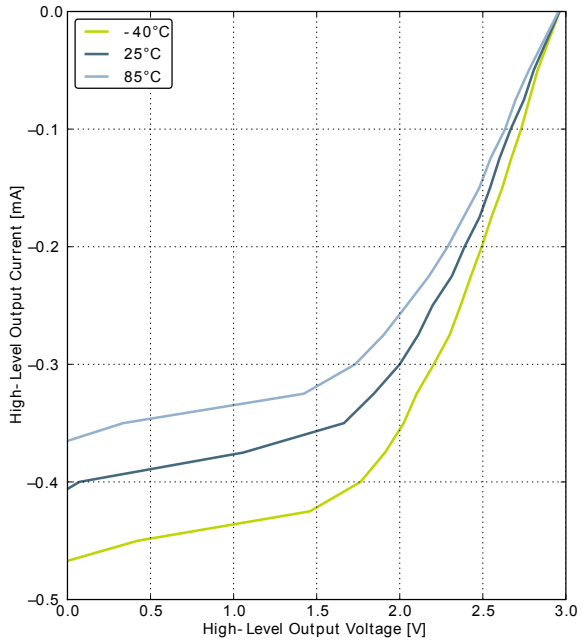



GPIO_Px_CTRL DRIVEMODE = STANDARD

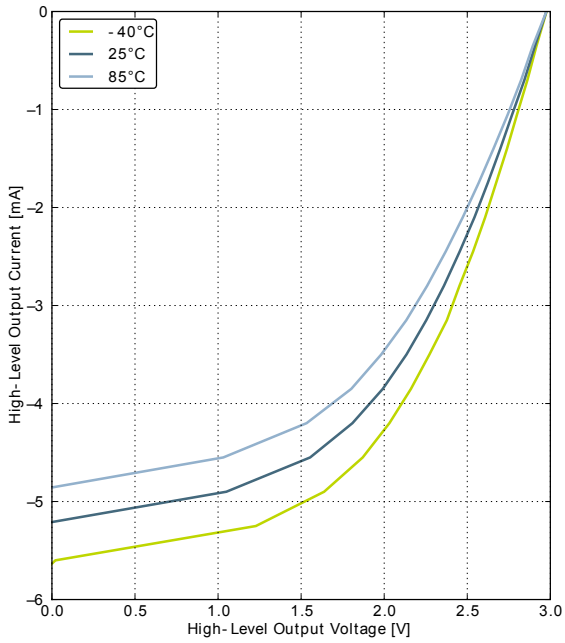



GPIO_Px_CTRL DRIVEMODE = HIGH

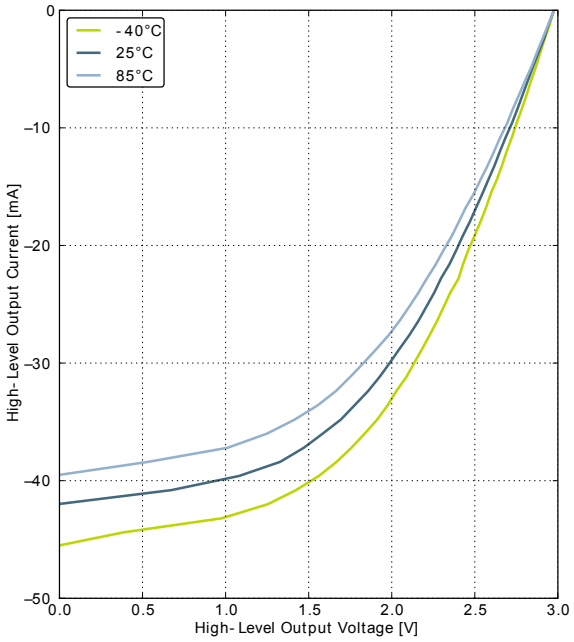
***Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage***



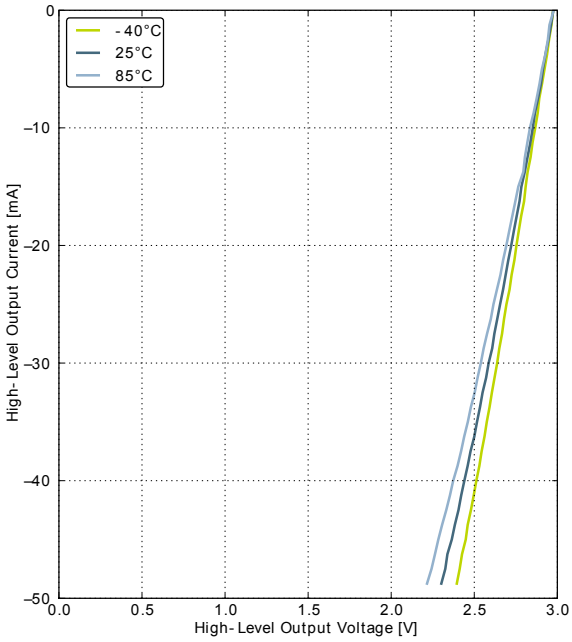

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW




GPIO_Px_CTRL DRIVEMODE = STANDARD




GPIO_Px_CTRL DRIVEMODE = HIGH

# 3.9 Oscillators

## 3.9.1 LFXO

***Table 3.8. LFXO***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LFXO}$ | Supported nominal crystal frequency | | | 32.768 | | kHz |
| $ESR_{LFXO}$ | Supported crystal equivalent series resistance (ESR) | | | 30 | 120 | kOhm |
| $C_{LFXOL}$ | Supported crystal external load range | | 5 | | 25 | pF |
| $I_{LFXO}$ | Current consumption for core and buffer after startup. | ESR=30 kOhm, $C_L$=10 pF, LFXOBOOST in CMU_CTRL is 1 | | 190 | | nA |
| $t_{LFXO}$ | Start- up time. | ESR=30 kOhm, $C_L$=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1 | | 1100 | | ms |

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

## 3.9.2 HFXO

***Table 3.9. HFXO***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HFXO}$ | Supported frequency, any mode | | 4 | | 25 | MHz |
| $ESR_{HFXO}$ | Supported crystal equivalent series resistance (ESR) | Crystal frequency 25 MHz | | 30 | 100 | Ohm |
| | | Crystal frequency 4 MHz | | 400 | 1500 | Ohm |
| $g_{mHFXO}$ | The transconductance of the HFXO input transistor at crystal startup | HFXOBOOST in CMU_CTRL equals 0b11 | 20 | | | mS |
| $C_{HFXOL}$ | Supported crystal external load range | | 5 | | 25 | pF |
| $I_{HFXO}$ | Current consumption for HFXO after startup | 4 MHz: ESR=400 Ohm, $C_L$=20 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 85 | | µA |
| | | 25 MHz: ESR=30 Ohm, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 165 | | µA |
| $t_{HFXO}$ | Startup time | 25 MHz: ESR=30 Ohm, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 785 | | µs |

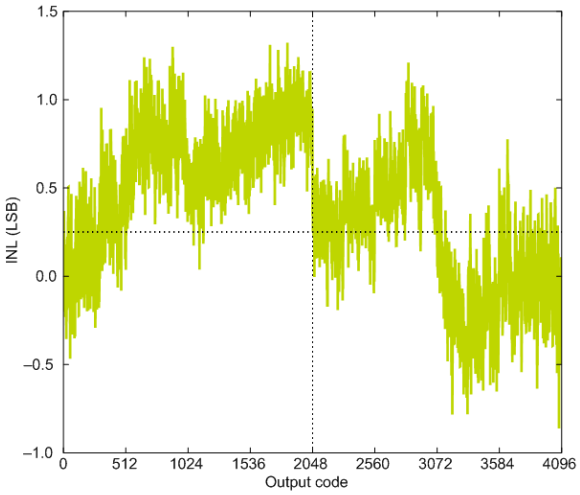
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCREFIN\_CH6}$ | Input range of external positive reference voltage on channel 6 | See $V_{ADCREFIN}$ | 0.625 | | $V_{DD}$ | V |
| $V_{ADCCMIN}$ | Common mode input range | | 0 | | $V_{DD}$ | V |
| $I_{ADCIN}$ | Input current | 2pF sampling capacitors | | <100 | | nA |
| $CMRR_{ADC}$ | Analog input common mode rejection ratio | | | 65 | | dB |
| $I_{ADC}$ | Average active current | 1 MSamples/s, 12 bit, external reference | | 392 | 510 | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00 | | 67 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01 | | 63 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b10 | | 64 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b11 | | 244 | | µA |
| $I_{ADCREF}$ | Current consumption of internal voltage reference | Internal voltage reference | | 65 | | µA |
| $C_{ADCIN}$ | Input capacitance | | | 2 | | pF |
| $R_{ADCIN}$ | Input ON resistance | | 1 | | | MOhm |
| $R_{ADCFILT}$ | Input RC filter resistance | | | 10 | | kOhm |
| $C_{ADCFILT}$ | Input RC filter/decoupling capacitance | | | 250 | | fF |
| $f_{ADCCLK}$ | ADC Clock Frequency | | | | 13 | MHz |
| $t_{ADCCONV}$ | Conversion time | 6 bit | 7 | | | ADCCLK Cycles |
| | | 8 bit | 11 | | | ADCCLK Cycles |
| | | 12 bit | 13 | | | ADCCLK Cycles |
| $t_{ADCACQ}$ | Acquisition time | Programmable | 1 | | 256 | ADCCLK Cycles |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 76 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 78 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 68 | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 79 | | dBc |
| $V_{ADCOFFSET}$ | Offset voltage | After calibration, single ended | -4 | 0.3 | 4 | mV |
| | | After calibration, differential | | 0.3 | | mV |
| $TGRAD_{ADCTH}$ | Thermometer output gradient | | | -1.92 | | mV/°C |
| | | | | -6.3 | | ADC Codes/ °C |
| $DNL_{ADC}$ | Differential non-linearity (DNL) | $V_{DD}$= 3.0 V, external 2.5V reference | -1 | ±0.7 | 4 | LSB |
| $INL_{ADC}$ | Integral non-linearity (INL), End point method | | | ±1.6 | ±3 | LSB |
| $MC_{ADC}$ | No missing codes | | 11.999[1] | 12 | | bits |
| $VREF_{ADC}$ | ADC Internal Voltage Reference | Internal 1.25V, $V_{DD}$ = 3V, 25°C | 1.248 | 1.254 | 1.262 | V |
| | | Internal 1.25V, Full temperature and supply range | 1.188 | 1.254 | 1.302 | V |
| | | Internal 2.5V, $V_{DD}$ = 3V, 25°C | 2.492 | 2.506 | 2.520 | V |
| | | Internal 2.5V, Full temperature and supply range | 2.402 | 2.506 | 2.600 | V |

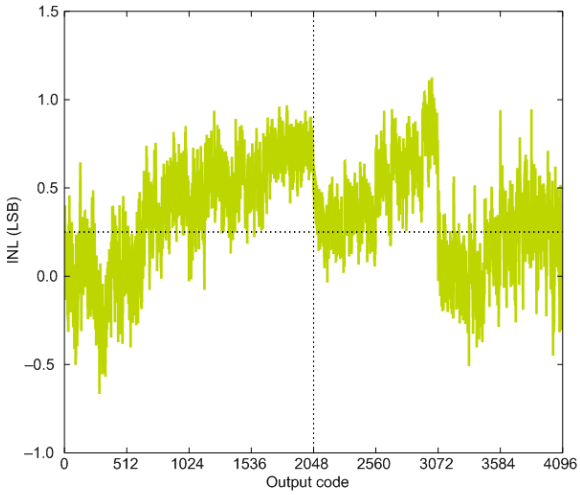
[1]On the average every ADC will have one missing code, most likely to appear around 2048 ± n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.26 (p. 37) and Figure 3.27 (p. 37) , respectively.

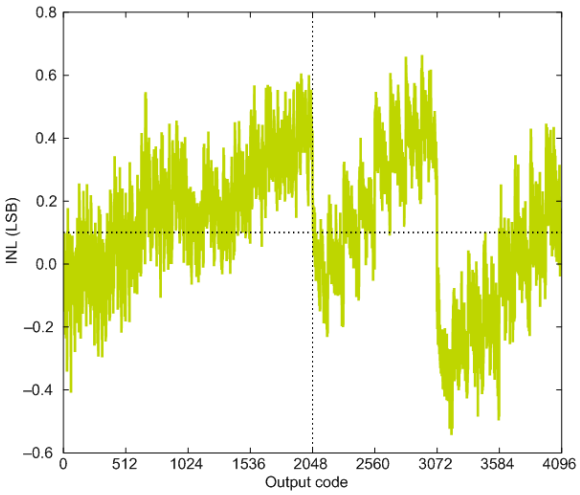
***Figure 3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C***



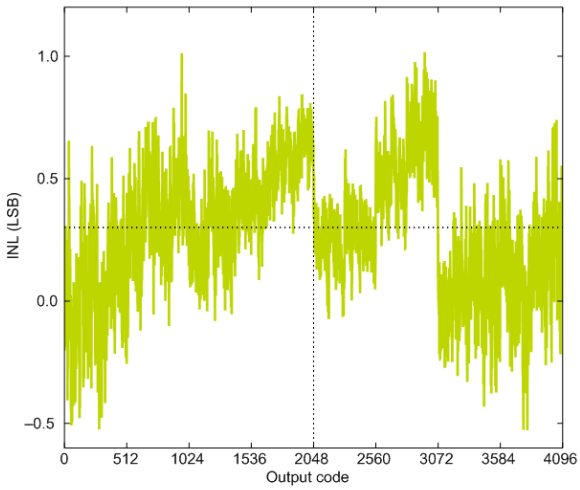

1.25V Reference



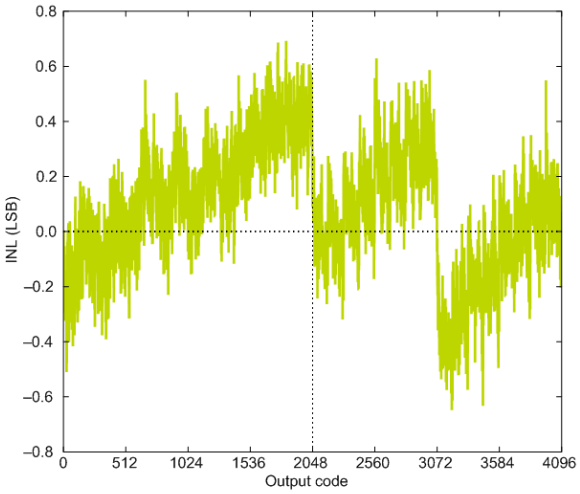

2.5V Reference




2XVDDVSS Reference

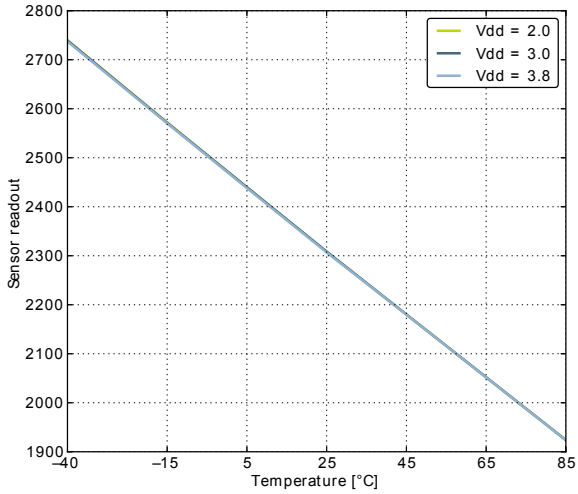



5VDIFF Reference




VDD Reference

*Figure 3.33. ADC Temperature sensor readout*




# 3.11 Current Digital Analog Converter (IDAC)

*Table 3.16. IDAC Range 0 Source*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 13.0 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 0.85 | | µA |
| $I_{STEP}$ | Step size | | | 0.05 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = $V_{DD}$ - 100mV | | 0.79 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0V, STEPSEL=0x10 | | 0.3 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 11.7 | | nA/V |

*Table 3.17. IDAC Range 0 Sink*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 15.1 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 0.85 | | µA |
| $I_{STEP}$ | Step size | | | 0.05 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 0.30 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.2 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 12.5 | | nA/V |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 8.5 | | µA |
| $I_{STEP}$ | Step size | | | 0.5 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 0.62 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 2.8 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 94.4 | | nA/V |

*Table 3.22. IDAC Range 3 Source*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 18.7 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 33.9 | | µA |
| $I_{STEP}$ | Step size | | | 2.0 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = $V_{DD}$ - 100 mV | | 3.54 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 10.9 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 159.5 | | nA/V |

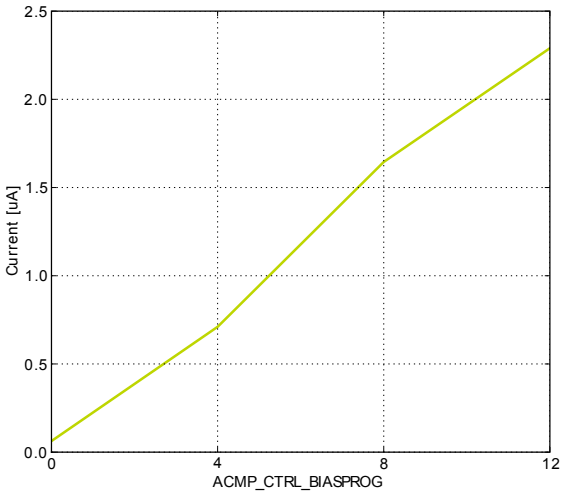
*Table 3.23. IDAC Range 3 Sink*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 62.5 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 34.1 | | µA |
| $I_{STEP}$ | Step size | | | 2.0 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 1.75 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 10.9 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 148.6 | | nA/V |

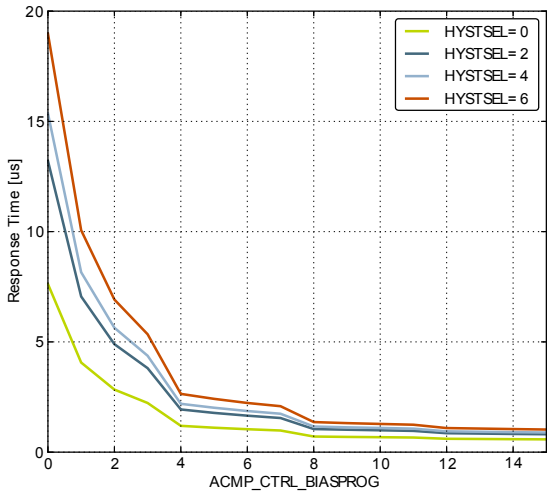
*Table 3.24. IDAC*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{IDACSTART}$ | Start-up time, from enabled to output settled | | 40 | | µs |

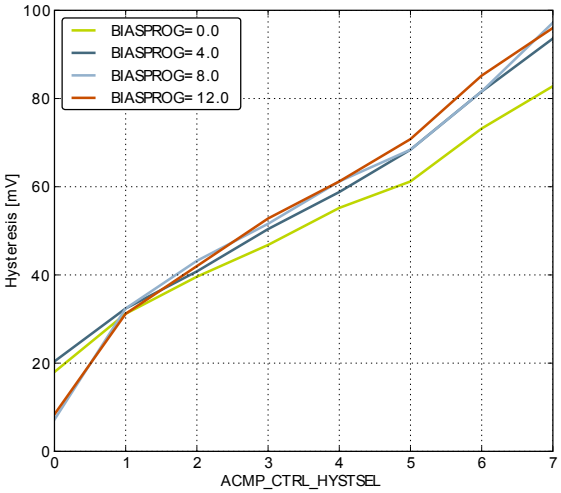
***Figure 3.37. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1***




Current consumption, HYSTSEL = 4




Response time , $V_{cm}$ = 1.25V, CP+ to CP- = 100mV




Hysteresis

# 3.13 Voltage Comparator (VCMP)

***Table 3.26. VCMP***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{VCMPIN}$ | Input voltage range | | | $V_{DD}$ | | V |
| $V_{VCMPCM}$ | VCMP Common Mode voltage range | | | $V_{DD}$ | | V |
| $I_{VCMP}$ | Active current | BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register | | 0.2 | 0.8 | µA |
| | | BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0. | | 22 | 35 | µA |
| $t_{VCMPREF}$ | Startup time reference generator | NORMAL | | 10 | | µs |
| $V_{VCMPOFFSET}$ | Offset voltage | Single ended | | 10 | | mV |
| | | Differential | | 10 | | mV |
| $V_{VCMPHYST}$ | VCMP hysteresis | | | 17 | | mV |
| $t_{VCMPSTART}$ | Startup time | | | | 10 | µs |

The $V_{DD}$ trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

***VCMP Trigger Level as a Function of Level Setting***

$$V_{DD\ Trigger\ Level}=1.667V+0.034 \times TRIGLEVEL \quad (3.2)$$

# 3.14 I2C

***Table 3.27. I2C Standard-mode (Sm)***

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 100[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 4.7 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 4.0 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 250 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | 3450[2,3] | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 4.7 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 4.0 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 4.0 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | | | µs |

[1]For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32HG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 5).

# 3.16 Digital Peripherals

***Table 3.31. Digital Peripherals***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{USART}$ | USART current | USART idle current, clock enabled | | 7.5 | | µA/MHz |
| $I_{LEUART}$ | LEUART current | LEUART idle current, clock enabled | | 150 | | nA |
| $I_{I2C}$ | I2C current | I2C idle current, clock enabled | | 6.25 | | µA/MHz |
| $I_{TIMER}$ | TIMER current | TIMER_0 idle current, clock enabled | | 8.75 | | µA/MHz |
| $I_{PCNT}$ | PCNT current | PCNT idle current, clock enabled | | 100 | | nA |
| $I_{RTC}$ | RTC current | RTC idle current, clock enabled | | 100 | | nA |
| $I_{AES}$ | AES current | AES idle current, clock enabled | | 2.5 | | µA/MHz |
| $I_{GPIO}$ | GPIO current | GPIO idle current, clock enabled | | 5.31 | | µA/MHz |
| $I_{PRS}$ | PRS current | PRS idle current | | 2.81 | | µA/MHz |
| $I_{DMA}$ | DMA current | Clock enable | | 8.12 | | µA/MHz |

| CSP36 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| | | To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| E6 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| F1 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| F2 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| F3 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| F4 | AVDD_1 | Analog power supply 1. | | | |
| F5 | PB11 | IDAC0_OUT | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| F6 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |

## 4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 54). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

***Note***

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

***Table 4.2. Alternate functionality overview***

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | PD6 | PB11 | | | | Analog comparator ACMP0, digital output. |
| ADC0_CH0 | PE12 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PE13 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | PF2 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | PB11 | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_CS | PB8 | | PF1 | PC14 | PC14 | PC0 | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | PD6 | PA0 | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | PF2 | PC1 | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PC14 | | | | | | | USB D- pin. |
| USB_DMPU | PA0 | | | | | | | USB D- Pullup control. |
| USB_DP | PC15 | | | | | | | USB D+ pin. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

## 4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32HG350* is shown in Table 4.3 (p. 56) . Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

***Table 4.3. GPIO Pinout***

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

# List of Figures

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ZERO
ARM Cortex-M0+
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ARM Cortex-M3
WONDER
ARM Cortex-M4