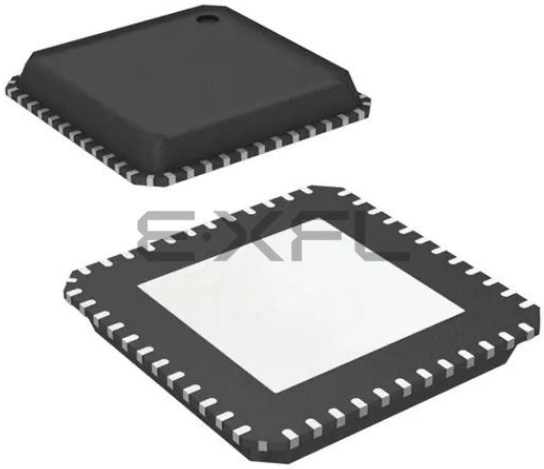

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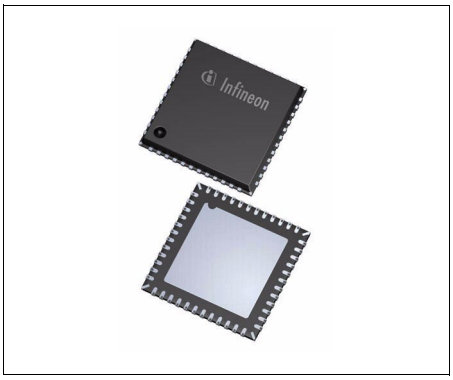
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (64kB)
Controller Series	-
RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9867qxa20xuma1

1 Overview



VQFN-48-31

Summary of Features

- 32 bit ARM Cortex M3 Core
  - up to 24 MHz clock frequency
  - one clock per machine cycle architecture
- On-chip memory
  - 64 kByte Flash including
  - 4 kByte EEPROM (emulated in Flash)
  - 512 Byte 100 Time Programmable Memory (100TP)
  - 6 kByte RAM
  - Boot ROM for startup firmware and Flash routines
- On-chip OSC and PLL for clock generation
  - PLL loss-of-lock detection
- MOSFET driver including charge pump
- 10 general-purpose I/O Ports (GPIO)
- 5 analog inputs, 10-bit A/D Converter (ADC1)
- 16-bit timers - GPT12, Timer 2, Timer 21 and Timer 3
- Capture/compare unit for PWM signal generation (CCU6)
- 2 full duplex serial interfaces (UART) with LIN support (for UART1 only)
- 2 synchronous serial channels (SSC)
- On-chip debug support via 2-wire SWD
- 1 LIN 2.2 transceiver
- 1 high voltage monitoring input
- Single power supply from 5.5 V to 27 V
- Extended power supply voltage range from 3 V to 28 V
- Low-dropout voltage regulators (LDO)
- High speed operational amplifier for motor current sensing via shunt
- 5 V voltage supply for external loads (e.g. Hall sensor)
- Core logic supply at 1.5 V
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes
  - MCU slow-down Mode
  - Sleep Mode
  - Stop Mode
  - Cyclic wake-up Sleep Mode
- Power-on and undervoltage/brownout reset generator

Type	Package	Marking
TLE9867QXA20	VQFN-48-31	

5.2.1 Block Diagram

The following figure shows the structure of the Power Management Unit. **Table 4** describes the submodules in more detail.

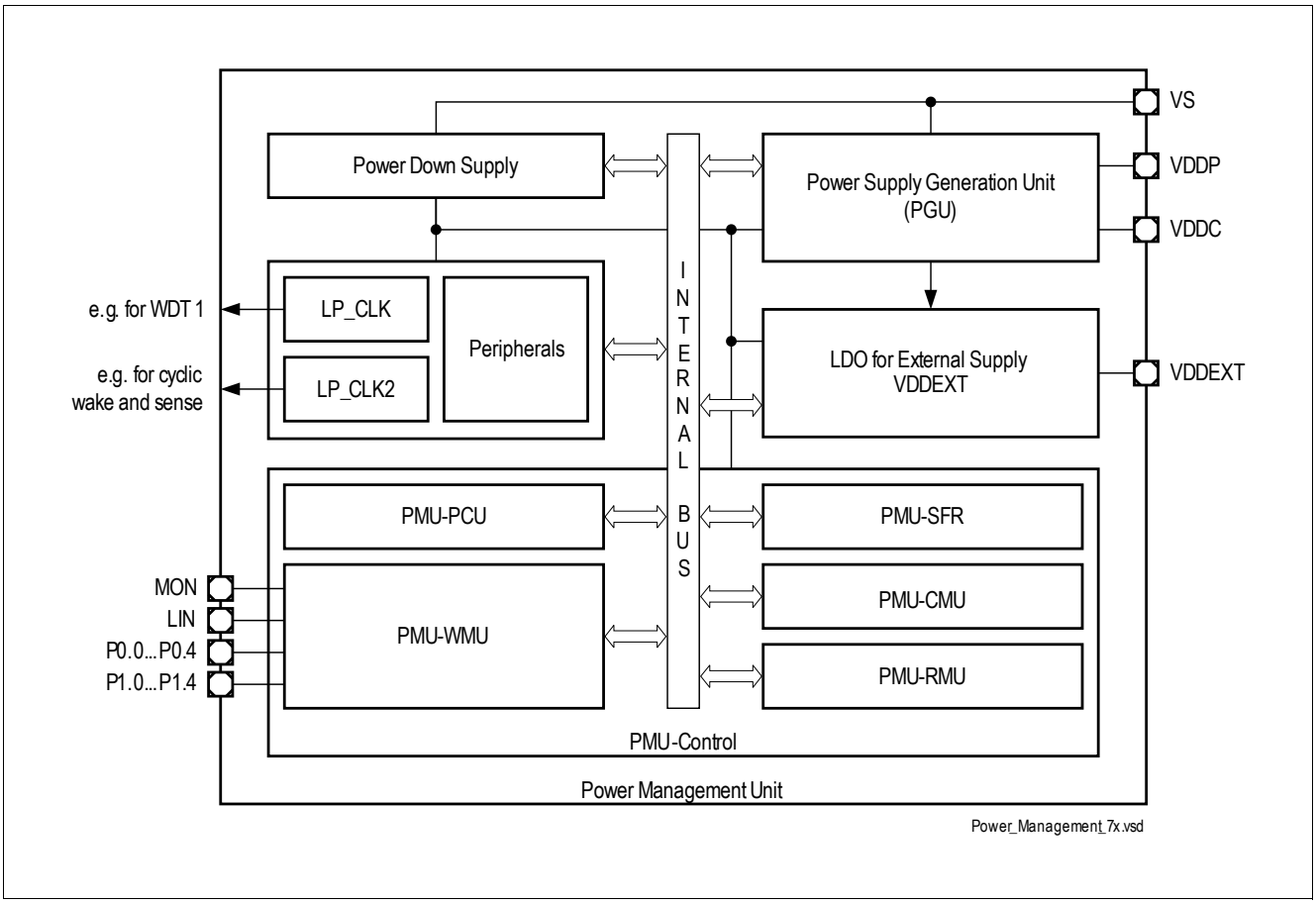


Figure 3 Power Management Unit Block Diagram

Table 4 Description of PMU Submodules

Mod. Name	Modules	Functions
Power Down Supply	Independent supply voltage generation for PMU	This supply is dedicated to the PMU to ensure an independent operation from generated power supplies (VDDP, VDDC).
LP_CLK (= 18 MHz)	- Clock source for all PMU submodules - Backup clock source for System - Clock source for WDT1	This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL Clock failure and as an independent clock source for WDT1.
LP_CLK2 (= 100 kHz)	Clock source for PMU	This ultra low power oscillator generates the clock for the PMU in Stop Mode and in the cyclic modes.
Peripherals	Peripheral blocks of PMU	These blocks include the analog peripherals to ensure a stable and fail-safe PMU startup and operation (bandgap, bias).

WDT1 (System Watchdog)

- LP_CLK clock source for all PMU submodules and WDT1

ICU (Interrupt Control Unit)

- PREWARN_SUP_NMI supply prewarning NMI request
- PREWARN_SUP_INT supply prewarning interrupt
- grouping of peripheral interrupts for external interupt nodes:
  - grouping single peripheral interrupts for interrupt node INT<2> (Measurement Unit (MU))
  - grouping single peripheral interrupts for interrupt node INT<3> (ADC1-VAREF)
  - grouping single peripheral interrupts for interrupt node INT<10> (UART1-LIN Transceiver)
  - grouping single peripheral interrupts for interrupt node INT<14> (Bridge Driver)

10 Address Space Organization

The TLE9867QXA20 manipulates operands in the following memory spaces:

- 64 KByte of Flash memory in code space
- 32 KByte Boot ROM memory in code space (used for boot code and IP storage)
- 6 KByte RAM memory in code space and data space (RAM can be read/written as program memory or external data memory)
- Special function registers (SFRs) in peripheral space

The figure below shows the detailed address alignment of TLE9867QXA20:

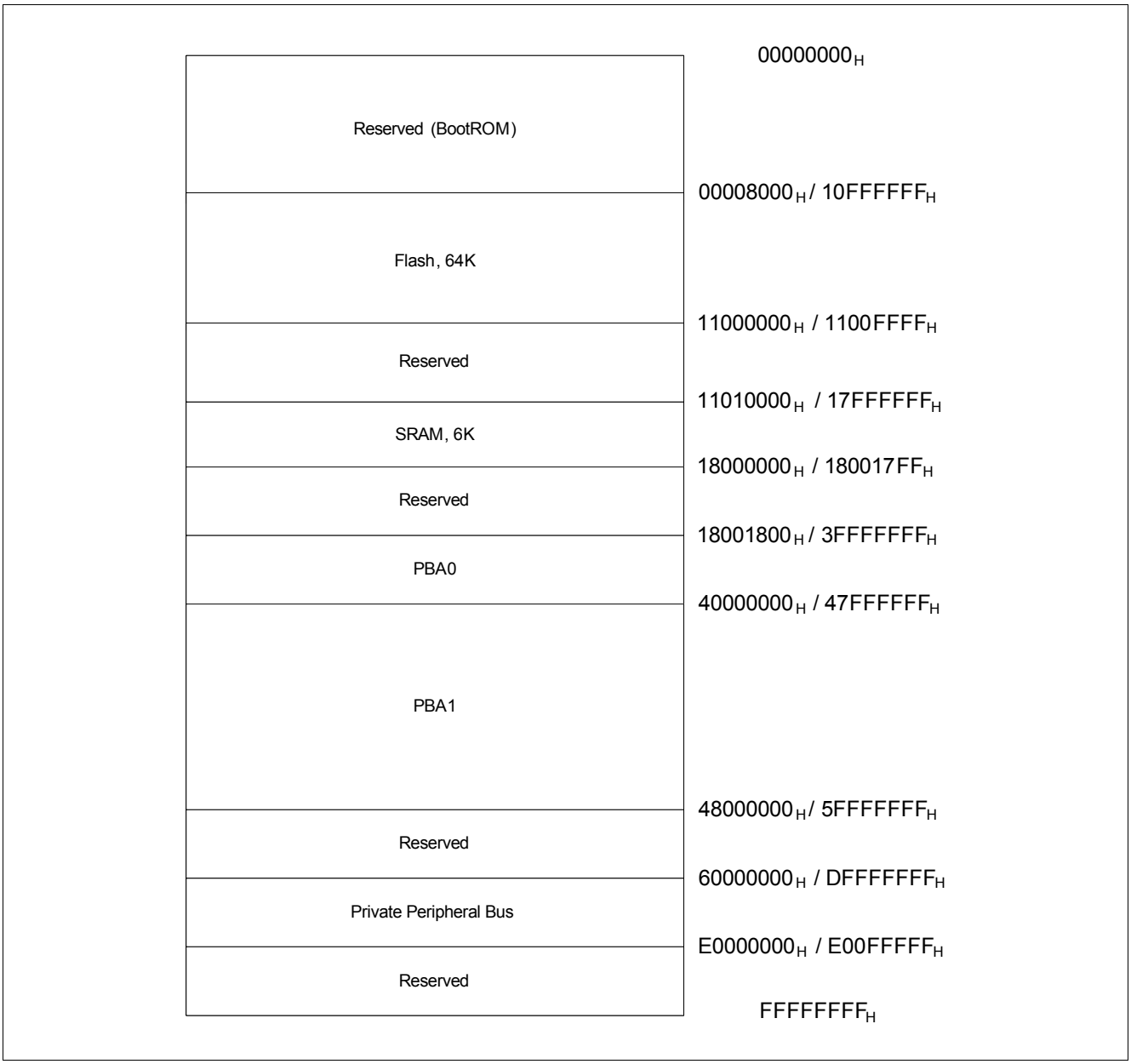


Figure 14 TLE9867QXA20 Memory Map

11.3 NVM Module (Flash Memory)

The Flash Memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data.

Features

- In-system programming via LIN (Flash Mode) and SWD
- Error Correction Code (ECC) for detection of single-bit and double-bit errors and dynamic correction of single Bit errors.
- Interrupts and signals double-bit error by NMI
- Program width of 128 byte (page)
- Minimum erase width of 128 bytes (page)
- Integrated hardware support for EEPROM emulation
- 8 byte read access
- Physical read access time: 75 ns
- Code read access acceleration integrated; read buffer and automatic pre-fetch
- Page program time: 3 ms
- Page erase (128 bytes) and sector erase (4K bytes) time: 4ms

Note: The user has to ensure that no flash operations which change the content of the flash get interrupted at any time.

The clock for the NVM is supplied with the system frequency fsys. Integrated firmware routines are provided to erase NVM, and other operations including EEPROM emulation are provided as well.

Table 7 NMI Interrupt Table

Service Request	Node	Description
Oscillator Watchdog NMI	NMI	Oscillator Watchdog / MI_CLK Watchdog Timer Overflow
NVM Map Error NMI	NMI	NVM Map Error
ECC Error NMI	NMI	RAM / NVM Uncorrectable ECC Error
Supply Prewarning NMI	NMI	Supply Prewarning

13.2 Introduction

The behavior of the Watchdog Timer in Active Mode is illustrated in **Figure 16**.

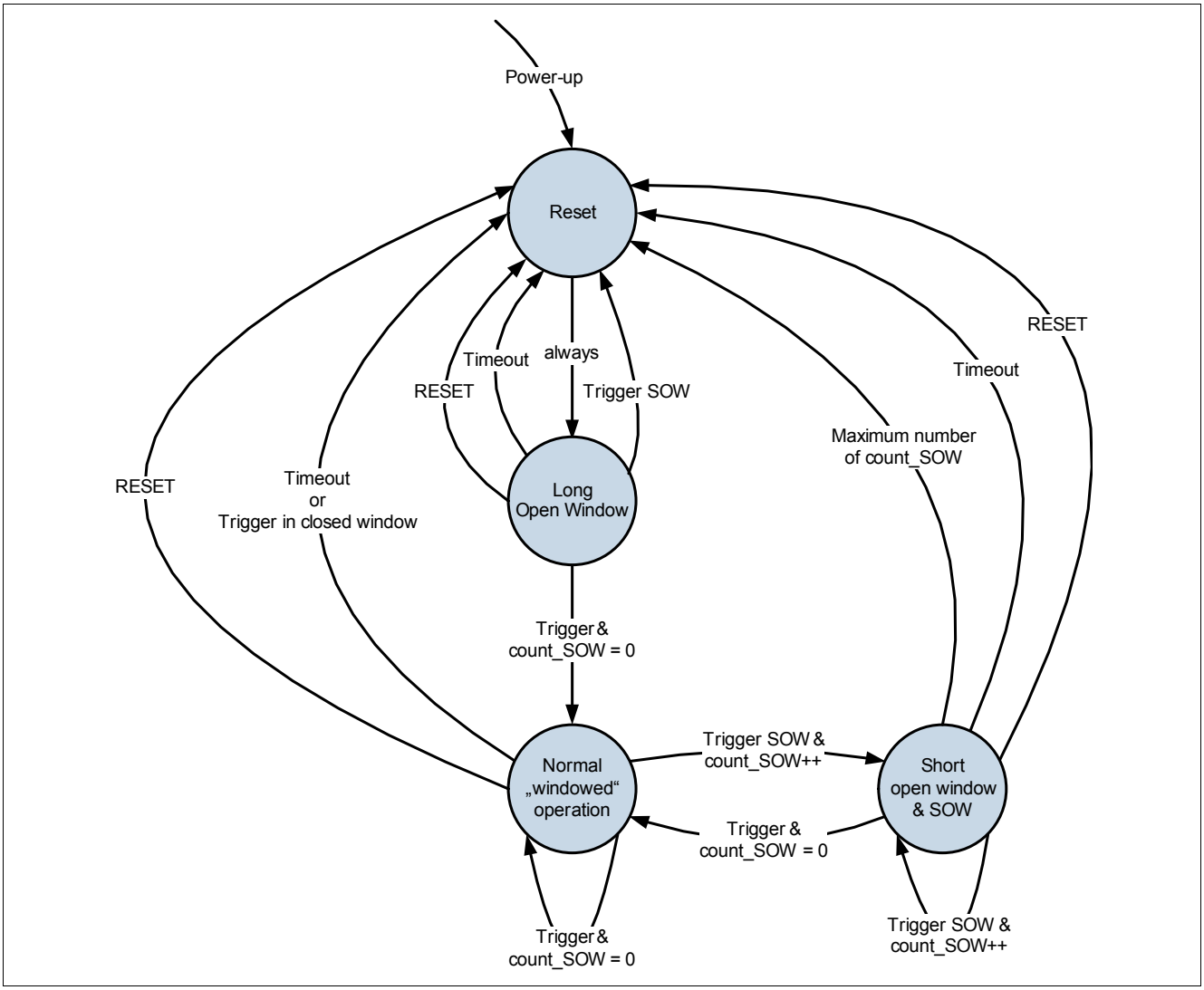


Figure 16 Watchdog Timer Behavior

20.2 Introduction

The LIN Module is a transceiver for the Local Interconnect Network (LIN) compliant to the LIN2.2 standard, backward compatible to LIN1.3, LIN2.0 and LIN2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single wire, bi-directional bus typically used for in-vehicle networks, using baud rates between 2.4 kBaud and 20 kBaud. Additionally baud rates up to 115.2 kBaud are implemented.

The LIN Module offers several different operation modes, including a LIN Sleep Mode and the LIN Normal Mode. The integrated slope control allows to use several data transmission rates with optimized EMC performance. For data transfer at the end of line, a Flash Mode up to 115.2 kBaud is implemented. This Flash Mode can be used for data transfer under special conditions for up to 250 kbit/s (in production environment, point-to-point communication with reduced wire length and limited supply voltage).

20.2.1 Block Diagram

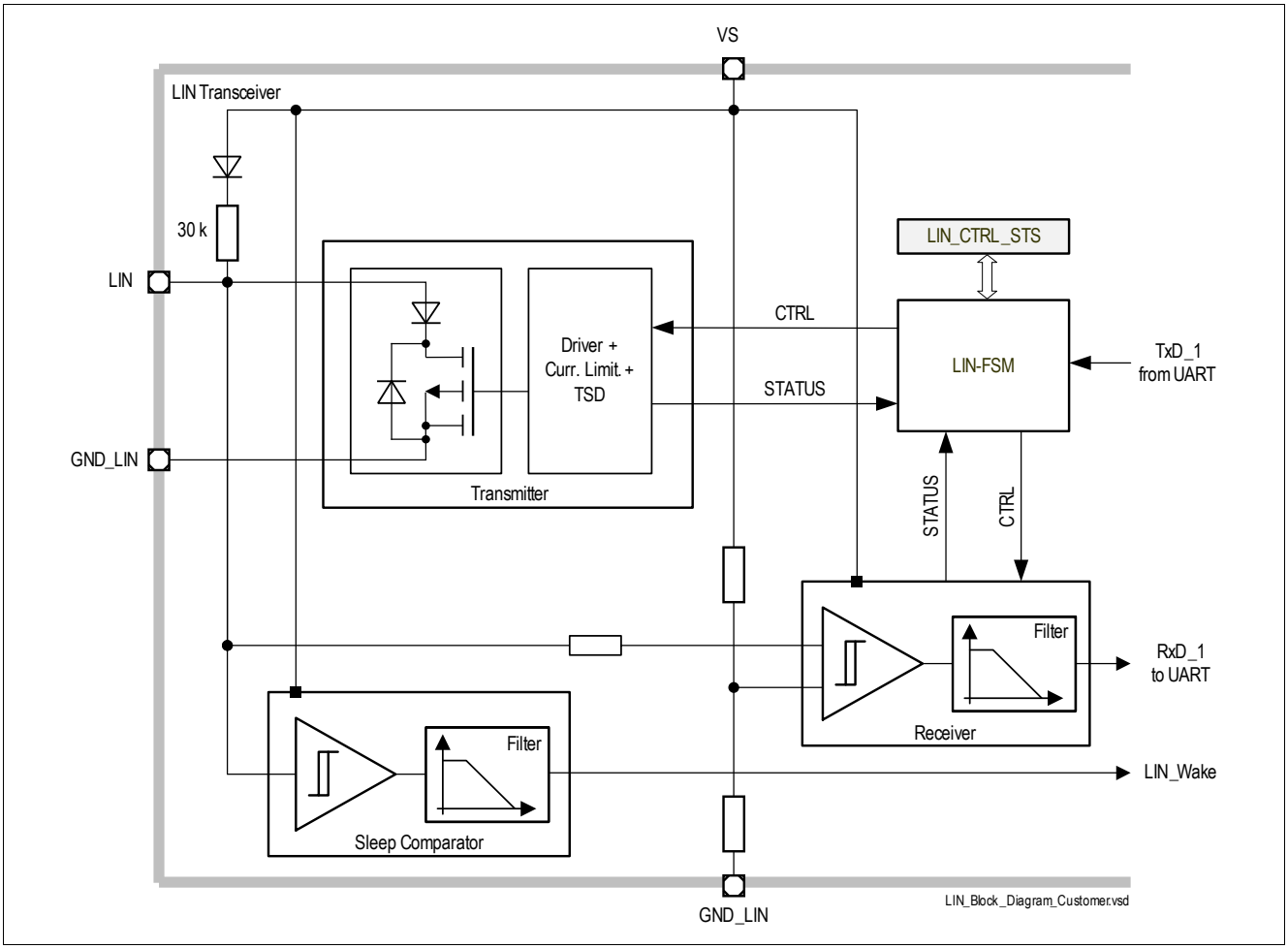


Figure 23 LIN Transceiver Block Diagram

24.2.1 Block Diagram

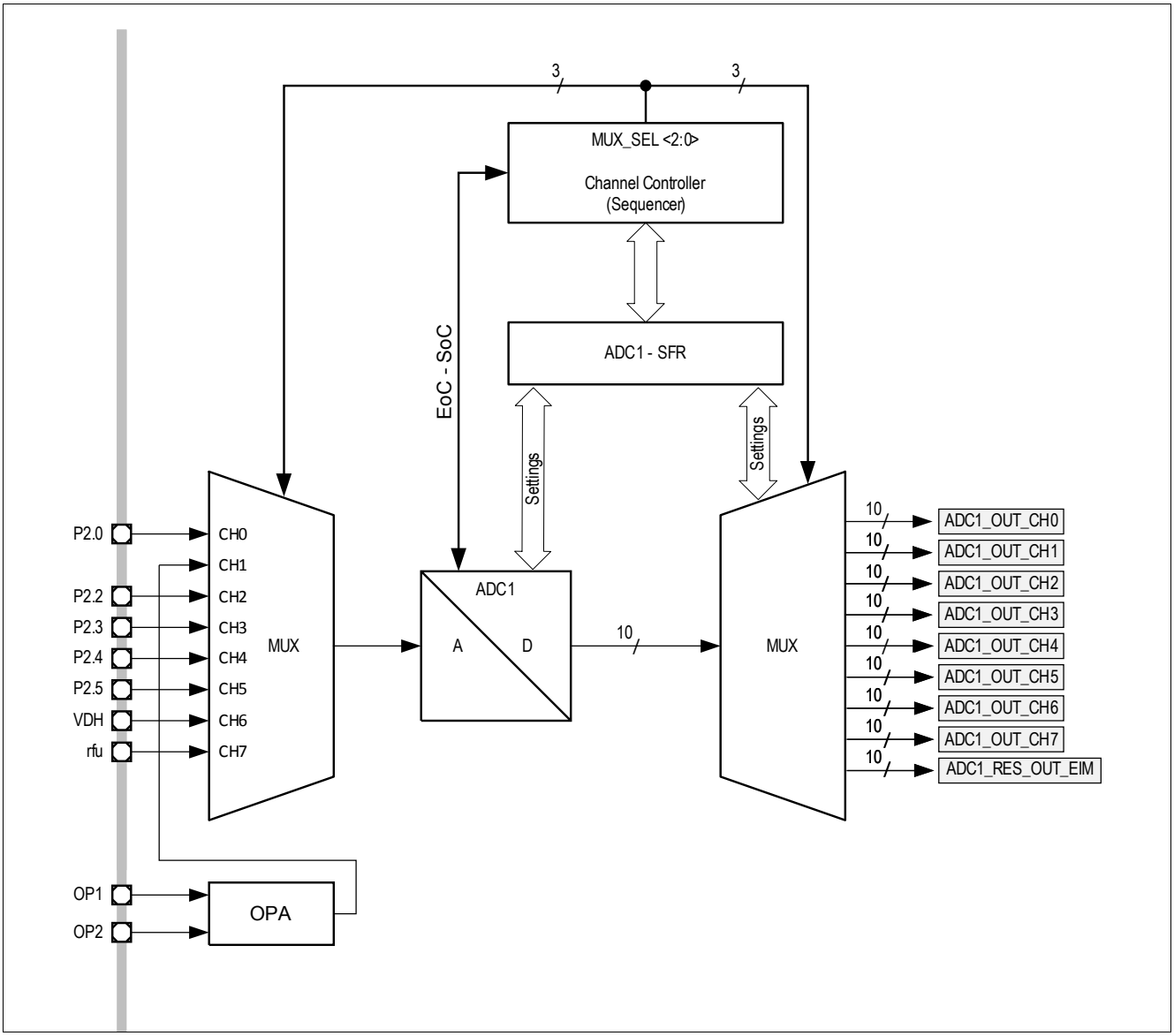


Figure 27 ADC1 Top Level Block Diagram

As shown in the figure above, the ADC1 postprocessing consists of a channel controller (Sequencer) and an 8-channel demultiplexer. The channel control block controls the multiplexer sequencing on the analog side before the ADC1 and on the digital domain after the ADC1. As described in the following section, the channel sequence can be controlled in a flexible way, which allows a certain degree of channel prioritization.

This capability can be used e.g. to give a higher priority to some channels compared to the other channel measurements.

26 Bridge Driver (incl. Charge Pump)

26.1 Features

The MOSFET Driver is intended to drive external normal level NFET transistors in bridge configuration. The driver provides many diagnostic possibilities to detect faults.

Functional Features

- External Power NFET Transistor Driver Stage with driver capability for max. 100 nC gate charge @ 25 kHz switching frequency.
- Implemented adjustable cross conduction protection.
- Supply voltage (VSD) monitoring incl. adjustable over- and undervoltage shutdown with configurable interrupt signalling.
- VSD operating range down to 5.4 V
- VDS comparators for short circuit detection in on- and off-state
- Open-Load detection in off-state

26.2 Introduction

The MOSFET Driver Stage can be used for controlling external Power NFET Transistors (normal level). The module output is controlled by SFR or System PWM Machine (CCU6).

28 Application Information

28.1 H-Bridge Driver

Figure 31 shows the TLE9867QXA20 in an electric drive application setup controlling an H-Bridge motor.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

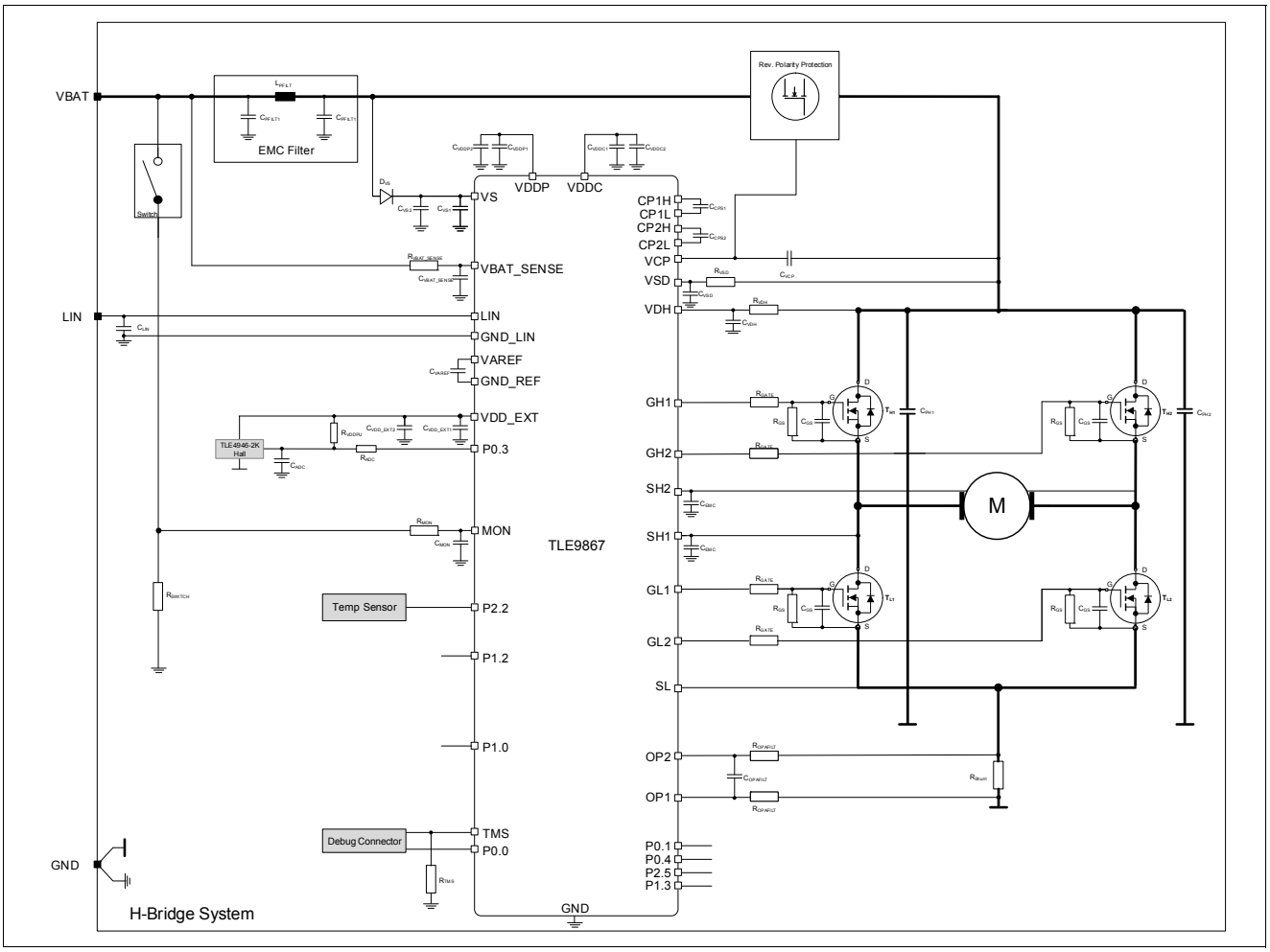


Figure 31 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of materials. The function must be verified in the actual application.

Table 17 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltage range at charge pump pins CP1H, CP1L, CP2H, CP2L, VCP	V_{CPx}	-0.3	–	48	V	8)	P_1.1.15
Voltages – GPIOs							
Voltage on any port pin[9)]	V_{in}	-0.3	–	V_{DDP} +0.3	V	$V_{IN} < V_{DDPmax}$ 10)	P_1.1.16
Current at VCP Pin							
Max. current at VCP pin	I_{VCP}	-15	–	–	mA	–	P_1.1.35
Injection Current at GPIOs							
Injection current on any port pin	I_{GPIONM}	-5	–	5	mA	11)	P_1.1.34
Sum of all injected currents in Normal Mode	I_{GPIOAM_sum}	-50	–	50	mA	11)	P_1.1.30
Sum of all injected currents in Power Down Mode (Stop Mode)	I_{GPIOPD_sum}	-5000	–	50	µA	11)	P_1.1.36
Sum of all injected currents in Sleep Mode	$I_{GPIOSleep\_sum}$	-5	–	5	mA	11)	P_1.1.37
Other Voltages							
Input voltage VAREF	V_{AREF}	-0.3	–	V_{DDP} +0.3	V	–	P_1.1.17
Input voltage OP1, OP2	V_{OAI}	-7	–	7	V	–	P_1.1.23
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_1.1.18
Storage temperature	T_{stg}	-55	–	150	°C	–	P_1.1.19
ESD Susceptibility							
ESD susceptibility all pins	V_{ESD1}	-2	–	2	kV	HBM 12)	P_1.1.20
ESD susceptibility pins MON, VS, VSD, VBAT_SENSE vs.GND	V_{ESD2}	-4	–	4	kV	HBM 13)	P_1.1.21
ESD susceptibility pins LIN vs. GND_LIN	V_{ESD3}	-6	–	6	kV	HBM 12)	P_1.1.22
ESD susceptibility **CDM** all pins vs. GND	V_{ESD_CDM1}	-500	–	500	V	14)	P_1.1.28
ESD susceptibility **CDM** pins 1, 12, 13, 24, 25, 36, 37, 48 (corner pins) vs. GND	V_{ESD_CDM2}	-750	–	750	V	14)	P_1.1.43

1) Not subject to production test, specified by design.

2) Conditions and min. value is derived from application condition for reverse polarity event.

29.1.2 Functional Range

Table 18 Functional Range

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage in Active Mode	V_{S_AM}	5.5	–	28	V	–	P_1.2.1
Extended supply voltage in Active Mode	$V_{S\_AM\_extend}$	28	–	40	V	1) Functional with parameter deviation	P_1.2.16
Supply voltage in Active Mode for MOSFET Driver Supply	V_{SD_AM}	5.4	–	28	V		P_1.2.18
Extended supply voltage in Active Mode for MOSFET Driver Supply	$V_{SD\_AM\_extend}$	28	–	32	V	1)3)Functional with parameter deviation	P_1.2.17
Specified supply voltage for LIN Transceiver	$V_{S\_AM\_LIN}$	5.5	–	18	V	Parameter Specification	P_1.2.2
Extended supply voltage for LIN Transceiver	$V_{S\_AM\_LIN}$	4.8	–	28	V	Functional with parameter deviation	P_1.2.14
Supply voltage in Active Mode with reduced functionality (Microcontroller / Flash with full operation)	V_{S_AMmin}	3.0	–	5.5	V	2)	P_1.2.3
Supply voltage in Sleep Mode	V_{S_Sleep}	3.0	–	28	V	–	P_1.2.4
Supply voltage transients slew rate	dV_S/dt	-1	–	1	V/µs	3)	P_1.2.5
Output sum current for all GPIO pins	$I_{GPIO,sum}$	-50	–	50	mA	3)	P_1.2.7
Operating frequency	f_{sys}	5	–	24	MHz	4)	P_1.2.20
Junction temperature	T_j	-40	–	150	°C	–	P_1.2.9

1) This operation voltage range is only allowed for a short duration: t_{max} ≤ 400 ms (continuous operation at this voltage is not allowed), f_{sys} = 24 MHz, I_{VDDP} = 10 mA, I_{VDDEXT} = 5 mA. In addition, the power dissipation caused by the Charge Pump + MOSFET driver have to be considered.

2) Reduced functionality (e.g. cranking pulse) - Parameter deviation possible.

3) Not subject to production test, specified by design.

4) Function not specified when limits are exceeded.

29.2.4 VPRE Voltage Regulator (PMU Subblock) Parameters

The PMU VPRE Regulator acts as a supply of VDDP and VDDEXT voltage regulators.

Table 25 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VPRE}	–	–	110	mA	1)	P_2.4.1

1) Not subject to production test, specified by design.

29.2.4.1 Load Sharing Scenarios of VPRE Regulator

The figure below shows the possible load sharing scenarios of VPRE regulator.

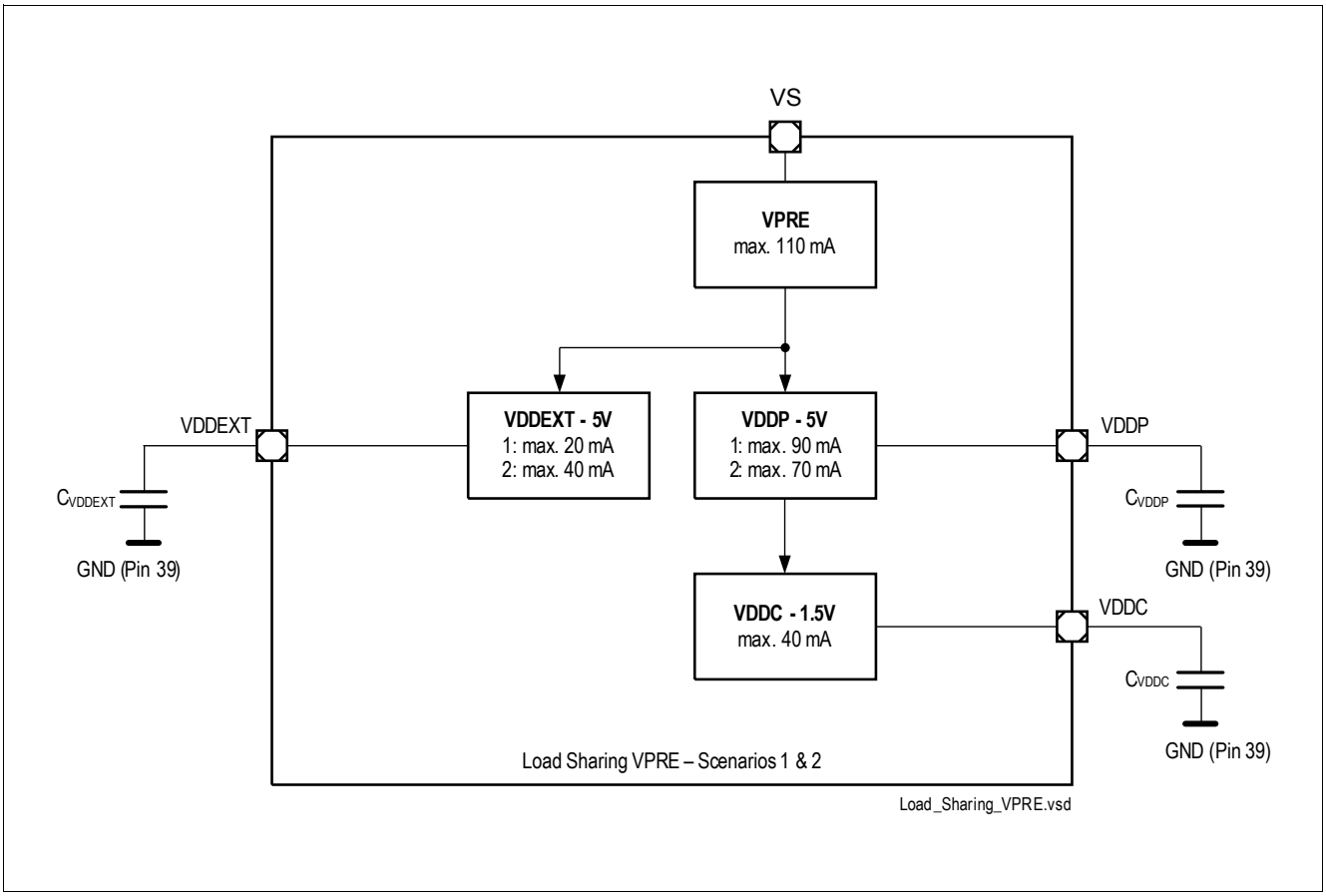


Figure 32 Load Sharing Scenarios of VPRE Regulator

Table 31 DC Characteristics Port0, Port1 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	2)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.3
Input low voltage	V_{IL_extend}	-0.3	0.42 x V_{DDP}	–	V	1)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.17
Input high voltage	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	2)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.4
Input high voltage	V_{IH_extend}	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	1)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.18
Output low voltage	V_{OL}	–	–	1.0	V	3) 4) $I_{OL} \leq I_{OLmax}$	P_5.1.6
Output low voltage	V_{OL}	–	–	0.4	V	3) 5) $I_{OL} \leq I_{OLnom}$	P_5.1.7
Output high voltage	V_{OH}	V_{DDP} - 1.0	–	–	V	3) 4) $I_{OH} \geq I_{OHmax}$	P_5.1.8
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	3) 5) $I_{OH} \geq I_{OHnom}$	P_5.1.9
Input leakage current	$I_{OZ\_extend1}$	-500	–	+500	nA	-40°C ≤ T_J ≤ 25°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.20
Input leakage current	I_{OZ1}	-5	–	+5	µA	6) 25°C < T_J ≤ 85°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.10
Input leakage current	$I_{OZ\_extend2}$	-15	–	+15	µA	85°C < T_J ≤ 150°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.11
Pull level keep current	I_{PLK}	-200	–	+200	µA	7) $V_{PIN} \geq V_{IH}$ (up) $V_{PIN} \leq V_{IL}$ (dn)	P_5.1.12
Pull level force current	I_{PLF}	-1.5	–	+1.5	mA	7) $V_{PIN} \leq V_{IL}$ (up) $V_{PIN} \geq V_{IH}$ (dn)	P_5.1.13
Pin capacitance	C_{IO}	–	–	10	pF	1)	P_5.1.14
Reset Pin Timing							
Reset Pin Input Filter Time	t_{filt_RESET}	–	5	–	µs	1)	P_5.1.19

1) Not subject to production test, specified by design.

2) Tested at V_{DDP} = 5V, specified for 4.5V < V_{DDP} < 5.5V.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

4) Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 4mA, I_{OH} = -4mA, specified for 4.5V < V_{DDP} < 5.5V.

5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow GND$, $V_{OH} \rightarrow V_{DDP}$). Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 1mA, I_{OH} = -1mA.

6) The given values are worst-case values. In production tests, this leakage current is only tested at 150°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
I_{OZ} = 0.05 × $e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
I_{OZ} = $I_{OZtempmax}$ - (1.6 × DV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.

7) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pull-up; $V_{PIN} \leq V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pull-up; $V_{PIN} \geq V_{IH}$ for a pull-down.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

29.5.3 DC Parameters of Port 2

These parameters apply to the IO voltage range, 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 32 DC Characteristics Port 2

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	1)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.2.1
Input low voltage	V_{IL_extend}	-0.3	0.42 x V_{DDP}	–	V	2)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.2.10
Input high voltage	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	1)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.2.2
Input high voltage	V_{IH_extend}	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	2)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.2.11
Input hysteresis	HYS_{P2}	0.11 x V_{DDP}	–	–	V	2)Series resistance = 0 Ω; 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.2.3
Input hysteresis	HYS_{P2_extend}	–	0.09 x V_{DDP}	–	V	2)Series resistance = 0 Ω; 2.6V ≤ VDDP < 4.5V	P_5.2.12
Input leakage current	I_{OZ2}	-400	–	+400	nA	T_J ≤ 85°C, 0 V < V_{IN} < V_{DDP}	P_5.2.4
Pull level keep current	I_{PLK}	-30	–	+30	µA	3) $V_{PIN} \geq V_{IH}$ (up) $V_{PIN} \leq V_{IL}$ (dn)	P_5.2.5

Table 33 Electrical Characteristics LIN Transceiver (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Bus short circuit current	$I_{BUS,sc}$	40	100	150	mA	Current Limitation for driver dominant state driver on V_{BUS} = 18 V; LIN Spec 2.2 (Par. 12)	P_6.1.10
Bus short circuit filter time	$t_{BUS,sc}$	–	5	–	µs	[6]The overall bus short circuit filter time is a sum of tBUS,sc + digital filter time. The digital filter time is 4 µs (typ.)	P_6.1.71
Leakage current (loss of ground)	$I_{BUS\_NO\_GND}$	-1000	-450	1000	µA	V_S = 12 V; 0 < V_{BUS} < 18 V; LIN Spec 2.2 (Par. 15)	P_6.1.11
Leakage current	$I_{BUS\_NO\_BAT}$	–	10	20	µA	V_S = 0 V; V_{BUS} = 18 V; LIN Spec 2.2 (Par. 16)	P_6.1.12
Leakage current	$I_{BUS\_PAS\_dom}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN Spec 2.2 (Par. 13)	P_6.1.13
Leakage current	$I_{BUS\_PAS\_rec}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; LIN Spec 2.2 (Par. 14)	P_6.1.14
Bus pull-up resistance	R_{BUS}	20	30	47	kΩ	Normal mode LIN Spec 2.2 (Par. 26)	P_6.1.15
AC Characteristics - Transceiver Normal Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.16
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.17
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$; LIN Spec 2.2 (Par. 32)	P_6.1.18
Duty cycle D1 Normal Slope Mode (for worst case at 20 kbit/s)	t_{duty1}	0.396	–	–		[4] duty cycle 1 TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 5.5 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN Spec 2.2 (Par. 27)	P_6.1.19

29.8 Measurement Unit

29.8.1 System Voltage Measurement Parameters

Table 35 Supply Voltage Signal Conditioning

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Measurement output voltage range @ VAREF5	V_{A5}	0	–	5	V	–	P_8.1.15
Measurement output voltage range @ VAREF1V2	V_{A1V2}	0	–	1.23	V	–	P_8.1.16
Battery / Supply Voltage Measurement V_{BAT_SENSE} / V_S							
Input to output voltage attenuation: V_S	ATT_{VS_1}	–	0.055	–		SFR setting 1	P_8.1.41
Input to output voltage attenuation: V_{BAT_SENSE}	$ATT_{VBAT\_SENSE\_1}$	–	0.055	–		SFR setting 1	P_8.1.60
Nominal operating input voltage range V_{BAT_SENSE} and V_S	$V_{BAT\_SENSE,range1}$, $V_{S,range1}$	3	–	22	V	[1] SFR setting 1; Max. value corresponds to typ. ADC full scale input; 3V < V_{BAT_SENSE}/ V_S < 28V	P_8.1.1
Accuracy of V_{BAT_SENSE}/ V_S after calibration	$\Delta V_{BAT\_SENSE,range1}$, $V_{S,range1}$	-220	–	220	mV	SFR setting 1, V_S = 5.5 V to 18V	P_8.1.70
Input to output voltage attenuation: V_S	ATT_{VS_2}	–	0.039	–		SFR setting 2	P_8.1.42
Input to output voltage attenuation: V_{BAT_SENSE}	$ATT_{VBAT\_SENSE\_2}$	–	0.039	–		SFR setting 2	P_8.1.61
Nominal operating input voltage range V_{BAT_SENSE} and V_S	$V_{BAT\_SENSE,range2}$, $V_{S,range2}$	3	–	31	V	[1] SFR setting 2; Max. value corresponds to typ. ADC full scale input 3V < V_{BAT_SENSE}/ V_S < 28V	P_8.1.40
Accuracy of V_{BAT_SENSE} / V_S after calibration	$\Delta V_{BAT\_SENSE,range2}$, $V_{S,range2}$	-370	–	370	mV	SFR setting 2, V_S = 5.5V to 18V	P_8.1.44

29.9.2 Electrical Characteristics ADC1 (10-Bit)

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 40 A/D Converter Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Analog reference supply	V_{AREF}	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	1)	P_9.2.1
Analog reference ground	V_{AGND}	V_{SS} - 0.05	–	1.5	V	–	P_9.2.2
Analog input voltage range	V_{AIN}	V_{AGND}	–	V_{AREF}	V	2)	P_9.2.3
Analog clock frequency	f_{ADCI}	5	–	24	MHz	3)	P_9.2.4
Conversion time for 10-bit result	t_{C10}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	–	1)4)	P_9.2.5
Conversion time for 8-bit result	t_{C8}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	–	1)	P_9.2.6
Wakeup time from analog powerdown, fast mode	t_{WAF}	–	–	4	µs	1)	P_9.2.7
Wakeup time from analog powerdown, slow mode	t_{WAS}	–	–	15	µs	1)5)	P_9.2.8
Total unadjusted error (8 bit)	TUE_{8B}	-2	±1	+2	counts	6)7)Reference is internal V_{AREF}	P_9.2.9
Total unadjusted error (10 bit)	TUE_{10B}	-12	±6	+12	counts	7)8)Reference is internal V_{AREF}	P_9.2.22
DNL error	EA_{DNL}	-3	±0.8	+3	counts	–	P_9.2.10
INL error	$EA_{INL\_int\_VAREF}$	-5	±0.8	+5	counts	Reference is internal V_{AREF}	P_9.2.11
Gain error	$EA_{GAIN\_int\_VAREF}$	-10	±0.4	+10	counts	Reference is internal V_{AREF}	P_9.2.12
Offset error	EA_{OFF}	-2	±0.5	+2	counts	–	P_9.2.13
Total capacitance of an analog input	C_{AINT}	–	–	10	pF	1)5)9)	P_9.2.14
Switched capacitance of an analog input	C_{AINS}	–	–	4	pF	1)5)9)	P_9.2.15
Resistance of the analog input path	R_{AIN}	–	–	2	kΩ	1)5)9)	P_9.2.16

30 Package Outlines

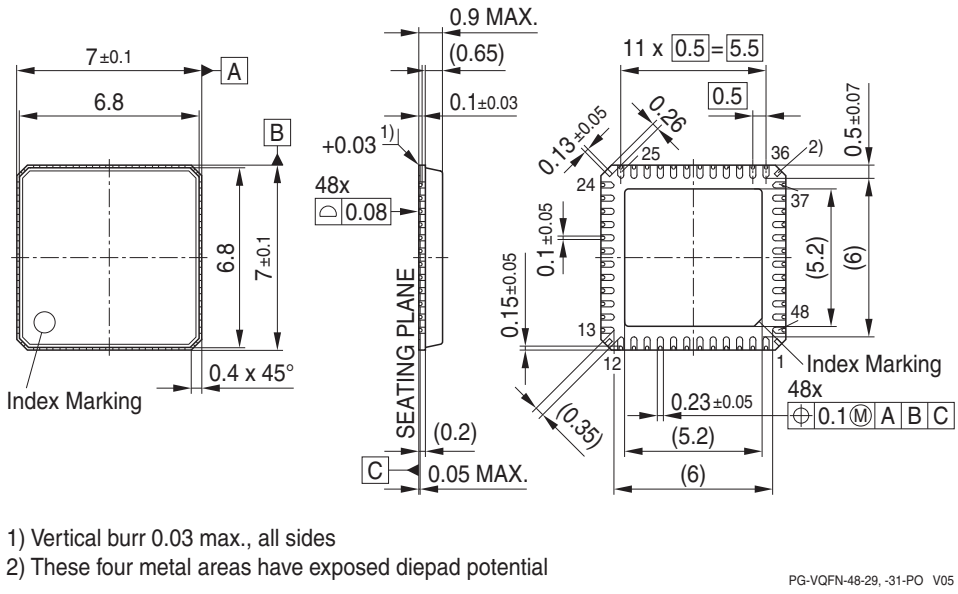


Figure 37 Package outline VQFN-48-31 (with LTI)

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.*
2. *Dimensions in mm.*