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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk22dx128vlk5

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK22 and MK22.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	 M = Fully qualified, general market flow P = Prequalification
K##	Kinetis family	• K22
A	Key attribute	 D = Cortex-M4 w/ DSP F = Cortex-M4 w/ DSP and FPU
Μ	Flash memory type	 N = Program flash only X = Program flash and FlexMemory

Table continues on the next page...



reminology and guidelines

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/ pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- Operating ratings apply during operation of the chip.
- Handling ratings apply when the chip is not powered.



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Тур.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μΑ

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



Symbol	Description	Min.	Max.	Unit	Notes
I _{ICcont}	 Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins Negative current injection Positive current injection 	-25 —	 +25	mA	
V _{RAM}	V _{DD} voltage required to retain RAM	1.2	_	V	
V _{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V _{POR_VBAT}	—	V	

Table 1. Voltage and current operating requirements (continued)

1. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX} , a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{ICAIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{ICAIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.

5.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V _{LVW1H}	Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V _{LVW2H}	Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V _{LVW3H}	Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V _{LVW4H}	Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	_	mV	
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V _{LVW1L}	Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V _{LVW2L}	Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V _{LVW3L}	Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V _{LVW4L}	Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60		mV	
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	



General

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.			μs	1
	 1.71 V/(V_{DD} slew rate) ≤ 300 μs 	—	300		
	 1.71 V/(V_{DD} slew rate) > 300 µs 	—	1.7 V / (V _{DD} slew rate)		
	VLLS0 → RUN	—	135	μs	
	• VLLS1 → RUN		135	μs	
	• VLLS2 \rightarrow RUN	—	85	μs	
	 VLLS3 → RUN 	_	85	μs	
	• LLS → RUN	_	6	μs	
	 VLPS → RUN 		5.2	μs	
	• STOP \rightarrow RUN	_	5.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8 V	_	12.98	14	mA	
	• @ 3.0 V	_	12.93	13.8	mA	

Table continues on the next page...

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General



Figure 3. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors Table 7. EMC radiated emissions operating behaviors 1

Symbol	Description	Frequency band (MHz)	Тур.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	19	dBµV	2, 3
V _{RE2}	Radiated emissions voltage, band 2	50–150	21	dBµV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	19	dBµV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	11	dBµV	
V _{RE_IEC}	IEC level	0.15–1000	L	_	3, 4

1. This data was collected on a MK20DN128VLH5 64pin LQFP device.

2. Determined according to IEC Standard 61967-1, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions and IEC Standard 61967-2, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions – TEM Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

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- 3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
- 4. 75 pF load
- 5. 15 pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
TJ	Die junction temperature	-40	125	°C
T _A	Ambient temperature	-40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	80 LQFP	Unit	Notes
Single-layer (1s)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	50	°C/W	1,2
Four-layer (2s2p)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	35	°C/W	1,3
Single-layer (1s)	R _{θJMA}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	39	°C/W	1,3
Four-layer (2s2p)	R _{θJMA}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	29	°C/W	1,3
	R _{0JB}	Thermal resistance, junction to board	19	°C/W	4
_	R _{θJC}	Thermal resistance, junction to case	8	°C/W	5

Table continues on the next page ...



Symbol	Description	Min.	Max.	Unit
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	_	ns
J7	TCLK low to boundary scan output data valid		25	ns
J8	TCLK low to boundary scan output high-Z		25	ns
J9	TMS, TDI input data setup time to TCLK rise	8		ns
J10	TMS, TDI input data hold time after TCLK rise	1	_	ns
J11	TCLK low to TDO data valid		17	ns
J12	TCLK low to TDO high-Z		17	ns
J13	TRST assert time	100		ns
J14	TRST setup time (negation) to TCLK high	8		ns

Table 12. JTAG limited voltage range electricals (continued)

Table 13. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	20	
	Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	Boundary Scan	50	—	ns
	JTAG and CJTAG	25	_	ns
	Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8		ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	_	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z		22.1	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	_	0.6		V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V _{DD}		V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	_	0.6		V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	_	V _{DD}		V	

Table 15. Oscillator DC electrical specifications (continued)

- 1. V_{DD} =3.3 V, Temperature =25 °C
- 2. See crystal or resonator manufacturer's recommendation
- 3. C_x and C_y can be provided by using either integrated capacitors or external components.
- 4. When low-power mode is selected, R_F is integrated and must not be attached externally.
- 5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

6.3.2.2 Oscillator frequency specifications Table 16. Oscillator frequency speci

able 16.	Oscillator	frequency	specifications
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Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal or resonator frequency — low- frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f _{osc_hi_1}	Oscillator crystal or resonator frequency — high- frequency mode (low range) (MCG_C2[RANGE]=01)	3	_	8	MHz	
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8		32	MHz	
f _{ec_extal}	Input clock frequency (external clock mode)			50	MHz	1, 2
t _{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t _{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	_	750	_	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	_	0.6	_	ms	•
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)		1	_	ms	

- 1. Other frequency limits may apply when external clock is being used as a reference for FLL or PLL.
- 2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that—it remains within the limits of DCO input clock frequency when divided by FRDIV.
- 3. Proper PC board layout procedures must be followed to achieve specifications.

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4. Crystal startup time is defined as the time between oscillator being enabled and OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz oscillator electrical characteristics

6.3.3.1 32 kHz oscillator DC electrical specifications Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{BAT}	Supply voltage	1.71	—	3.6	V
R _F	Internal feedback resistor		100	_	MΩ
C _{para}	Parasitical capacitance of EXTAL32 and XTAL32		5	7	pF
V _{pp} ¹	Peak-to-peak amplitude of oscillation	_	0.6	_	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32 kHz oscillator frequency specifications Table 18. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t _{start}	Crystal start-up time	—	1000	—	ms	1
V _{ec_extal32}	Externally provided input clock amplitude	700	—	V _{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.

This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The
oscillator remains enabled and XTAL32 must be left unconnected.

3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	Swap Control execution time					
t _{swapx01}	control code 0x01	_	200	—	μs	
t _{swapx02}	control code 0x02	_	70	150	μs	
t _{swapx04}	control code 0x04	_	70	150	μs	
t _{swapx08}	control code 0x08		—	30	μs	
	Program Partition for EEPROM execution time					
t _{pgmpart64k}	• 64 KB FlexNVM	_	138	—	ms	
	Set FlexRAM Function execution time:					
t _{setramff}	Control Code 0xFF	—	70	—	μs	
t _{setram32k}	32 KB EEPROM backup	_	0.8	1.2	ms	
t _{setram64k}	64 KB EEPROM backup		1.3	1.9	ms	
	Byte-write to FlexRAM	for EEPROM	loperation		1	
t _{eewr8bers}	Byte-write to erased FlexRAM location execution time	_	175	260	μs	3
	Byte-write to FlexRAM execution time:					
t _{eewr8b32k}	32 KB EEPROM backup	_	385	1800	μs	
t _{eewr8b64k}	64 KB EEPROM backup		475	2000	μs	
	Word-write to FlexRAM	for EEPRON	A operation		1	
t _{eewr16bers}	Word-write to erased FlexRAM location execution time	_	175	260	μs	
	Word-write to FlexRAM execution time:					
t _{eewr16b32k}	32 KB EEPROM backup	_	385	1800	μs	
t _{eewr16b64k}	64 KB EEPROM backup		475	2000	μs	
Longword-write to FlexRAM for EEPROM operation						1
t _{eewr32bers}	Longword-write to erased FlexRAM location execution time	_	360	540	μs	
	Longword-write to FlexRAM execution time:					
t _{eewr32b32k}	32 KB EEPROM backup	_	630	2050	μs	
t _{eewr32b64k}	64 KB EEPROM backup	_	810	2250	μs	

Table 20. Flash command timing specifications (continued)

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.



- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.



Figure 9. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics Table 25. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions ¹ .	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
	ADC	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/$
	asynchronous clock source	• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	f _{ADACK}
TADACK		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter	for sample t	imes			
TUE	Total unadjusted	12-bit modes	—	±4	±6.8	LSB ⁴	5
	error	 <12-bit modes 	—	±1.4	±2.1		
DNL	Differential non-	12-bit modes	_	±0.7	-1.1 to +1.9	LSB ⁴	5
	linearity				-0.3 to 0.5		
		 <12-bit modes 	—	±0.2			

Table continues on the next page...



Symbol	Description	Conditions ¹ .	Min.	Typ. ²	Max.	Unit	Notes
INL	Integral non-	12-bit modes	—	±1.0	-2.7 to +1.9	LSB ⁴	5
	linearity				-0.7 to +0.5		
		 <12-bit modes 	—	±0.5			
E _{FS}	Full-scale error	12-bit modes	—	-4	-5.4	LSB ⁴	V _{ADIN} =
		 <12-bit modes 	_	-1.4	-1.8		V _{DDA}
EQ	Quantization	16-bit modes	—	-1 to 0	—	LSB ⁴	
	error	• ≤13-bit modes	_		±0.5		
ENOB	Effective number	16-bit differential mode					6
	of bits	• Avg = 32	12.8	14.5	_	bits	
		• Avg = 4	11.9	13.8	—	bits	
		16-bit single-ended mode					
		• Avg = 32	12.2	13.9	_	bits	
		• Avg = 4	11.4	13.1	_	bits	
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic	16-bit differential mode					7
	distortion	• Avg = 32	_	-94	_	dB	
		16-bit single-ended mode	_	-85	_	dB	
		• Avg = 32					
SFDR	Spurious free	16-bit differential mode					7
	dynamic range	• Avg = 32	82	95	—	dB	
		16-bit single-ended mode	79	90		dB	
		• Avg = 32		30		ЧD	
E _{IL}	Input leakage error			$I_{In} \times R_{AS}$		mV	I _{In} = leakage current
							(refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V _{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

Table 25. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$



- Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^N$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- 8. ADC conversion clock < 3 MHz



Typical ADC 16-bit Differential ENOB vs ADC Clock 100Hz, 90% FS Sine Input

Figure 10. Typical ENOB vs. ADC_CLK for 16-bit differential mode

6.6.3.2 12-bit DAC operating behaviors Table 28. 12-bit DAC operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA_DACL}	Supply current — low-power mode	_	—	330	μΑ	
I _{DDA_DACH} P	Supply current — high-speed mode	_	—	1200	μΑ	
tDACLP	Full-scale settling time (0x080 to 0xF7F) — low-power mode	_	100	200	μs	1
t _{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
t _{CCDACLP}	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	_	0.7	1	μs	1
V _{dacoutl}	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	_	_	100	mV	
V _{dacouth}	DAC output voltage range high — high- speed mode, no load, DAC set to 0xFFF	V _{DACR} -100	—	V _{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V _{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V _{DACR} = VREF_OUT	_	—	±1	LSB	4
V _{OFFSET}	Offset error	_	±0.4	±0.8	%FSR	5
E _G	Gain error	_	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \ge 2.4 \text{ V}$	60	—	90	dB	
T _{CO}	Temperature coefficient offset voltage	_	3.7	_	μV/C	6
T _{GE}	Temperature coefficient gain error	_	0.000421	_	%FSR/C	
Rop	Output resistance (load = $3 \text{ k}\Omega$)	_	—	250	Ω	
SR	Slew rate -80h \rightarrow F7Fh \rightarrow 80h				V/µs	
	 High power (SP_{HP}) 	1.2	1.7	—		
	Low power (SP _{LP})	0.05	0.12	_		
СТ	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth				kHz	
	 High power (SP_{HP}) 	550	_	—		
	Low power (SP _{LP})	40	-	—		

1. Settling within ±1 LSB

- 2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV
- 3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV
- 4. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V
- 5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} 100 mV
- V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device





Figure 15. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 29.	VREF full-range	operating	requirements
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Symbol	Description	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
T _A	Temperature	Operating temperature range of the device		°C	
CL	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.

 The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.



6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

6.8.2 USB DCD electrical specifications

Table 33.	USB DCD	electrical	specifications
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Symbol	Description	Min.	Тур.	Max.	Unit
V _{DP_SRC}	USB_DP source voltage (up to 250 µA)	0.5	—	0.7	V
V _{LGC}	Threshold voltage for logic high	0.8	_	2.0	V
I _{DP_SRC}	USB_DP source current	7	10	13	μA
I _{DM_SINK}	USB_DM sink current	50	100	150	μA
R _{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	_	24.8	kΩ
V _{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

6.8.3 VREG electrical specifications

Table 34. VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	μA	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μA	
I _{DDoff}	Quiescent current — Shutdown mode					
	 VREGIN = 5.0 V and temperature=25 °C 	—	650	—	nA	
	Across operating voltage and temperature	—	_	4	μA	
I _{LOADstby}	Maximum load current — Standby mode	_	_	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) > 3.6 V					
	Run mode	3	3.3	3.6	v	
	Standby mode	2.1	2.8	3.6	v	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1		3.6	V	2
C _{OUT}	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I _{LIM}	Short circuit current		315		mA	



Num.	Characteristic	Min.	Max.	Unit
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

Table 39. I2S/SAI master mode timing (continued)



Figure 20. I2S/SAI timing — master modes

Table 40. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	_	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	_	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	_	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	_	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear





Figure 22. I2S/SAI timing — master modes

Table 42. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	_	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear





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