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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	34MHz
Connectivity	Ethernet, I²C, LPC, PECI, SCI, SSU
Peripherals	DMA, POR, PWM, WDT
Number of I/O	106
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f2462vfq34v

Section 8 I/O Ports

Section 9 14-Bit PWM Timer (PWMX)

Section 10 16-Bit Free-Running Timer (FRT)

Section 25 Flash Memory

Section 26 Boundary Scan (JTAG)

Section 2 CPU

The H8S/2600 CPU is a high-speed central processing unit with an internal 32-bit architecture that is upward-compatible with the H8/300 and H8/300H CPUs. The H8S/2600 CPU has sixteen 16-bit general registers, can address a 16-Mbyte linear address space, and is ideal for realtime control. This section describes the H8S/2600 CPU. The usable modes and address spaces differ depending on the product. For details on each product, refer to section 3, MCU Operating Modes.

2.1 Features

- Upward-compatible with H8/300 and H8/300H CPUs
  - Can execute H8/300 and H8/300H CPUs object programs
- General-register architecture
  - Sixteen 16-bit general registers also usable as sixteen 8-bit registers or eight 32-bit registers
- Sixty-nine basic instructions
  - 8/16/32-bit arithmetic and logic instructions
  - Multiply and divide instructions
  - Powerful bit-manipulation instructions
  - Multiply-and-accumulate instruction
- Eight addressing modes
  - Register direct [Rn]
  - Register indirect [@ERn]
  - Register indirect with displacement [@(d:16,ERn) or @(d:32,ERn)]
  - Register indirect with post-increment or pre-decrement [@ERn+ or @–ERn]
  - Absolute address [@aa:8, @aa:16, @aa:24, or @aa:32]
  - Immediate [#xx:8, #xx:16, or #xx:32]
  - Program-counter relative [@(d:8,PC) or @(d:16,PC)]
  - Memory indirect [@@aa:8]
- 16-Mbyte address space
  - Program: 16 Mbytes
  - Data: 16 Mbytes
- High-speed operation
  - All frequently-used instructions execute in one or two states
  - 8/16/32-bit register-register add/subtract: 1 state
  - 8 × 8-bit register-register multiply: 2 states

2.5 Data Formats

The H8S/2600 CPU can process 1-bit, 4-bit (BCD), 8-bit (byte), 16-bit (word), and 32-bit (longword) data. Bit-manipulation instructions operate on 1-bit data by accessing bit n (n = 0, 1, 2, …, 7) of byte operand data. The DAA and DAS decimal-adjust instructions treat byte data as two digits of 4-bit BCD data.

2.5.1 General Register Data Formats

Figure 2.9 shows the data formats in general registers.

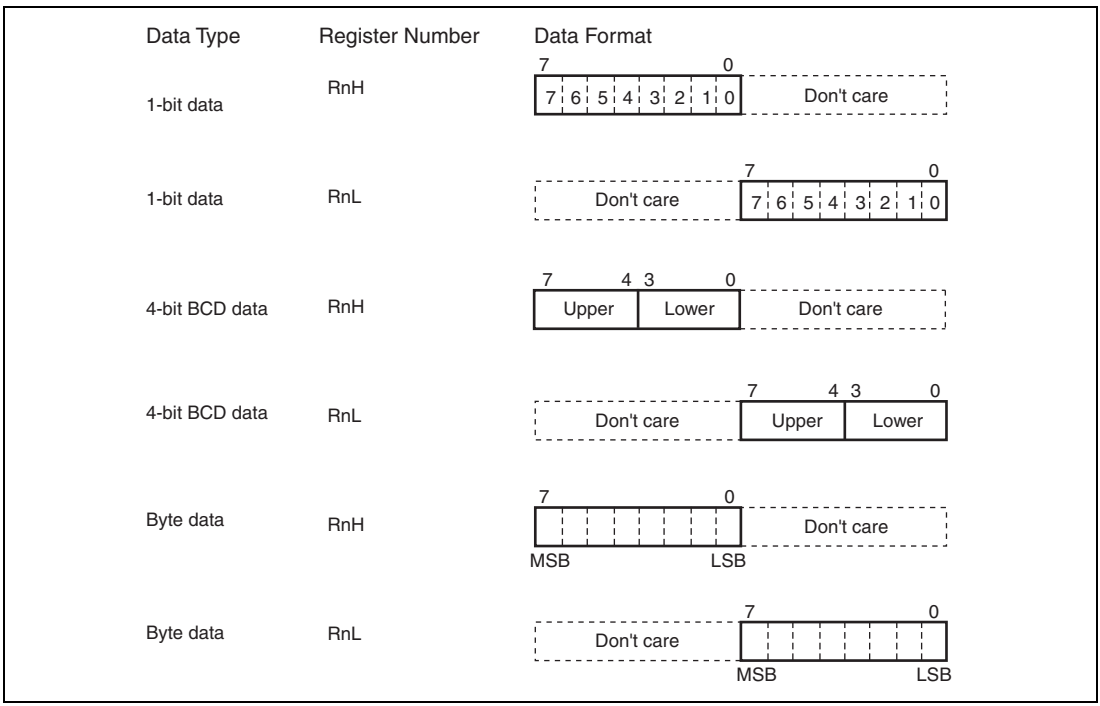

Figure 2.9 General Register Data Formats (1)

7.4 Activation Sources

The DTC is activated by an interrupt request or by a write to DTVECR by software. The interrupt request source to activate the DTC is selected by DTCER. At the end of a data transfer (or the last consecutive transfer in the case of chain transfer), the interrupt flag that became the activation source or the corresponding DTCER bit is cleared. The activation source flag, in the case of RXI0, for example, is the RDRF flag in SCI_0.

When an interrupt has been designated as a DTC activation source, the existing CPU mask level and interrupt controller priorities have no effect. If there is more than one activation source at the same time, the DTC operates in accordance with the default priorities. Figure 7.2 shows a block diagram of DTC activation source control. For details on the interrupt controller, see section 5, Interrupt Controller.

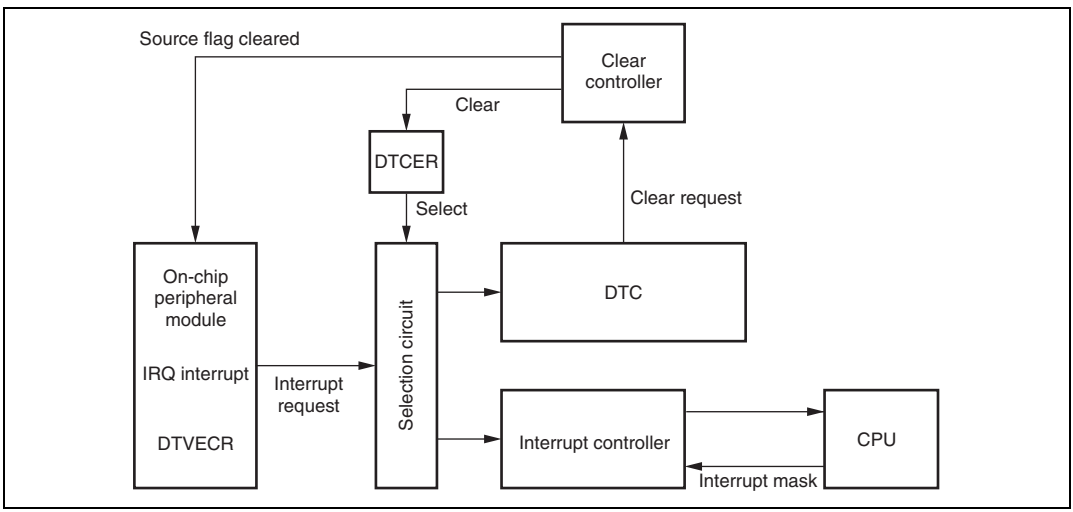

Figure 7.2 Block Diagram of DTC Activation Source Control

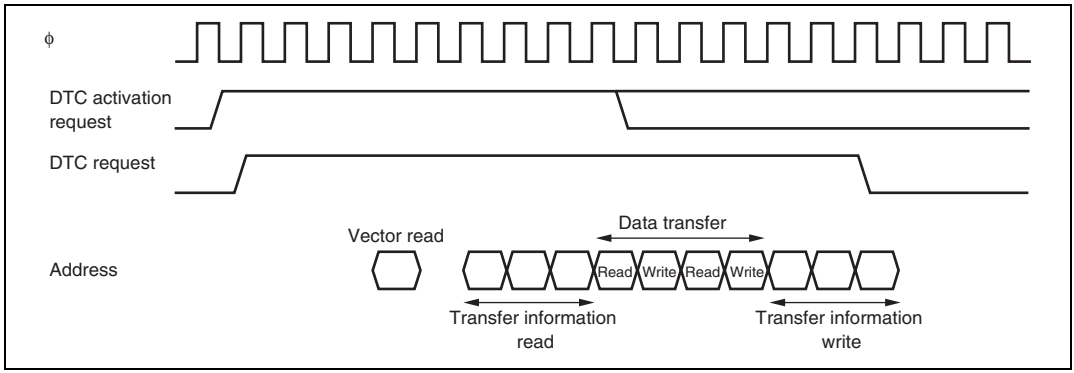

Figure 7.10 DTC Operation Timing (Example of Block Transfer Mode, with Block Size of 2)

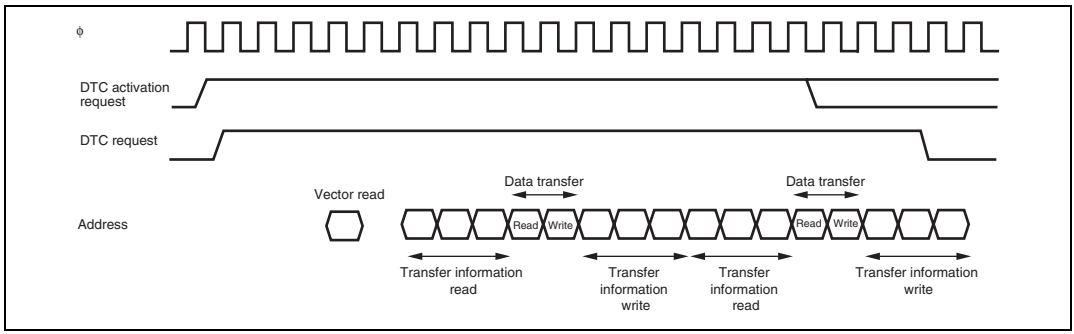

Figure 7.11 DTC Operation Timing (Example of Chain Transfer)

(5) Input Pull-Up MOS

Port A has built-in input pull-up MOSs that can be controlled by software. This input pull-up MOS can be used in any operating mode, and can be specified as on or off on a bit-by-bit basis.

PAnDDR	0		1
PAnODR	1	0	X
PAn pull-up MOS	ON	OFF	OFF

[Legend] n = 7 to 0, X: Don't care.

The input pull-up MOS is in the off state after a reset and in hardware standby mode. The prior state is retained in software standby mode.

Table 8.7 summarizes the input pull-up MOS states.

Table 8.7 Input Pull-Up MOS States

Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
Off	Off	On/Off	On/Off

[Legend]

Off: Always off.

On/Off: On when PADDR = 0 and PAODR = 1; otherwise off.

(4) Pin Functions

(a) Normal Extended Mode and Address-Data Multiplex Extended Mode

Port C pins can also function as the bus control output and IIC_2, IIC_3, and IIC_4 input/output pins. The relationship between register setting values and pin functions are as follows.

- PC7

  The PC7 pin functions as a bus control output pin.
- PC6

  When set for 16-bit bus width, the PC7 pin functions as a bus control output pin. When 8-bit bus width, the pin function is the same as that in single-chip mode.
- PC5 to PC0

  The pin functions are the same as those in single-chip mode.

10.2.5 Timer Control/Status Register (TCSR)

TCSR is used for counter clear selection and control of interrupt request signals.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
3	OCFA	0	R/(W)*	Output Compare Flag A Indicates that the FRC value matches the OCRA value. [Setting condition] When FRC = OCRA [Clearing condition] Read OCFA when OCFA = 1, then write 0 to OCFA
2	OCFB	0	R/(W)*	Output Compare Flag B Indicates that the FRC value matches the OCRB value. [Setting condition] When FRC = OCRB [Clearing condition] Read OCFB when OCFB = 1, then write 0 to OCFB
1	OVF	0	R/(W)*	Overflow Flag Indicates that the FRC has overflowed. [Setting condition] When FRC overflows (changes from H'FFFF to H'0000) [Clearing condition] Read OVF when OVF = 1, then write 0 to OVF
0	CCLRA	0	R/W	Counter Clear A Selects whether the FRC is to be cleared on compare-match A (when the FRC and OCRA values match). 0: FRC clearing is disabled 1: FRC is cleared on compare-match A

Note: * Only 0 can be written to clear the flag.

13.5.2 Multiprocessor Serial Data Reception

Figure 13.13 shows a sample flowchart for multiprocessor serial data reception. If the MPIE bit in SCR is set to 1, data is skipped until data with a 1 multiprocessor bit is sent. On receiving data with a 1 multiprocessor bit, the receive data is transferred to RDR. An RXI interrupt request is generated at this time. All other SCI operations are the same as in asynchronous mode. Figure 13.12 shows an example of SCI operation for multiprocessor format reception.

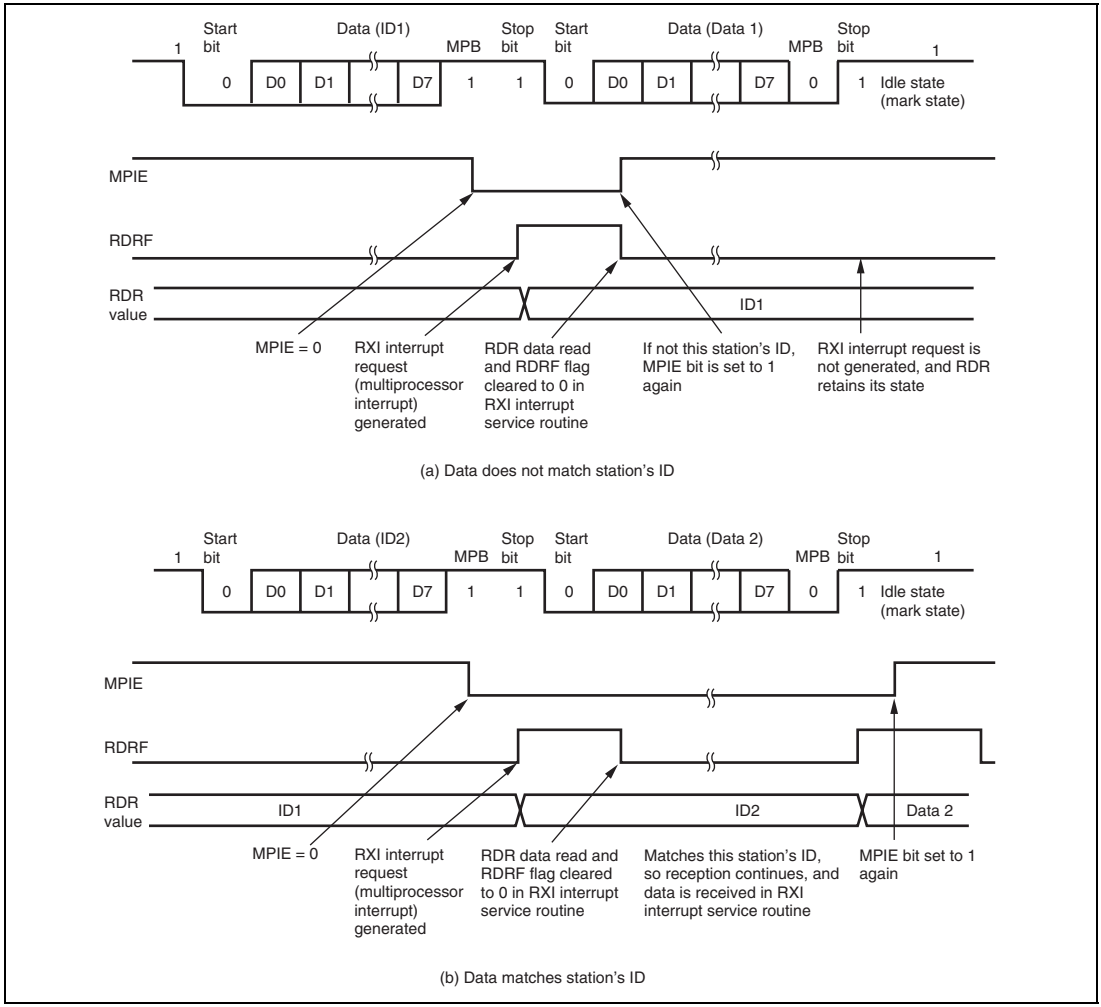

Figure 13.12 Example of SCI Operation in Reception (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)

Bit	Bit Name	Initial Value	R/W	Description
3	SCSATS	0	R/W	Selects the assertion timing of the $\overline{SCS}$ pin (valid in SSU and master mode). 0: Min. values of t_{LEAD} and t_{LAG} are 1/2 × t_{SUcyc} 1: Min. values of t_{LEAD} and t_{LAG} are 3/2 × t_{SUcyc}
2	SSODTS	0	R/W	Selects the data output timing of the SSO pin (valid in SSU and master mode) 0: While BIDE = 0, MSS = 1, and TE = 1 or while BIDE = 1, TE = 1, and RE = 0, the SSO pin outputs data 1: While BIDE = 0, MSS = 1, and TE = 1 or while BIDE = 1, TE = 1, and RE = 0, the SSO pin outputs data while the SCS pin is driven low
1, 0	—	All 0	R/W	Reserved These bits are always read as 0. The initial value should not be changed.

17.3.7 SS Transmit Data Registers 0 to 3 (SSTDR0 to SSTDR3)

SSTDR is an 8-bit register that stores transmit data. When 8-bit data length is selected by bits DATS1 and DATS0 in SSCRL, SSTDR0 is valid. When 16-bit data length is selected, SSTDR0 and SSTDR1 are valid. When 32-bit data length is selected, SSTDR0 to SSTDR3 are valid.

When the SSU detects that SSTRSR is empty, it transfers the transmit data written in SSTDR to SSTRSR and starts serial transmission. If the next transmit data has already been written to SSTDR during serial transmission, the SSU performs consecutive serial transmission.

Although SSTDR can always be read from or written to by the CPU and DMAC, to achieve reliable serial transmission, write transmit data to SSTDR after confirming that the TDRE bit in SSSR is set to 1.

Bit	Bit Name	Initial Value	R/W Slave	R/W Host	Description
2	PMEE	0	R/W	—	PME Output Enable Controls PME output in combination with the PMEB bit in HICR1. $\overline{\text{PME}}$ pin output is open-drain, and an external pull-up resistor (Vcc) is needed. The PD2DDR bit should be cleared to 0 when the LPC is used. PMEE PMEB 0 X : PME output disabled; general I/O function of pin PD2 is enabled 1 0 : PME output enabled, $\overline{\text{PME}}$ pin output goes to 0 level 1 1 : PME output enabled, $\overline{\text{PME}}$ pin output is high-impedance
1	LSMIE	0	R/W	—	LSMI output Enable Controls LSMI output in combination with the LSMIB bit in HICR1. $\overline{\text{LSMI}}$ pin output is open-drain, and an external pull-up resistor (Vcc) is needed. The PD1DDR bit should be cleared to 0 when the LPC is used. LSMIE LSMIB 0 X : LSMI output disabled; general I/O function of pin PD1 is enabled 1 0 : LSMI output enabled, LSMI pin output goes to 0 level 1 1 : LSMI output enabled, LSMI pin output is Hi-Z

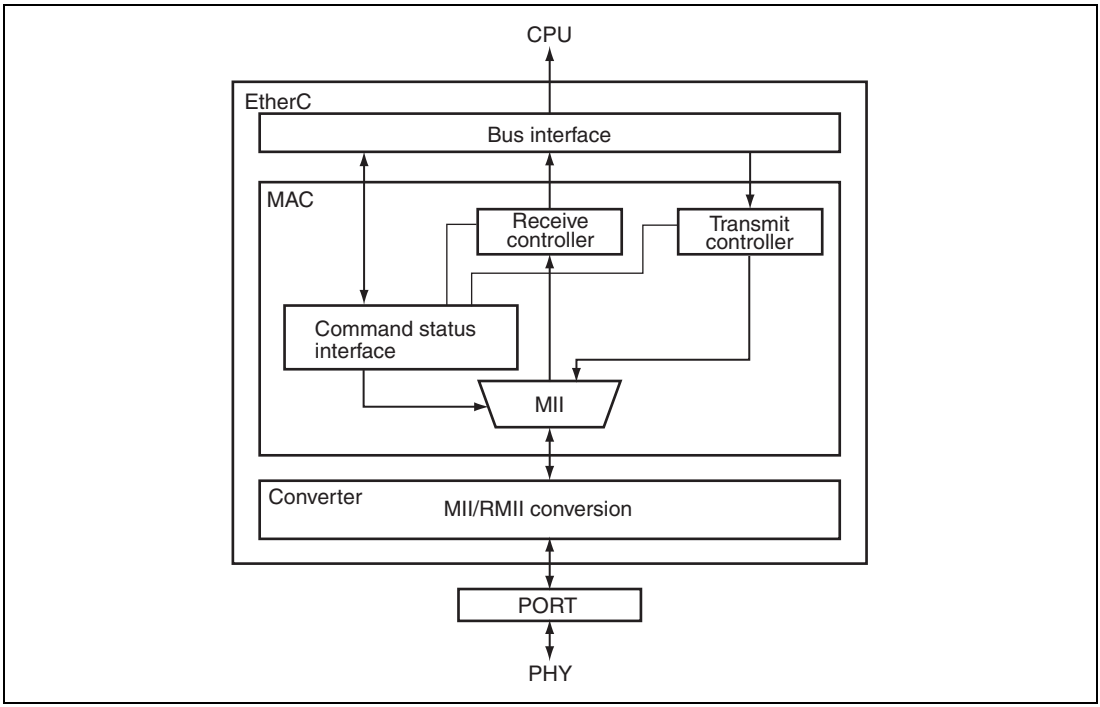

Figure 20.1 Configuration of EtherC

22.3.26 Transceiver Test Register 0 (TRNTREG0)

TRNTREG0 controls the built-in transceiver output signals. Setting the PTSTE bit to 1 specifies the transceiver output signals (USD+ and USD-) arbitrarily. Table 22.4 shows the relationship between TRNTREG0 setting and pin output.

Bit	Bit Name	Initial Value	R/W	Description
7	PTSTE	0	R/W	Pin Test Enable Enables the test control for the built-in transceiver output pins (USD+ and USD-).
6 to 4	—	All 0	R	Reserved These bits are always read as 0. The initial value should not be changed.
3	SUSPEND	0	R/W	Built-In Transceiver Output Signal Setting
2	txenl	0	R/W	SUSPEND: Sets the (SUSPEND) signal of the built-in transceiver.
1	txse0	0	R/W	txenl: Sets the output enable (txenl) signal of the built-in transceiver.
0	txdata	0	R/W	txse0: Sets the Signal-ended 0 (txse0) signal of the built-in transceiver. txdata: Sets the (txdata) signal of the built-in transceiver.

22.5.3 Suspend and Resume Operations

(1) Suspend Operation

When the USB bus enters the suspend state from the non-suspend state, processing should proceed as shown below.

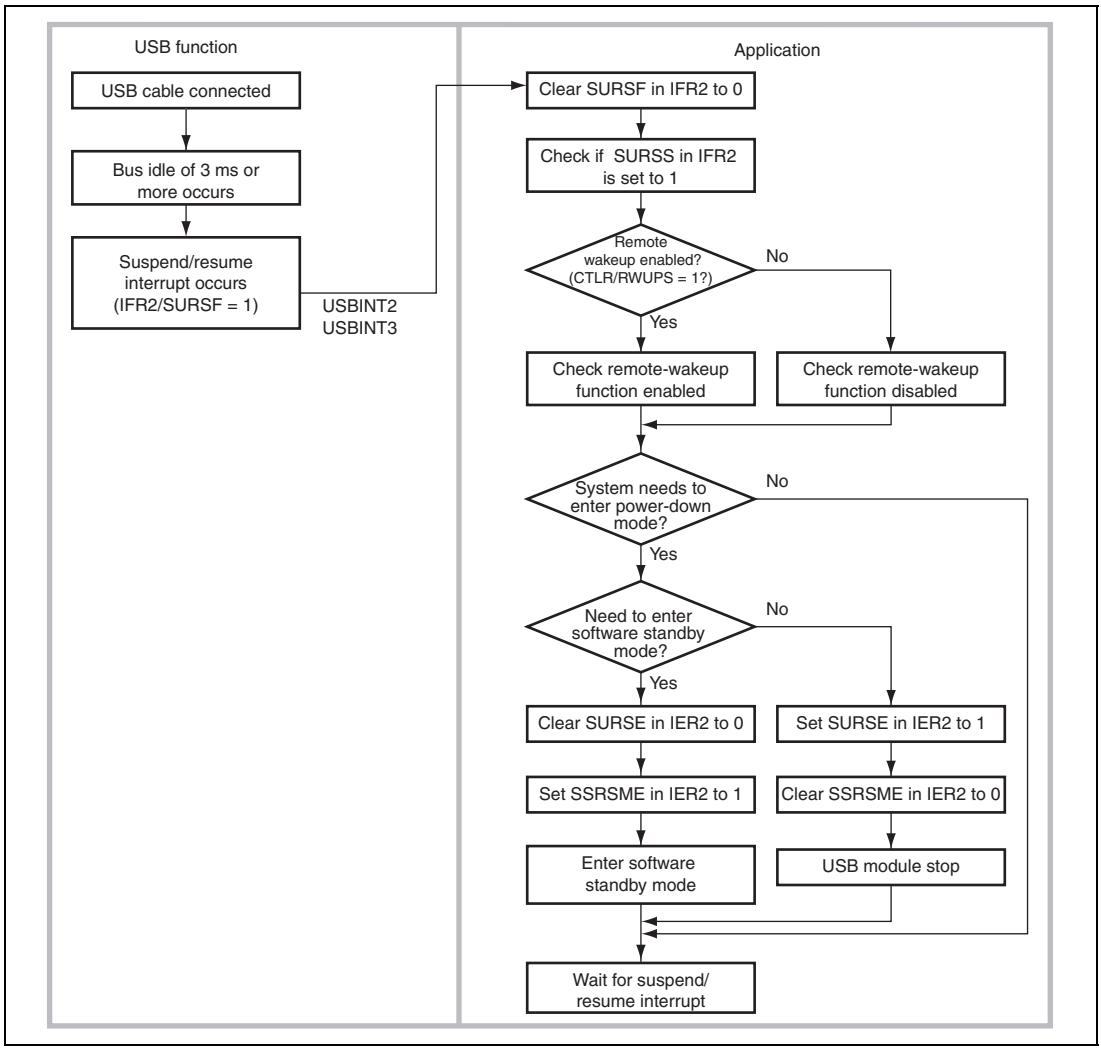

Figure 22.4 Suspend Operation

4. The ADST bit is not automatically cleared to 0 and steps 2 to 3 are repeated as long as the ADST bit remains set to 1. When the ADST bit is cleared to 0, A/D conversion stops and the A/D converter enters the idle state. After that, when the ADST bit is set to 1, the operation starts from the first channel again.

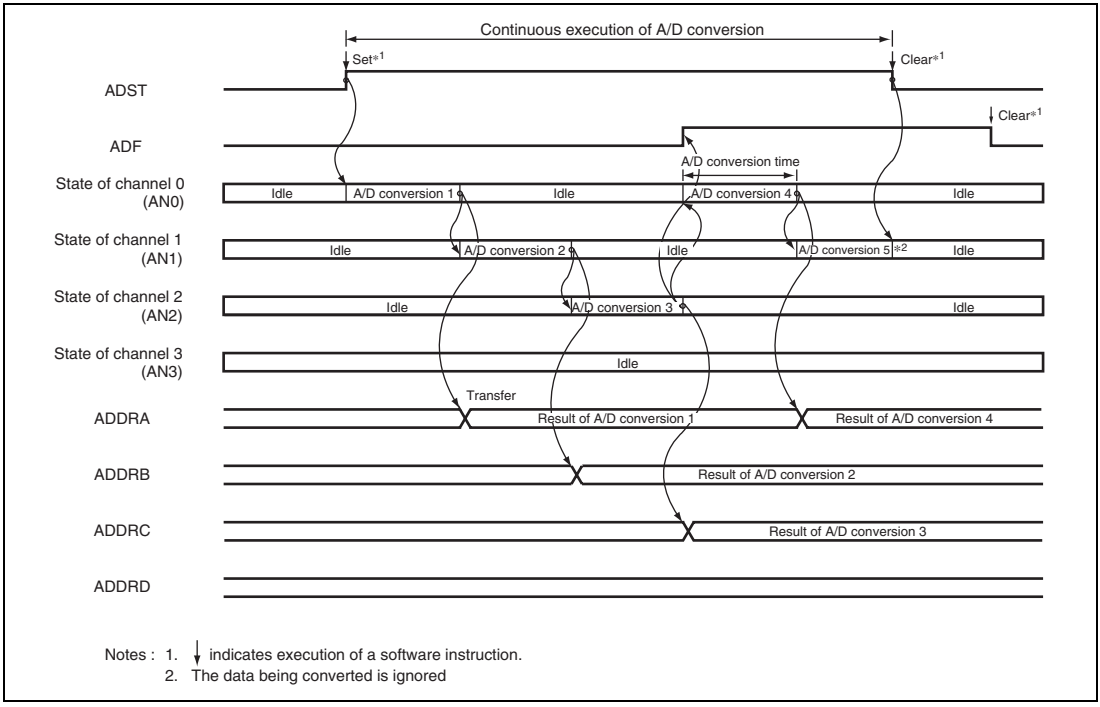

Figure 23.3 Example of A/D Converter Operation (When Channels AN0 to AN3 are Selected in Scan Mode)

Bit	Bit Name	Initial Value	R/W	Description
0	SF	—	R/W	Success/Fail Returns the result whether download is ended normally or not. The determination result whether program that is downloaded to the on-chip RAM is read back and then transferred to the on-chip RAM is returned. 0: Downloading on-chip program is ended normally (no error) 1: Downloading on-chip program is ended abnormally (error occurs)

Bit	Bit Name	Initial Value	R/W	Description
6	STS2	0	R/W	Standby Timer Select 2 to 0
5	STS1	0	R/W	Select the wait time for clock settling from clock oscillation start when canceling software standby mode. Select a wait time of 8 ms (oscillation settling time) or more, depending on the operating frequency.
4	STS0	0	R/W	With an external clock, select a wait time of 500 μs (external clock output settling delay time) or more, depending on the operating frequency.
				Table 28.1 shows the relationship between the STS2 to STS0 values and wait time.
3	DTSPEED	0	R/W	DTC Speed
				Specifies the operating clock for the bus masters (DTC) other than the CPU in medium-speed mode.
				0: All bus masters operate based on the medium-speed clock.
				1: The DTC operates based on the system clock.
				The operating clock is changed when a DTC transfer is requested even if the CPU operates based on the medium-speed clock.
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Select a clock for the bus master in high-speed mode or medium-speed mode.
0	SCK0	0	R/W	000: High-speed mode (Initial value)
				001: Medium-speed clock: φ/2
				010: Medium-speed clock: φ/4
				011: Medium-speed clock: φ/8
				100: Medium-speed clock: φ/16
				101: Medium-speed clock: φ/32
				11x: Must not be set.

[Legend]

x: Don't care

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
Event count status register	ECS	16	H'FE40	EVC	16	2
Event count control register	ECCR	8	H'FE42	EVC	8	2
Module stop control register A	MSTPCRA	8	H'FE43	SYSTEM	8	2
Noise canceler enable register	P3NCE	8	H'FE44	PORT	8	2
Noise canceler mode control register	P3NCMC	8	H'FE45	PORT	8	2
Noise canceler cycle setting register	NCCS	8	H'FE46	PORT	8	2
Port E output data register	PEODR	8	H'FE48	PORT	8	2
Port F output data register	PFODR	8	H'FE49	PORT	8	2
Port E input data register	PEPIN	8	H'FE4A	PORT	8	2
Port E data direction register	PEDDR	8	H'FE4A	PORT	8	2
Port F input data register	PFPIN	8	H'FE4B	PORT	8	2
Port F data direction register	PFDDR	8	H'FE4B	PORT	8	2
Port C output data register	PCODR	8	H'FE4C	PORT	8	2
Port D output data register	PDODR	8	H'FE4D	PORT	8	2
Port C input data register	PCPIN	8	H'FE4E	PORT	8	2
Port C data direction register	PCDDR	8	H'FE4E	PORT	8	2
Port D input data register	PDPIN	8	H'FE4F	PORT	8	2
Port D data direction register	PDDDR	8	H'FE4F	PORT	8	2
Flash code control/status register	FCCS	8	H'FE88	FLASH	8	2
Flash program code select register	FPCS	8	H'FE89	FLASH	8	2
Flash erase code select register	FECS	8	H'FE8A	FLASH	8	2
Flash key code register	FKEY	8	H'FE8C	FLASH	8	2
Flash MAT select register	FMATS	8	H'FE8D	FLASH	8	2
Flash transfer destination address register	FTDAR	8	H'FE8E	FLASH	8	2
I^2C bus control register_4	ICCR_4	8	H'FE90	IIC_4	8	2
I^2C bus status register_4	ICSR_4	8	H'FE91	IIC_4	8	2
I^2C bus data register_4	ICDR_4	8	H'FE92	IIC_4	8	2
Second slave address register_4	SARX_4	8	H'FE92	IIC_4	8	2