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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	34MHz
Connectivity	Ethernet, I²C, LPC, PECI, SCI, SSU, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	110
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f2472vbr34v

7.3.1 Event Counter Handling Priority

EVENT0 to EVENT15 count handling is operated in the priority shown as below.

High Low

EVENT0 > EVENT1 · · · · · · · · · · EVENT14 > EVENT15

7.3.2 Usage Notes

There are following usage notes for this event counter because it uses the DTC.

1. Continuous events that are input from the same pin and out of DTC handling are ignored because the count up is operated by means of the DTC.
2. If some events are generated in short intervals, the priority of event counter handling is not ordered and events are not handled in order of arrival.
3. If the counter overflows, this event counter counts from H'0000 without generating an interrupt.

8.1.8 Port 8

Port 8 is an 8-bit I/O port. Port 8 pins can also function as the A/D converter external trigger input, SCI_1 and SCI_3 input/output, IIC_0 and IIC_1 input/output, and interrupt input pins. Pins 83 to 80 perform the NMOS push-pull output. Port 8 has the following registers.

- Port 8 data direction register (P8DDR)
- Port 8 data register (P8DR)

(1) Port 8 Data Direction Register (P8DDR)

The individual bits of P8DDR specify input or output for the port 8 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P87DDR	0	W	If port 8 pins are specified for use as the general I/O port, the corresponding pins function as output port when the P8DDR bits are set to 1, and as input port when cleared to 0. Since this register is allocated to the same address as PBPIN, states of the port 8 pins are when this register is read.
6	P86DDR	0	W	
5	P85DDR	0	W	
4	P84DDR	0	W	
3	P83DDR	0	W	
2	P82DDR	0	W	
1	P81DDR	0	W	
0	P80DDR	0	W	

8.2.5 Port 5

Port 5 is an 8-bit I/O port. Port 5 pins can also function as the SCIF, SCI_1, and SSU input/output, bus control output, system clock output, external subclock input, and interrupt input pins. Port 5 has the following registers.

- Port 5 data direction register (P5DDR)
- Port 5 data register (P5DR)

(1) Port 5 Data Direction Register (P5DDR)

The individual bits of P5DDR specify input or output for the port 5 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P57DDR	0	W	If port 5 pins are specified for use as the general I/O port, the corresponding pins function as output port when the P5DDR bits are set to 1, and as input port when cleared to 0.
6	P56DDR	0	W	The corresponding port 5 pin functions as the system clock output pin (φ) when this bit is set to 1, and as the general I/O port when cleared to 0.
5	P55DDR	0	W	If port 5 pins are specified for use as the general I/O port, the corresponding pins function as output port when the P5DDR bits are set to 1, and as input port when cleared to 0.
4	P54DDR	0	W	
3	P53DDR	0	W	
2	P52DDR	0	W	
1	P51DDR	0	W	
0	P50DDR	0	W	

Since the value of the subsequent six bits is B'0000 01, an additional pulse is output only at the location of base pulse No. 63 according to table 9.4. Thus, an additional pulse of 1/256 × (T) is to be added to the base pulse.

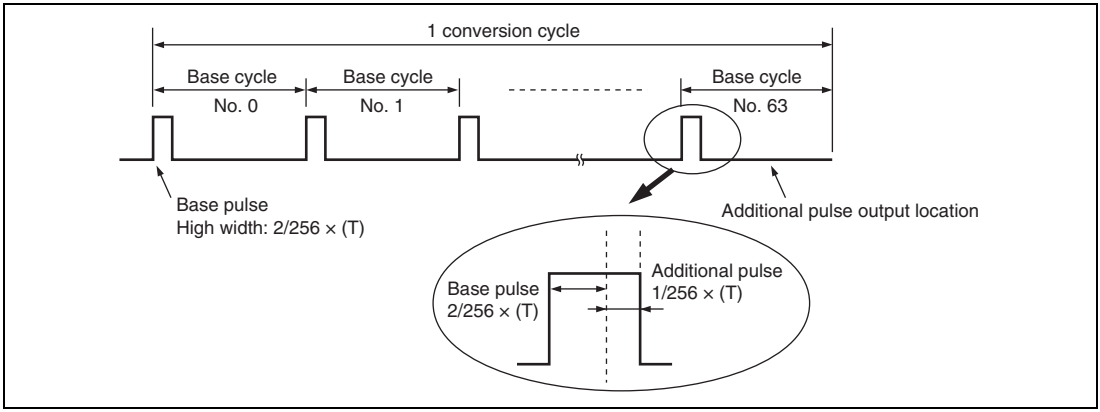


Figure 9.6 Output Waveform when DADR = H'0207 (OS = 1)

However, when CFS = 0 (base cycle = resolution (T) × 64), the duty cycle of the base pulse is determined by the upper six bits and the locations of the additional pulses by the subsequent eight bits with a method similar to as above.

10.5 Usage Notes

10.5.1 Conflict between FRC Write and Clear

If an internal counter clear signal is generated during the state after an FRC write cycle, the clear signal takes priority and the write is not performed. Figure 10.8 shows the timing for this type of conflict.

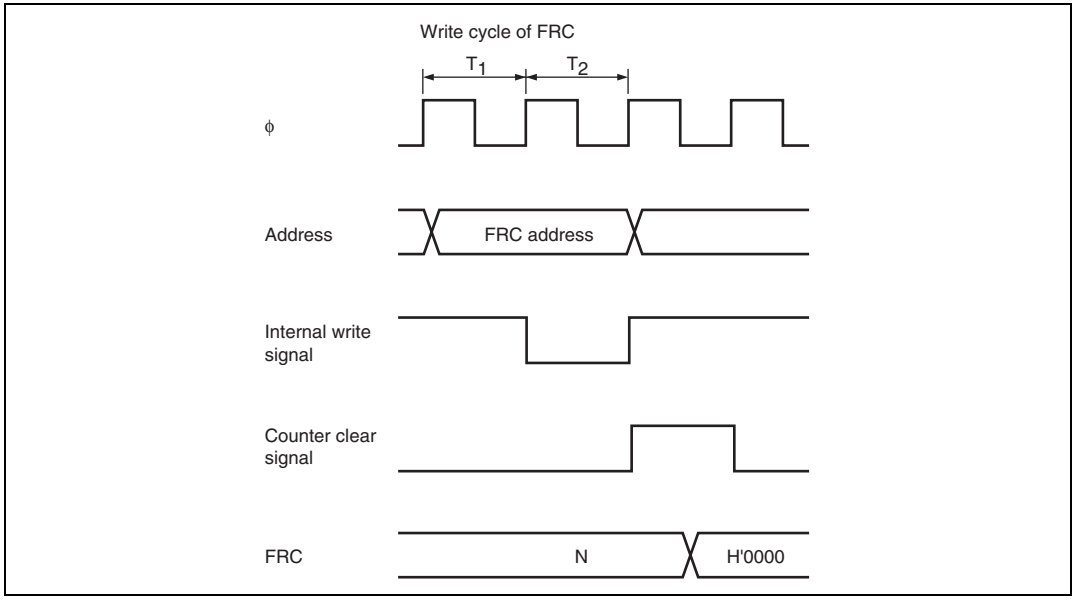


Figure 10.8 Conflict between FRC Write and Clear

11.3.3 Timing of Counter Clear at Compare-Match

TCNT is cleared when compare-match A or compare-match B occurs, depending on the setting of the CCLR1 and CCLR0 bits in TCR. Figure 11.5 shows the timing of clearing the counter by a compare-match.

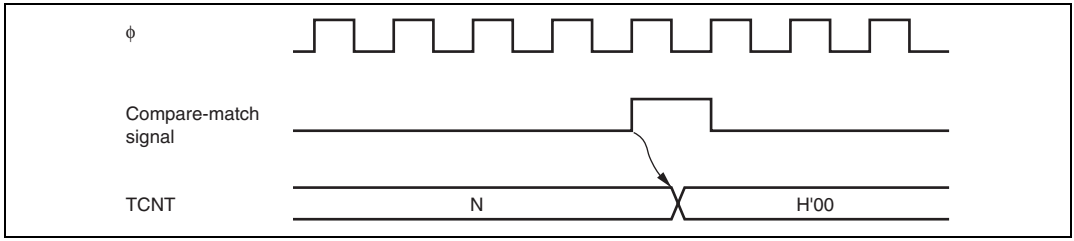


Figure 11.5 Timing of Counter Clear by Compare-Match

11.3.4 Timing of Overflow Flag (OVF) Setting

The OVF bit in TCSR is set to 1 when the TCNT overflows (changes from H'FF to H'00). Figure 11.6 shows the timing of OVF flag setting.

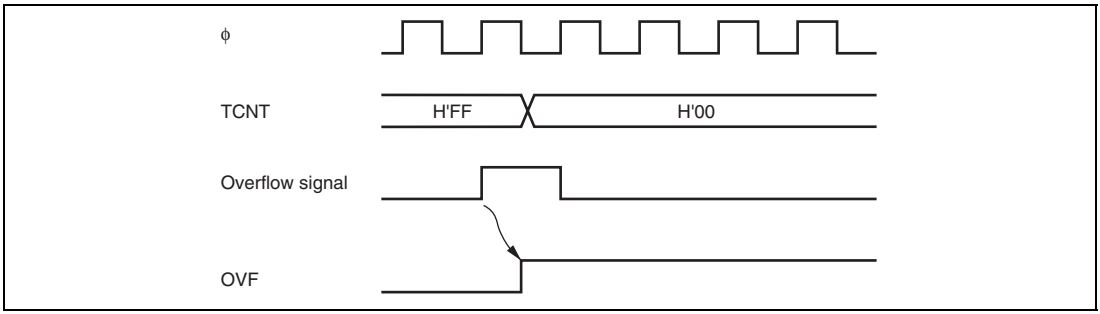


Figure 11.6 Timing of OVF Flag Setting

12.3.2 Timer Control/Status Register (TCSR)

TCSR selects the clock source to be input to TCNT, and the timer mode.

- TCSR_0

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*	Overflow Flag Indicates that TCNT has overflowed (changes from H'FF to H'00). [Setting conditions] • When TCNT overflows (changes from H'FF to H'00) • When internal reset request generation is selected in watchdog timer mode, OVF is cleared automatically by the internal reset. [Clearing conditions] • When TCSR is read when OVF = 1, then 0 is written to OVF • When 0 is written to TME
6	WT/$\overline{IT}$	0	R/W	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Interval timer mode 1: Watchdog timer mode
5	TME	0	R/W	Timer Enable When this bit is set to 1, TCNT starts counting. When this bit is cleared, TCNT stops counting and is initialized to H'00.
4	—	0	R/W	Reserved The initial value should not be changed.
3	RST/$\overline{NMI}$	0	R/W	Reset or NMI Selects to request an internal reset or an NMI interrupt when TCNT has overflowed. 0: An NMI interrupt is requested 1: An internal reset is requested

13.5.2 Multiprocessor Serial Data Reception

Figure 13.13 shows a sample flowchart for multiprocessor serial data reception. If the MPIE bit in SCR is set to 1, data is skipped until data with a 1 multiprocessor bit is sent. On receiving data with a 1 multiprocessor bit, the receive data is transferred to RDR. An RXI interrupt request is generated at this time. All other SCI operations are the same as in asynchronous mode. Figure 13.12 shows an example of SCI operation for multiprocessor format reception.

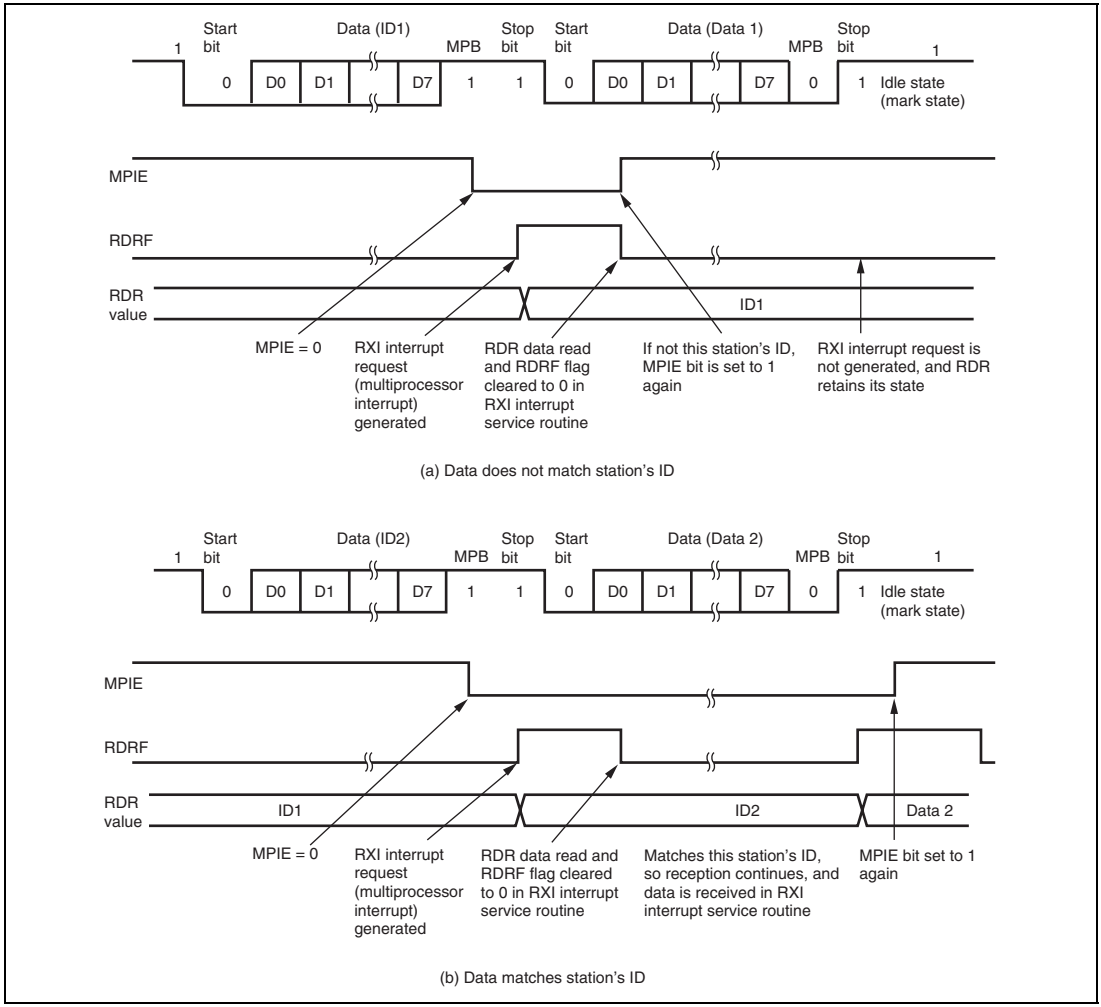


Figure 13.12 Example of SCI Operation in Reception (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)

Bit	Bit Name	Initial value	R/W	Description
25	RABT	0	R/W	Receive Abort Detection Indicates that the EtherC aborts receiving a frame because of failures during receiving the frame. 0: Frame reception has not been aborted or no receive directive 1: Frame receive has been aborted
24	RFCOF	0	R/W	Receive Frame Counter Overflow Indicates that the receive FIFO frame counter has overflowed. 0: Receive frame counter has not overflowed 1: Receive frame counter overflows
23	ADE	0	R/W	Address Error Indicates that the memory address that the E-DMAC tried to transfer is found illegal. 0: Illegal memory address not detected (normal operation) 1: Illegal memory address detected Note: When an address error is detected, the E-DMAC halts transmitting/receiving. To resume the operation, set the E-DMAC again after software reset by means of the SWR bit in EDMR.
22	ECI	0	R	EtherC Status Register Interrupt Source This bit is a read-only bit. When the source of an ECSR interrupt in the EtherC is cleared, this bit is also cleared. 0: EtherC status interrupt source has not been detected 1: EtherC status interrupt source has been detected

Section 22 USB Function Module (USB)

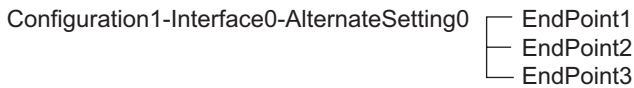
The H8S/2472 Group incorporates a USB function module (USB).

22.1 Features

- The UDC (USB device controller) conforming to USB2.0 and transceiver process USB protocol automatically.

  Automatic processing of USB standard commands for endpoint 0 (some commands and class/vendor commands require decoding and processing by firmware)
- Transfer speed: Supports full-speed (12 Mbps)
- Endpoint configuration:

Endpoint Name	Abbreviation	Transfer Type	Maximum Packet Size	FIFO Buffer Capacity (Byte)	DTC Transfer
Endpoint 0	EP0s	Setup	8	8	—
	EP0i	Control-in	8	8	—
	EP0o	Control-out	8	8	—
Endpoint 1	EP1	Bulk-out	64	128	Possible
Endpoint 2	EP2	Bulk-in	64	128	Possible
Endpoint 3	EP3	Interrupt-in	8	8	—



- Interrupt requests: Generates various interrupt signals necessary for USB transmission/reception
- Power mode: Self-powered mode

Note: The EtherC operates only in high-speed mode

22.3.21 DTC Transfer Setting Register (DMA)

DMA supports the DTC transfer that can be carried out between the endpoint 1 and 2 data registers and memory by the data transfer controller (DTC). Dual address transfer is performed in byte units. To initiate transfer by the DTC, necessary settings must be made to the DTC in addition to the setting of this register.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The initial value should not be changed.
2	PULLUP_E	0	R/W	PULLUP Enable This pin performs pull-up control for the D+ pin, with use of PUPDPLS as the pull-up control pin. 0: D+ pull-up is disabled. (The PULLUP pin is driven low.) 1: D+ pull-up is enabled. (The PULLUP pin is driven high.)

22.5.4 Control Transfer

Control transfer consists of three stages: setup, data (not always included), and status (figure 22.9). The data stage comprises a number of bus transactions. Operation flowcharts for each stage are shown below.

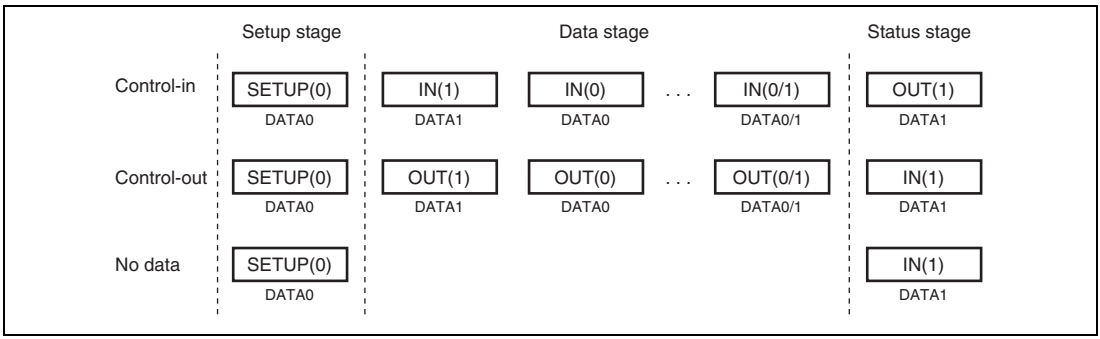


Figure 22.9 Transfer Stages in Control Transfer

22.5.5 EP1 Bulk-Out Transfer (Dual FIFOs)

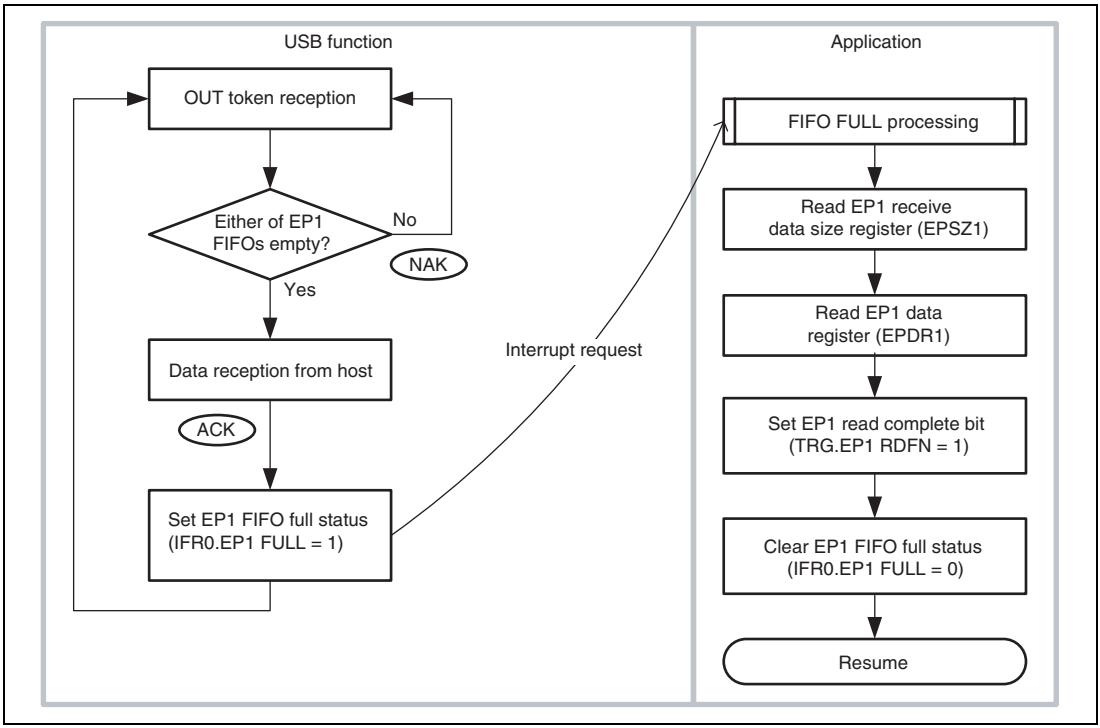


Figure 22.15 EP1 Bulk-Out Transfer Operation

EP1 has two 64-byte FIFOs, but the user can receive data and read receive data without being aware of this dual-FIFO configuration.

When one FIFO is full after reception is completed, the EP1FULL bit in IFR0 is set. After the first receive operation into one of the FIFOs when both FIFOs are empty, the other FIFO is empty, and so the next packet can be received immediately. When both FIFOs are full, NAK is returned to the host automatically. When reading of the receive data is completed following data reception, 1 is written to the EP1RDFN bit in TRG and 0 is written to the EP1FULL bit in IFR0. This operation empties the FIFO that has just been read, and makes it ready to receive the next packet.

23.3 Register Descriptions

The A/D converter has the following registers.

- A/D data register A (ADDRA)
- A/D data register B (ADDRB)
- A/D data register C (ADDRC)
- A/D data register D (ADDRD)
- A/D data register E (ADDRE)
- A/D data register F (ADDRF)
- A/D data register G (ADDRG)
- A/D data register H (ADDRH)
- A/D control/status register (ADCSR)
- A/D control register (ADCR)

23.3.1 A/D Data Registers A to H (ADDRA to ADDRH)

The ADDR are eight 16-bit read-only registers, ADDRA to ADDRH, which store the results of A/D conversion. The ADDR registers, which store a conversion result for each channel, are shown in table 23.2.

The converted 10-bit data is stored to bits 15 to 6. The lower 6-bit data is always read as 0.

The data bus between the CPU and the A/D converter is 16-bit width and can be read directly from the CPU. The ADDR must always be accessed in 16-bit unit. They cannot be accessed in 8-bit unit.

The results of A/D conversion are stored in each registers, when the ADF flag is set to 1.

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
RFLR	—	—	—	—	—	—	—	—	EtherC
	—	—	—	—	—	—	—	—	
	—	—	—	—	RFL11	RFL10	RFL9	RFL8	
	RFL7	RFL6	RFL5	RFL4	RFL3	RFL2	RFL1	RFL0	
PSR	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	LMON	
TROCR	TROC31	TROC30	TROC29	TROC28	TROC27	TROC26	TROC25	TROC24	
	TROC23	TROC22	TROC21	TROC20	TROC19	TROC18	TROC17	TROC16	
	TROC15	TROC14	TROC13	TROC12	TROC11	TROC10	TROC9	TROC8	
	TROC7	TROC6	TROC5	TROC4	TROC3	TROC2	TROC1	TROC0	
CDCR	COSDC31	COSDC30	COSDC29	COSDC28	COSDC27	COSDC26	COSDC25	COSDC24	
	COSDC23	COSDC22	COSDC21	COSDC20	COSDC19	COSDC18	COSDC17	COSDC16	
	COSDC15	COSDC14	COSDC13	COSDC12	COSDC11	COSDC10	COSDC9	COSDC8	
	COSDC7	COSDC6	COSDC5	COSDC4	COSDC3	COSDC2	COSDC1	COSDC0	
LCCR	LCC31	LCC30	LCC29	LCC28	LCC27	LCC26	LCC25	LCC24	
	LCC23	LCC22	LCC21	LCC20	LCC19	LCC18	LCC17	LCC16	
	LCC15	LCC14	LCC13	LCC12	LCC11	LCC10	LCC9	LCC8	
	LCC7	LCC6	LCC5	LCC4	LCC3	LCC2	LCC1	LCC0	
CNDCR	CNDC31	CNDC30	CNDC29	CNDC28	CNDC27	CNDC26	CNDC25	CNDC24	
	CNDC23	CNDC22	CNDC21	CNDC20	CNDC19	CNDC18	CNDC17	CNDC16	
	CNDC15	CNDC14	CNDC13	CNDC12	CNDC11	CNDC10	CNDC9	CNDC8	
	CNDC7	CNDC6	CNDC5	CNDC4	CNDC3	CNDC2	CNDC1	CNDC0	
CEFCR	CEFC31	CEFC30	CEFC29	CEFC28	CEFC27	CEFC26	CEFC25	CEFC24	
	CEFC23	CEFC22	CEFC21	CEFC20	CEFC19	CEFC18	CEFC17	CEFC16	
	CEFC15	CEFC14	CEFC13	CEFC12	CEFC11	CEFC10	CEFC9	CEFC8	
	CEFC7	CEFC6	CEFC5	CEFC4	CEFC3	CEFC2	CEFC1	CEFC0	
FRECR	FREC31	FREC30	FREC29	FREC28	FREC27	FREC26	FREC25	FREC24	
	FREC23	FREC22	FREC21	FREC20	FREC19	FREC18	FREC17	FREC16	
	FREC15	FREC14	FREC13	FREC12	FREC11	FREC10	FREC9	FREC8	
	FREC7	FREC6	FREC5	FREC4	FREC3	FREC2	FREC1	FREC0	

Section 30 Platform Environment Control Interface (PECI)

Renesas Technology Corporation is only able to provide information contained in this section to the parties with which we have concluded a nondisclosure agreement. Please contact one of our sales representatives for details.

If this module is not used, the PECI-related pins should be handled as follows. PECI is not supported by the H8S/2463 Group.

- Connect the PEVref pin to VSS.
- Leave the other PECI pins open.

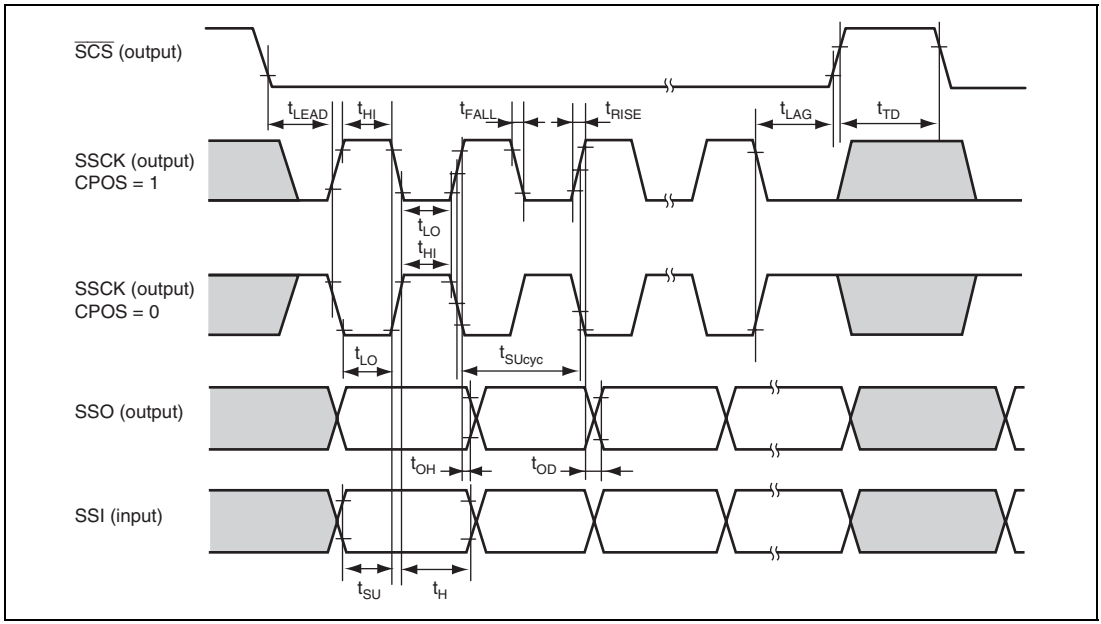


Figure 31.29 SSU Timing (Master, CPHS = 0)

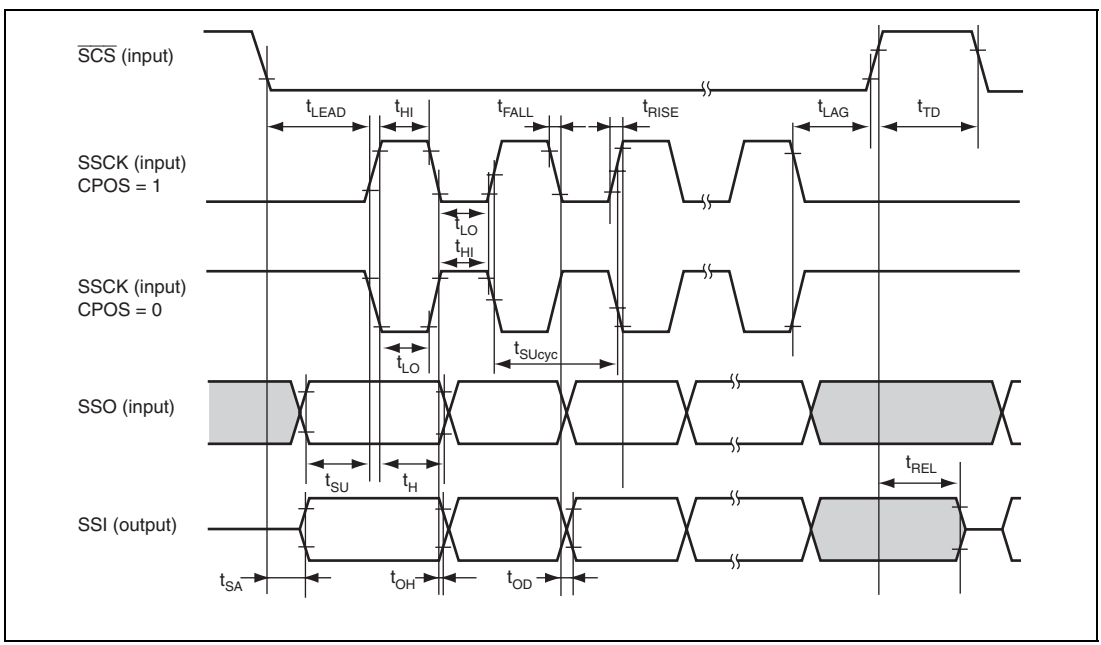


Figure 31.30 SSU Timing (Slave, CPHS = 1)

31.4 A/D Conversion Characteristics

Table 31.17 lists the A/D conversion characteristics.

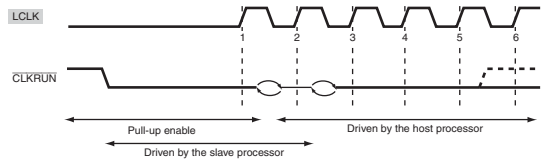
Table 31.17 A/D Conversion Characteristics (AN7 to AN0 Input: 80/160-State Conversion)

Condition A: VCC = 3.0 V to 3.6 V, AVCC = 3.0 V to 3.6 V, AVref = 3.0 V to AVCC
VSS = AVSS = 0 V, ϕ = 20 MHz

Condition B: VCC = 3.0 V to 3.6 V, AVCC = 3.0 V to 3.6 V, AVref = 3.0 V to AVCC,
VSS = AVSS = 0 V, ϕ = 20 MHz to 34 MHz

	Condition A			Condition B			
Item	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Resolution	10	10	10	10	10	10	Bits
Conversion time	—	—	4.0*[1]	—	—	4.7*[2]	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	5	—	—	5	kΩ
Nonlinearity error	—	—	±7.0	—	—	±7.0	LSB
Offset error	—	—	±7.5	—	—	±7.5	
Full-scale error	—	—	±7.5	—	—	±7.5	
Quantization error	—	—	±0.5	—	—	±0.5	
Absolute accuracy	—	—	±8.0	—	—	±8.0	

Notes: 1. Value when using the maximum operating frequency in single mode of 80 states.
2. Value when using the maximum operating frequency in single mode of 160 states.

Item	Page	Revision (See Manual for Details)
Section 19 LPC Interface (LPC) 19.3.1 Host Interface Control Registers 0 and 1 (HICR0 and HICR1) • HICR1	678	Amended **Bit** / **Bit Name** / **Description** 0 / LSCIB / LSCI output Bit Controls LSCI output in combination with the LSCIE bit. For details, refer to description on the LSCIE bit in HICR0.
Figure 19.11 Clock Start Request Timing	749	Amended 
Table 19.14 Host Address Example	755	Amended **Register** / **Host Address when LADR3 = H'A24F** / **Host Address when LADR3 = H'3FD0**
Section 20 Ethernet Controller (EtherC) Table 20.1 Pin Configuration	759	Amended and added **Type** / **Abbreviation** / **I/O** / **Function** PHY register interface signals / MDC / Output / Management Data Clock Reference clock signal for information transfer via MDIO Others / EXOUT / Output / External Output
Figure 20.10 1-Bit Data Read Flowchart	784	Modified