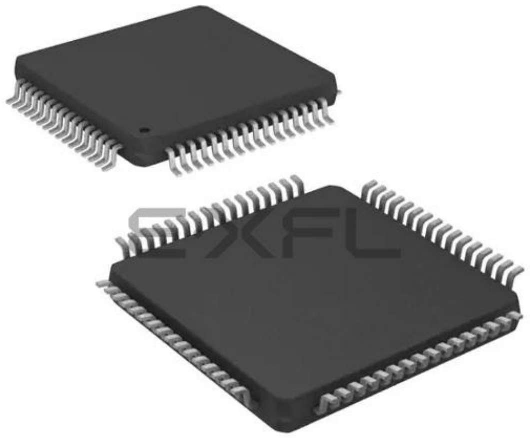


Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx120f064ht-v-pt

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input voltage low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For more information on MPLAB ICD 3 and MPLAB REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) DS50001765
- *"MPLAB® ICD 3 Design Advisory"* DS50001764
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide"* DS50001616
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) DS50001749

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

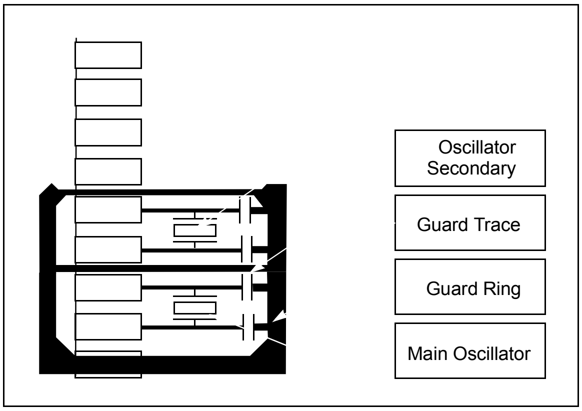
Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer or debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input voltage low (V_{IL}) requirements

2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



4.2 Special Function Register Maps

TABLE 4-2: BUS MATRIX REGISTER MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	BMXCON(1)	31:16	—	—	—	—	—	BMXCHEDMA	—	—	—	—	—	BMXERRIXI	BMXERRICD	BMXERRDMA	BMXERRDS	BMXERRIS	`041F`
		15:0	—	—	—	—	—	—	—	—	—	BMXWSDRM	—	—	—	BMXARB<2:0>			`0047`
2010	BMXDKPBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	`0000`
		15:0	BMXDKPBA<15:0>																`0000`
2020	BMXDUDBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	`0000`
		15:0	BMXDUDBA<15:0>																`0000`
2030	BMXDUPBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	`0000`
		15:0	BMXDUPBA<15:0>																`0000`
2040	BMXDRMSZ	31:16	BMXDRMSZ<31:0>																`xxxx`
		15:0																	`xxxx`
2050	BMXPUPBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	BMXPUPBA<19:16>				`0000`
		15:0	BMXPUPBA<15:0>																`0000`
2060	BMXPFMSZ	31:16	BMXPFMSZ<31:0>																`xxxx`
		15:0																	`xxxx`
2070	BMXBOOTSZ	31:16	BMXBOOTSZ<31:0>																`0000`
		15:0																	`0000`

Legend: x = unknown value on Reset; — = unimplemented, read as ‘`0`’. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.

TABLE 5-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source[1]	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
			Flag	Enable	Priority	Sub-priority	
CNA – PORTA Input Change Interrupt	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>	Yes
CNB – PORTB Input Change Interrupt	45	33	IFS1<13>	IEC1<13>	IPC8<12:10>	IPC8<9:8>	Yes
CNC – PORTC Input Change Interrupt	46	33	IFS1<14>	IEC1<14>	IPC8<12:10>	IPC8<9:8>	Yes
CND – PORTD Input Change Interrupt	47	33	IFS1<15>	IEC1<15>	IPC8<12:10>	IPC8<9:8>	Yes
CNE – PORTE Input Change Interrupt	48	33	IFS1<16>	IEC1<16>	IPC8<12:10>	IPC8<9:8>	Yes
CNF – PORTF Input Change Interrupt	49	33	IFS1<17>	IEC1<17>	IPC8<12:10>	IPC8<9:8>	Yes
CNG – PORTG Input Change Interrupt	50	33	IFS1<18>	IEC1<18>	IPC8<12:10>	IPC8<9:8>	Yes
PMP – Parallel Master Port	51	34	IFS1<19>	IEC1<19>	IPC8<20:18>	IPC8<17:16>	Yes
PMPE – Parallel Master Port Error	52	34	IFS1<20>	IEC1<20>	IPC8<20:18>	IPC8<17:16>	Yes
SPI2E – SPI2 Fault	53	35	IFS1<21>	IEC1<21>	IPC8<28:26>	IPC8<25:24>	Yes
SPI2RX – SPI2 Receive Done	54	35	IFS1<22>	IEC1<22>	IPC8<28:26>	IPC8<25:24>	Yes
SPI2TX – SPI2 Transfer Done	55	35	IFS1<23>	IEC1<23>	IPC8<28:26>	IPC8<25:24>	Yes
U2E – UART2 Error	56	36	IFS1<24>	IEC1<24>	IPC9<4:2>	IPC9<1:0>	Yes
U2RX – UART2 Receiver	57	36	IFS1<25>	IEC1<25>	IPC9<4:2>	IPC9<1:0>	Yes
U2TX – UART2 Transmitter	58	36	IFS1<26>	IEC1<26>	IPC9<4:2>	IPC9<1:0>	Yes
I2C2B – I2C2 Bus Collision Event	59	37	IFS1<27>	IEC1<27>	IPC9<12:10>	IPC9<9:8>	Yes
I2C2S – I2C2 Slave Event	60	37	IFS1<28>	IEC1<28>	IPC9<12:10>	IPC9<9:8>	Yes
I2C2M – I2C2 Master Event	61	37	IFS1<29>	IEC1<29>	IPC9<12:10>	IPC9<9:8>	Yes
U3E – UART3 Error	62	38	IFS1<30>	IEC1<30>	IPC9<20:18>	IPC9<17:16>	Yes
U3RX – UART3 Receiver	63	38	IFS1<31>	IEC1<31>	IPC9<20:18>	IPC9<17:16>	Yes
U3TX – UART3 Transmitter	64	38	IFS2<0>	IEC2<0>	IPC9<20:18>	IPC9<17:16>	Yes
U4E – UART4 Error	65	39	IFS2<1>	IEC2<1>	IPC9<28:26>	IPC9<25:24>	Yes
U4RX – UART4 Receiver	66	39	IFS2<2>	IEC2<2>	IPC9<28:26>	IPC9<25:24>	Yes
U4TX – UART4 Transmitter	67	39	IFS2<3>	IEC2<3>	IPC9<28:26>	IPC9<25:24>	Yes
U5E – UART5 Error[2]	68	40	IFS2<4>	IEC2<4>	IPC10<4:2>	IPC10<1:0>	Yes
U5RX – UART5 Receiver[2]	69	40	IFS2<5>	IEC2<5>	IPC10<4:2>	IPC10<1:0>	Yes
U5TX – UART5 Transmitter[2]	70	40	IFS2<6>	IEC2<6>	IPC10<4:2>	IPC10<1:0>	Yes
CTMU – CTMU Event[2]	71	41	IFS2<7>	IEC2<7>	IPC10<12:10>	IPC10<9:8>	Yes
DMA0 – DMA Channel 0	72	42	IFS2<8>	IEC2<8>	IPC10<20:18>	IPC10<17:16>	No
DMA1 – DMA Channel 1	73	43	IFS2<9>	IEC2<9>	IPC10<28:26>	IPC10<25:24>	No
DMA2 – DMA Channel 2	74	44	IFS2<10>	IEC2<10>	IPC11<4:2>	IPC11<1:0>	No
DMA3 – DMA Channel 3	75	45	IFS2<11>	IEC2<11>	IPC11<12:10>	IPC11<9:8>	No
CMP3 – Comparator 3 Interrupt	76	46	IFS2<12>	IEC2<12>	IPC11<20:18>	IPC11<17:16>	No
CAN1 – CAN1 Event	77	47	IFS2<13>	IEC2<13>	IPC11<28:26>	IPC11<25:24>	Yes
SPI3E – SPI3 Fault	78	48	IFS2<14>	IEC2<14>	IPC12<4:2>	IPC12<1:0>	Yes
SPI3RX – SPI3 Receive Done	79	48	IFS2<15>	IEC2<15>	IPC12<4:2>	IPC12<1:0>	Yes
SPI3TX – SPI3 Transfer Done	80	48	IFS2<16>	IEC2<16>	IPC12<4:2>	IPC12<1:0>	Yes
SPI4E – SPI4 Fault[2]	81	49	IFS2<17>	IEC2<17>	IPC12<12:10>	IPC12<9:8>	Yes
SPI4RX – SPI4 Receive Done[2]	82	49	IFS2<18>	IEC2<18>	IPC12<12:10>	IPC12<9:8>	Yes
SPI4TX – SPI4 Transfer Done[2]	83	49	IFS2<19>	IEC2<19>	IPC12<12:10>	IPC12<9:8>	Yes
Lowest Natural Order Priority							

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX1XX/2XX/5XX 64/100-pin Controller Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

6.1 Control Registers

TABLE 6-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F400	NVMCON[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	LVDSTAT	—	—	—	—	—	—	—	NVMOP<3:0>				0000
F410	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
F420	NVMADDR[1]	31:16	NVMADDR<31:0>																0000
		15:0																	0000
F430	NVMDATA	31:16	NVMDATA<31:0>																0000
		15:0																	0000
F440	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.

9.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

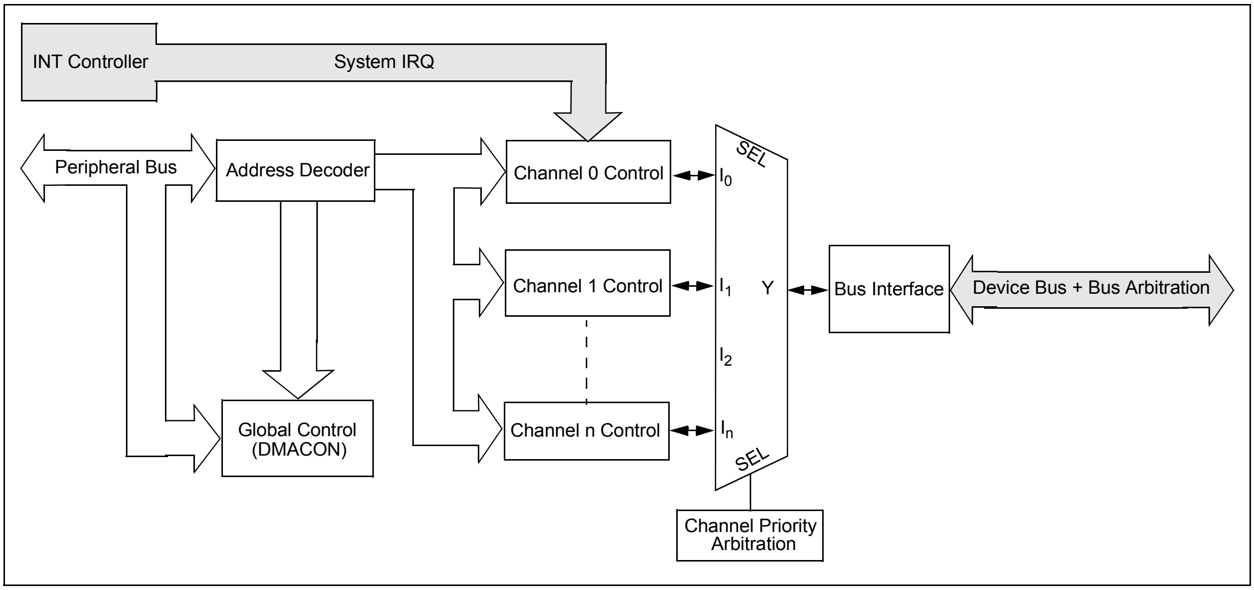
Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32 Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32 (such as Peripheral Bus (PBUS) devices: SPI, UART, PMP, etc.) or memory itself.

The following are some of the key features of the DMA controller module:

- Four identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

FIGURE 9-1: DMA BLOCK DIAGRAM



REGISTER 9-10: DCHxSSA: DMA CHANNEL ‘x’ SOURCE START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<7:0>							

Legend:
R = Readable bit   W = Writable bit   U = Unimplemented bit, read as ‘0’
-n = Value at POR   ‘1’ = Bit is set   ‘0’ = Bit is cleared   x = Bit is unknown

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits
Channel source start address.

Note: This must be the physical address of the source.

REGISTER 9-11: DCHxDSA: DMA CHANNEL ‘x’ DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<7:0>							

Legend:
R = Readable bit   W = Writable bit   U = Unimplemented bit, read as ‘0’
-n = Value at POR   ‘1’ = Bit is set   ‘0’ = Bit is cleared   x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits
Channel destination start address.

Note: This must be the physical address of the destination.

NOTES:

REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN(1,2)	CHIME(2)	PIV(2)	ALRMSYNC(3)	AMASK<3:0>(3)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARPT<7:0>(3)							

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ALRMEN:** Alarm Enable bit(1,2)

1 = Alarm is enabled
0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit(2)

1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit(2)

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.
When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit(3)

1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain
0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits(3)

0000 = Every half-second
0001 = Every second
0010 = Every 10 seconds
0011 = Every minute
0100 = Every 10 minutes
0101 = Every hour
0110 = Once a day
0111 = Once a week
1000 = Once a month
1001 = Once a year (except when configured for February 29, once every four years)
1010 = Reserved; do not use
1011 = Reserved; do not use
11xx = Reserved; do not use

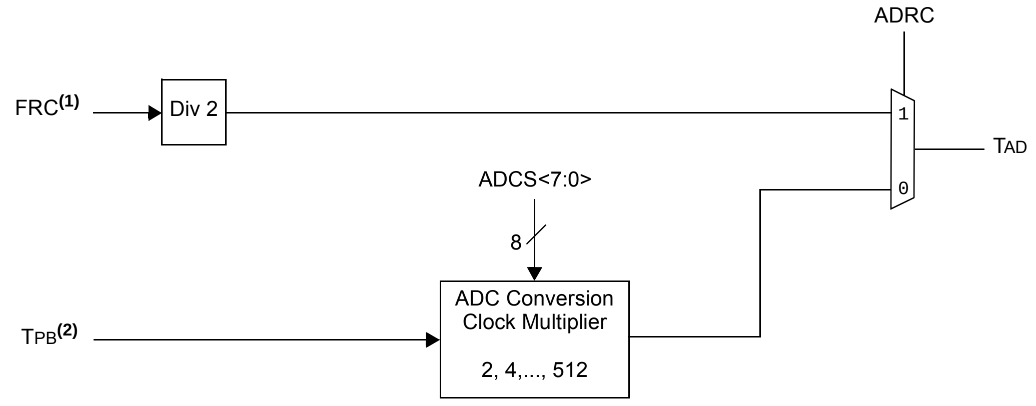
Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = ‘1’ (RTCCON<15>) and ALRMSYNC = 1.

3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

FIGURE 22-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



Note 1: See **Section 31.0 “40 MHz Electrical Characteristics”** for the exact FRC clock value.

2: Refer to Figure 8-1 in **Section 8.0 “Oscillator Configuration”** for more information.

REGISTER 22-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	—	CSCNA	—	—
7:0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFS	—	SMPI<3:0>				BUFM	ALTS

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘`0`’

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	VREFH	VREFL
`000`	AVDD	AVss
`001`	External VREF+ pin	AVSS
`010`	AVDD	External VREF- pin
`011`	External VREF+ pin	External VREF- pin
`1xx`	AVDD	AVSS

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit
`1` = Enable Offset Calibration mode
Positive and negative inputs of the sample and hold amplifier are connected to VREFL
`0` = Disable Offset Calibration mode
The inputs to the sample and hold amplifier are controlled by AD1CHS or AD1CSSL

bit 11 **Unimplemented:** Read as ‘`0`’

bit 10 **CSCNA:** Input Scan Select bit
`1` = Scan inputs
`0` = Do not scan inputs

bit 9-8 **Unimplemented:** Read as ‘`0`’

bit 7 **BUFS:** Buffer Fill Status bit
Only valid when BUFM = `1`.
`1` = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7
`0` = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 **Unimplemented:** Read as ‘`0`’

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
`1111` = Interrupts at the completion of conversion for each 16th sample/convert sequence
`1110` = Interrupts at the completion of conversion for each 15th sample/convert sequence
•
•
•
`0001` = Interrupts at the completion of conversion for each 2nd sample/convert sequence
`0000` = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit
`1` = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8
`0` = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
`1` = Uses Sample A input multiplexer settings for first sample, then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples
`0` = Always use Sample A input multiplexer settings

REGISTER 22-4: AD1CHS: ADC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NB	—	CH0SB<5:0>					
23:16	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NA	—	CH0SA<5:0>					
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **CH0NB:** Negative Input Select bit for Sample B

`1` = Channel 0 negative input is AN1
`0` = Channel 0 negative input is VREFL

bit 30 **Unimplemented:** Read as ‘`0`’

bit 29-24 **CH0SB<5:0>:** Positive Input Select bits for Sample B

For 64-pin devices:

`011110` = Channel 0 positive input is Open[1]
`011101` = Channel 0 positive input is CTMU temperature sensor (CTMUT)[2]
`011100` = Channel 0 positive input is IVREF[3]
`011011` = Channel 0 positive input is AN27
•
•
•
`000001` = Channel 0 positive input is AN1
`000000` = Channel 0 positive input is AN0

For 100-pin devices:

`110010` = Channel 0 positive input is Open[1]
`110001` = Channel 0 positive input is CTMU temperature sensor (CTMUT)[2]
`110000` = Channel 0 positive input is IVREF[3]
`101111` = Channel 0 positive input is AN47
•
•
•
`0000001` = Channel 0 positive input is AN1
`0000000` = Channel 0 positive input is AN0

bit 23 **CH0NA:** Negative Input Select bit for Sample A Multiplexer Setting[3]

`1` = Channel 0 negative input is AN1
`0` = Channel 0 negative input is VREFL

bit 22 **Unimplemented:** Read as ‘`0`’

Note 1: This selection is only used with CTMU capacitive and time measurement.
2: See **Section 26.0 “Charge Time Measurement Unit (CTMU)”** for more information.
3: Internal precision 1.2V reference. See **Section 24.0 “Comparator”** for more information.

REGISTER 23-2: C1CFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

bit 10-8 **PRSEG<2:0>:** Propagation Time Segment bits[4]

`111` = Length is 8 x T_Q
•
•
•
`000` = Length is 1 x T_Q

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits[3]

`11` = Length is 4 x T_Q
`10` = Length is 3 x T_Q
`01` = Length is 2 x T_Q
`00` = Length is 1 x T_Q

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits

`111111` = T_Q = (2 x 64)/SYSCLK
`111110` = T_Q = (2 x 63)/SYSCLK
•
•
•
`000001` = T_Q = (2 x 2)/SYSCLK
`000000` = T_Q = (2 x 1)/SYSCLK

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
2: 3 Time bit sampling is not allowed for BRP < 2.
3: SJW ≤ SEG2PH.
4: The Time Quanta per bit must be greater than 7 (that is, T_{QBIT} > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = `100`).

NOTES:

REGISTER 28-6: DEVID: DEVICE AND REVISION ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	VER<3:0>[1]				DEVID<27:24>[1]			
23:16	R	R	R	R	R	R	R	R
	DEVID<23:16>[1]							
15:8	R	R	R	R	R	R	R	R
	DEVID<15:8>[1]							
7:0	R	R	R	R	R	R	R	R
	DEVID<7:0>[1]							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28	**VER<3:0>:** Revision Identifier bits[1]
bit 27-0	**DEVID<27:0>:** Device ID[1]

Note 1: See the *“PIC32 Flash Programming Specification”* (DS60001145) for a list of Revision and Device ID values.

TABLE 31-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			**Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		I/O Pins with PMP	VSS	—	0.15 VDD	V	
		I/O Pins	VSS	—	0.2 VDD	V	
DI18		SDAx, SCLx	VSS	—	0.3 VDD	V	SMBus disabled **(Note 4)**
DI19		SDAx, SCLx	VSS	—	0.8	V	SMBus enabled **(Note 4)**
	VIH	**Input High Voltage**					
DI20		I/O Pins not 5V-tolerant(5)	0.65 VDD	—	VDD	V	**(Note 4,6)**
		I/O Pins 5V-tolerant with PMP(5)	0.25 VDD + 0.8V	—	5.5	V	**(Note 4,6)**
		I/O Pins 5V-tolerant(5)	0.65 VDD	—	5.5	V	
DI28		SDAx, SCLx	0.65 VDD	—	5.5	V	SMBus disabled **(Note 4,6)**
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 **(Note 4,6)**
DI30	ICNPU	**Change Notification Pull-up Current**	—	-200	-50	μA	VDD = 3.3V, VPIN = VSS **(Note 3,6)**
DI31	ICNPD	**Change Notification Pull-down Current(4)**	50	200	—	μA	VDD = 3.3V, VPIN = VDD
	IIL	**Input Leakage Current (Note 3)**					
DI50		I/O Ports	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		Analog Input Pins	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI55		$\overline{\text{MCLR}}$(2)	—	—	±1	μA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, XT and HS modes

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

5: See the **“Device Pin Tables”** section for the 5V-tolerant pins.

6: The VIH specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic “high” internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External “input” logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

TABLE 31-10: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**[(1)]	**Typical**	**Max.**	**Units**	**Conditions**
BO10	V_{BOR}	BOR Event on V_{DD} transition high-to-low**(2)**	2.0	—	2.3	V	—

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below V_{DDMIN}.

TABLE 31-11: ELECTRICAL CHARACTERISTICS: HVD

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.[(1)]	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
HV10	V_{HVD}	High Voltage Detect on V_{CAP} pin	—	2.5	—	V	—

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

TABLE 31-34: ADC MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions (see Note 5): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
ADC Accuracy – Measurements with Internal VREF+/VREF-							
AD20d	Nr	Resolution	10 data bits			bits	**(Note 3)**
AD21d	INL	Integral Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)**
AD22d	DNL	Differential Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Notes 2,3)**
AD23d	GERR	Gain Error	> -4	—	< 4	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)**
AD24d	EOFF	Offset Error	> -2	—	< 2	Lsb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)**
AD25d	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance							
AD32b	SINAD	Signal to Noise and Distortion	55	58.5	—	dB	**(Notes 3,4)**
AD34b	ENOB	Effective Number of bits	9.0	9.5	—	bits	**(Notes 3,4)**

Note 1: These parameters are not characterized or tested in manufacturing.

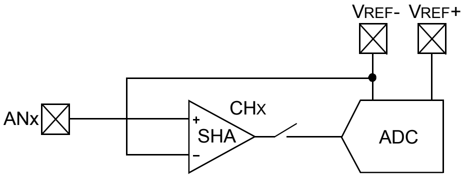
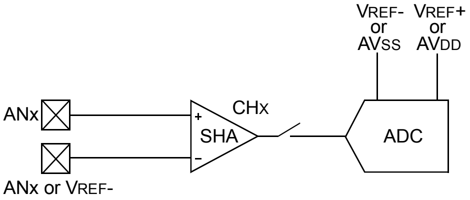
2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 31-35: 10-BIT CONVERSION RATE PARAMETERS

AC CHARACTERISTICS[2]			Standard Operating Conditions (see Note 3): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp		
ADC Speed	**TAD Min.**	**Sampling Time Min.**	**RS Max.**	**VDD**	**ADC Channels Configuration**
1 Msps to 400 ksps[1]	65 ns	132 ns	500Ω	3.0V to 3.6V	
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	

Note 1: External VREF- and VREF+ pins must be used for correct operation.

2: These parameters are characterized, but not tested in manufacturing.

3: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 31-36: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical[(1)]**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period[(2)]	65	—	—	ns	See Table 31-35
Conversion Rate							
AD55	TCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate (Sampling Speed)	—	—	1000	ksps	AVDD = 3.0V to 3.6V
			—	—	400	ksps	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	1 TAD	—	—	—	TSAMP must be ≥ 132 ns
Timing Parameters							
AD60	TPCS	Conversion Start from Sample Trigger[(3)]	—	1.0 TAD	—	—	Auto-Convert Trigger (SSRC<2:0> = `111`) not selected
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD	—	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = `1`)[(3)]	—	0.5 TAD	—	—	—
AD63	TDPU	Time to Stabilize Analog Stage from ADC Off to ADC On[(3)]	—	—	2	µs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

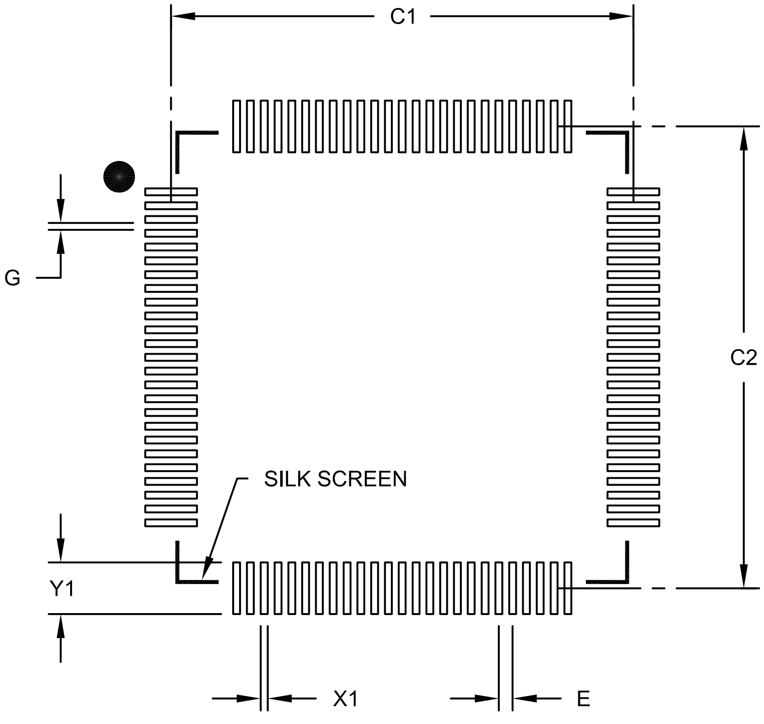
2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: Characterized by design but not tested.

4: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

100-Lead Plastic Thin Quad Flatpack (PT) - 12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B