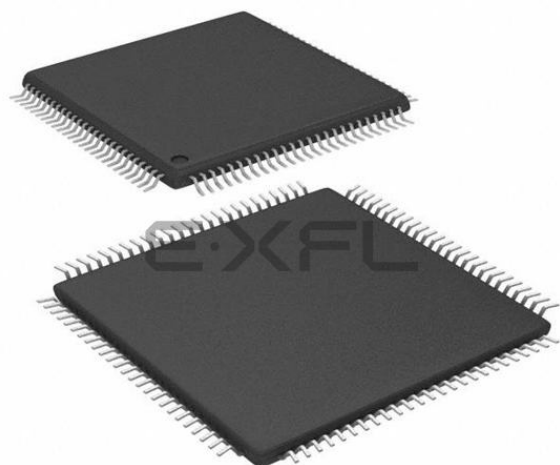




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx130f128lt-50i-pt

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

Device Pin Tables

TABLE 2: PIN NAMES FOR 64-PIN GENERAL PURPOSE DEVICES

64-PIN QFN ⁽⁴⁾ AND TQFP (TOP VIEW)			
PIC32MX120F064H PIC32MX130F128H PIC32MX150F256H PIC32MX170F512H			
		64	1
		64	1
		QFN⁽⁴⁾	TQFP
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN22/RPE5/PMD5/RE5	33	RPF3/RF3
2	AN23/PMD6/RE6	34	RPF2/RF2
3	AN27/PMD7/RE7	35	RPF6/SCK1/INT0/RF6
4	AN16/C1IND/RPG6/SCK2/PMA5/RG6	36	SDA1/RG3
5	AN17/C1INC/RPG7/PMA4/RG7	37	SCL1/RG2
6	AN18/C2IND/RPG8/PMA3/RG8	38	VDD
7	MCLR	39	OSC1/CLKI/RC12
8	AN19/C2INC/RPG9/PMA2/RG9	40	OSC2/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	RPD8/RTCC/RD8
11	AN5/C1INA/RPB5/RB5	43	RPD9/RD9
12	AN4/C1INB/RB4	44	RPD10/PMA15/RD10
13	PGED3/AN3/C2INA/RPB3/RB3	45	RPD11/PMA14/RD11
14	PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2	46	RPD0/RD0
15	PGEC1/VREF-/AN1/RPB1/CTED12/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN6/RPB6/RB6	49	AN24/RPD1/RD1
18	PGED2/AN7/RPB7/CTED3/RB7	50	AN25/RPD2/RD2
19	AVDD	51	AN26/C3IND/RPD3/RD3
20	AVSS	52	RPD4/PMWR/RD4
21	AN8/RPB8/CTED10/RB8	53	RPD5/PMRD/RD5
22	AN9/RPB9/CTED4/PMA7/RB9	54	C3INC/RD6
23	TMS/CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	55	C3INB/RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	VSS	57	VDD
26	VDD	58	C3INA/RPF0/RF0
27	TCK/AN12/PMA11/RB12	59	RPF1/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/RPB14/SCK3/CTED5/PMA1/RB14	61	PMD1/RE1
30	AN15/RPB15/OCFB/CTED6/PMA0/RB15	62	AN20/PMD2/RE2
31	RPF4/SDA2/PMA9/RF4	63	RPE3/CTPLS/PMD3/RE3
32	RPF5/SCL2/PMA8/RF5	64	AN21/PMD4/RE4

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
 - 2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 11.0 “I/O Ports”** for more information.
 - 3: Shaded pins are 5V tolerant.
 - 4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 5: PIN NAMES FOR 100-PIN USB DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW) PIC32MX230F128L PIC32MX530F128L PIC32MX250F256L PIC32MX550F256L PIC32MX270F512L PIC32MX570F512L 100 1			
Pin #	Full Pin Name	Pin #	Full Pin Name
71	RPD11/PMA14/RD11	86	VDD
72	RPD0/INT0/RD0	87	AN44/C3INA/RPF0/PMD11/RF0
73	SOSCI/RPC13/RC13	88	AN45/RPF1/PMD10/RF1
74	SOSCO/RPC14/T1CK/RC14	89	RPG1/PMD9/RG1
75	Vss	90	RPG0/PMD8/RG0
76	AN24/RPD1/RD1	91	RA6
77	AN25/RPD2/RD2	92	CTED8/RA7
78	AN26/C3IND/RPD3/RD3	93	AN46/PMD0/RE0
79	AN40/RPD12/PMD12/RD12	94	AN47/PMD1/RE1
80	AN41/PMD13/RD13	95	RG14
81	RPD4/PMWR/RD4	96	RG12
82	RPD5/PMRD/RD5	97	RG13
83	AN42/C3INC/PMD14/RD6	98	AN20/PMD2/RE2
84	AN43/C3INB/PMD15/RD7	99	RPE3/CTPLS/PMD3/RE3
85	VCAP	100	AN21/PMD4/RE4

- Note**
- 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
 - 2: Every I/O port pin (RAX-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 “I/O Ports”** for more information.
 - 3: Shaded pins are 5V tolerant.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP			
U3CTS	PPS	PPS	I	ST	UART3 Clear to Send
U3RTS	PPS	PPS	O	—	UART3 Ready to Send
U3RX	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	O	—	UART3 Transmit
U4CTS	PPS	PPS	I	ST	UART4 Clear to Send
U4RTS	PPS	PPS	O	—	UART4 Ready to Send
U4RX	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	O	—	UART4 Transmit
U5CTS	—	PPS	I	ST	UART5 Clear to Send
U5RTS	—	PPS	O	—	UART5 Ready to Send
U5RX	—	PPS	I	ST	UART5 Receive
U5TX	—	PPS	O	—	UART5 Transmit
SCK1	35 ⁽¹⁾ , 50 ⁽²⁾	55 ⁽¹⁾ , 70 ⁽²⁾	I/O	ST	Synchronous Serial Clock Input/Output for SPI1
SDI1	PPS	PPS	I	—	SPI1 Data In
SDO1	PPS	PPS	O	ST	SPI1 Data Out
SS1	PPS	PPS	I/O	—	SPI1 Slave Synchronization for Frame Pulse I/O
SCK2	4	10	I/O	ST	Synchronous Serial Clock Input/Output for SPI2
SDI2	PPS	PPS	I	—	SPI2 Data In
SDO2	PPS	PPS	O	ST	SPI2 Data Out
SS2	PPS	PPS	I/O	—	SPI2 Slave Synchronization for Frame Pulse I/O
SCK3	29	39	I/O	ST	Synchronous Serial Clock Input/Output for SPI3
SDI3	PPS	PPS	I	—	SPI3 Data In
SDO3	PPS	PPS	O	ST	SPI3 Data Out
SS3	PPS	PPS	I/O	—	SPI3 Slave Synchronization for Frame Pulse I/O
SCK4	—	48	I/O	ST	Synchronous Serial Clock Input/Output for SPI4
SDI4	—	PPS	I	—	SPI4 Data In
SDO4	—	PPS	O	ST	SPI4 Data Out
SS4	—	PPS	I/O	—	SPI4 Slave Synchronization for Frame Pulse I/O
SCL1	37 ⁽¹⁾ , 44 ⁽²⁾	57 ⁽¹⁾ , 66 ⁽²⁾	I/O	ST	Synchronous Serial Clock Input/Output for I2C1
SDA1	36 ⁽¹⁾ , 43 ⁽²⁾	56 ⁽¹⁾ , 67 ⁽²⁾	I/O	ST	Synchronous Serial Data Input/Output for I2C1
SCL2	32	58	I/O	ST	Synchronous Serial Clock Input/Output for I2C2
SDA2	31	59	I/O	ST	Synchronous Serial Data Input/Output for I2C2
TMS	23	17	I	ST	JTAG Test Mode Select Pin
TCK	27	38	I	ST	JTAG Test Clock Input Pin
TDI	28	60	I	—	JTAG Test Clock Input Pin
TDO	24	61	O	—	JTAG Test Clock Output Pin

Legend: CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

- Note 1:** This pin is only available on devices without a USB module.
2: This pin is only available on devices with a USB module.
3: This pin is not available on 64-pin devices with a USB module.
4: This pin is only available on 100-pin devices without a USB module.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

3.0 CPU

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS60001113) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). Resources for the MIPS32® M4K® Processor Core are available at <http://www.imgtec.com>.

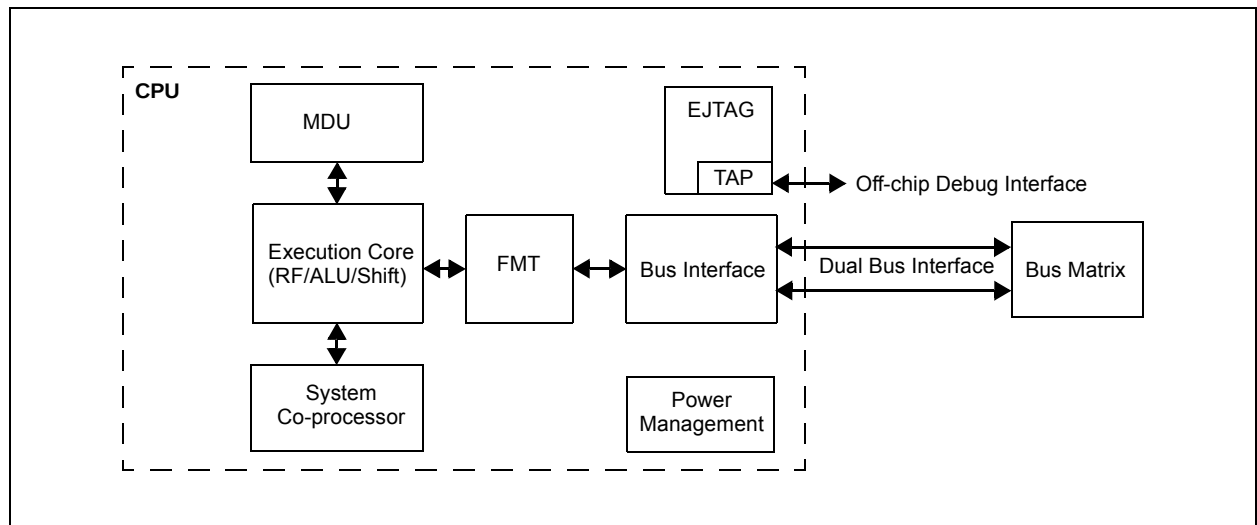
The the MIPS32® M4K® Processor Core is the heart of the PIC32MX1XX/2XX/5XX 64/100-pin device processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

3.1 Features

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32® Enhanced Architecture (Release 2):
 - Multiply-accumulate and multiply-subtract instructions
 - Targeted multiply instruction
 - Zero/One detect instructions
 - WAIT instruction
 - Conditional move instructions (MOVN, MOVZ)
 - Vectored interrupts
 - Programmable exception vector base
 - Atomic interrupt enable/disable
 - Bit field manipulation instructions

- MIPS16e® Code Compression:
 - 16-bit encoding of 32-bit instructions to improve code density
 - Special PC-relative instructions for efficient loading of addresses and constants
 - SAVE and RESTORE macro instructions for setting up and tearing down stack frames within subroutines
 - Improved support for handling 8 and 16-bit data types
- Simple Fixed Mapping Translation (FMT) Mechanism:
- Simple Dual Bus Interface:
 - Independent 32-bit address and data buses
 - Transactions can be aborted to improve interrupt latency
- Autonomous Multiply/Divide Unit (MDU):
 - Maximum issue rate of one 32x16 multiply per clock
 - Maximum issue rate of one 32x32 multiply every other clock
 - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension-dependent)
- Power Control:
 - Minimum frequency: 0 MHz
 - Low-Power mode (triggered by WAIT instruction)
 - Extensive use of local gated clocks
- EJTAG Debug:
 - Support for single stepping
 - Virtual instruction and data address/value
 - Breakpoints

FIGURE 3-1: MIPS32® M4K® PROCESSOR CORE BLOCK DIAGRAM



PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDKPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDKPBA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits

When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** Read-Only bits

Value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

7.0 RESETS

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. “Resets”** (DS60001118) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- MCLR: Master Clear Reset pin
- SWR: Software Reset
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- CMR: Configuration Mismatch Reset
- HVDR: High Voltage Detect Reset

A simplified block diagram of the Reset module is illustrated in Figure 7-1.

FIGURE 7-1: SYSTEM RESET BLOCK DIAGRAM

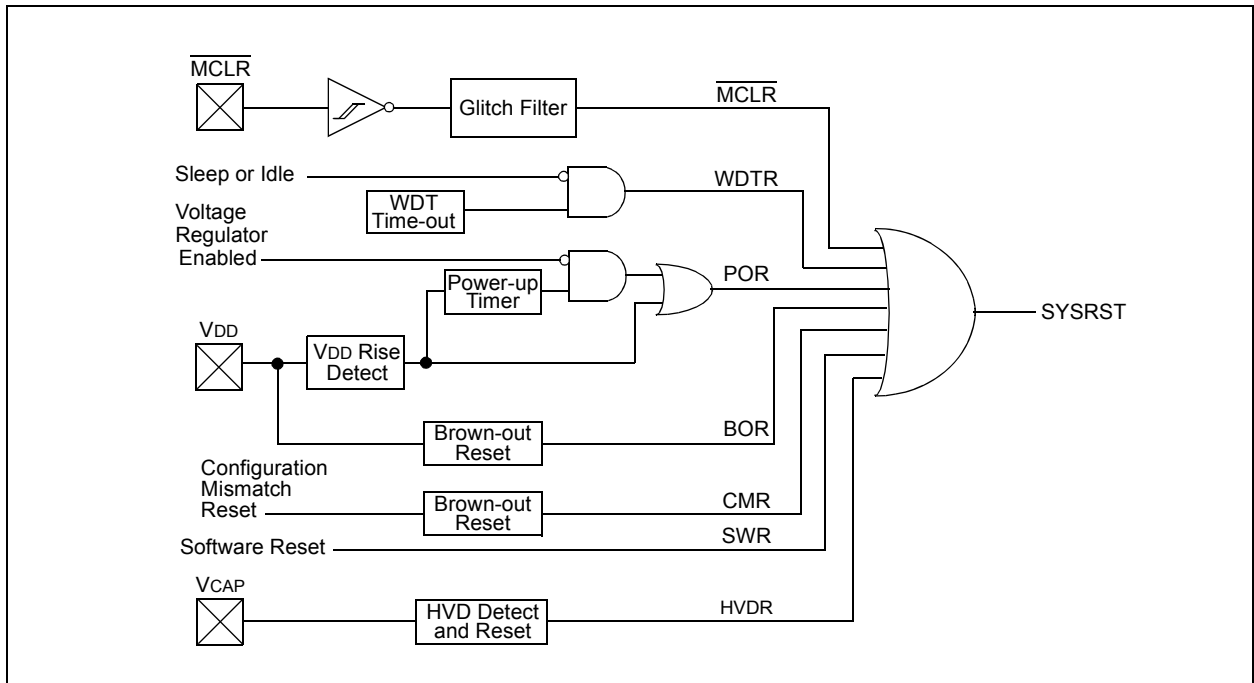


TABLE 9-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3060	DCH0CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3070	DCH0ECON	31:16	—	—	—	—	—	—	—	CHAIRQ<7:0>									00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FFF8
3080	DCH0INT	31:16	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000	
		15:0	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000	
3090	DCH0SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
30A0	DCH0DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
30B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSSIZ<15:0>																0000
30C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>																0000
30D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>																0000
30E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>																0000
30F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>																0000
3100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>																0000
3110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
3120	DCH1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
3130	DCH1ECON	31:16	—	—	—	—	—	—	—	CHAIRQ<7:0>									00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FFF8
3140	DCH1INT	31:16	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000	
		15:0	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000	
3150	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
3160	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET, and INV Registers” for more information.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 9-14: DCHxSPTR: DMA CHANNEL 'x' SOURCE POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSPTR<15:0>**: Channel Source Pointer bits

1111111111111111 = Points to byte 65,535 of the source

.

.

.

0000000000000001 = Points to byte 1 of the source

0000000000000000 = Points to byte 0 of the source

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 9-15: DCHxDPTR: DMA CHANNEL 'x' DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDPTR<15:0>**: Channel Destination Pointer bits

1111111111111111 = Points to byte 65,535 of the destination

.

.

.

0000000000000001 = Points to byte 1 of the destination

0000000000000000 = Points to byte 0 of the destination

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 10-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	UTEYE	—	—	USBSIDL	USBSIDL	—	—	UASUSPND

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye-Pattern Test Enable bit

1 = Eye-Pattern Test enabled

0 = Eye-Pattern Test disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 3 **LSDEV:** Low-Speed Device Enable bit

1 = USB module operates in Low-Speed Device mode only

0 = USB module operates in OTG, Host, or Full-Speed Device mode

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit

1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 10-5.

0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock

TABLE 11-6: PORTC REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF88_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	ANSELC3	ANSELC2	ANSELC1	—	000E
6210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
6220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
6230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
6240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
6250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
6260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
6270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6280	CNENC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEC15	CNIEC14	CNIEC13	CNIEC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
6290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATC15	CNSTATC14	CNSTATC13	CNSTATC12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 21-4: RTCDATE: RTC DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	YEAR10<3:0>				YEAR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<3:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **YEAR10<3:0>**: Binary-Coded Decimal Value of Years bits, 10s place digits

bit 27-24 **YEAR01<3:0>**: Binary-Coded Decimal Value of Years bits, 1s place digit

bit 23-20 **MONTH10<3:0>**: Binary-Coded Decimal Value of Months bits, 10s place digits; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>**: Binary-Coded Decimal Value of Months bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>**: Binary-Coded Decimal Value of Days bits, 10s place digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>**: Binary-Coded Decimal Value of Days bits, 1s place digit; contains a value from 0 to 9

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **WDAY01<3:0>**: Binary-Coded Decimal Value of Weekdays bits, 1s place digit; contains a value from 0 to 6

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

TABLE 22-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
9100	ADC1BUF9	31:16	ADC Result Word 9 (ADC1BUF9<31:0>)															0000
		15:0																0000
9110	ADC1BUFA	31:16	ADC Result Word A (ADC1BUFA<31:0>)															0000
		15:0																0000
9120	ADC1BUFB	31:16	ADC Result Word B (ADC1BUFB<31:0>)															0000
		15:0																0000
9130	ADC1BUFC	31:16	ADC Result Word C (ADC1BUFC<31:0>)															0000
		15:0																0000
9140	ADC1BUFD	31:16	ADC Result Word D (ADC1BUFD<31:0>)															0000
		15:0																0000
9150	ADC1BUFE	31:16	ADC Result Word E (ADC1BUFE<31:0>)															0000
		15:0																0000
9160	ADC1BUFF	31:16	ADC Result Word F (ADC1BUFF<31:0>)															0000
		15:0																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for details.
- 2:** For 64-pin devices, the MSB of these bits is not available.
- 3:** For 64-pin devices, only the CSSL30:CSSL0 bits are available.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 22-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL31 ⁽²⁾	CSSL30 ⁽¹⁾	CSSL29 ⁽¹⁾	CSSL28 ⁽¹⁾	CSSL27	CSSL26	CSSL25	CSSL24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL23	CSSL21	CSSL21	CSSL20	CSSL19	CSSL18	CSSL17	CSSL16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CSSL<31:0>**: ADC Input Pin Scan Selection bits

1 = Select ANx for input scan; CSSLx = ANx, where 'x' = 0-31

0 = Skip ANx for input scan; CSSLx = ANx, where 'x' = 0-31

Note 1: For devices with 64 pins, CSSL28 selects IVREF (Band Gap) for scan; CSSL29 selects CTMU temperature diode for scan; and CSSL30 selects CTMU input for scan

2: On devices with less than 32 analog inputs, all CSSLx bits can be selected; however, inputs selected for scan without a corresponding input on the device will convert to VREFL.

REGISTER 22-6: AD1CSSL2: ADC INPUT SCAN SELECT REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	CSSL50 ⁽¹⁾	CSSL49 ⁽¹⁾	CSSL48 ⁽¹⁾
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL47	CSSL46	CSSL45	CSSL44	CSSL43	CSSL42	CSSL41	CSSL40
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL39	CSSL38	CSSL37	CSSL36	CSSL35	CSSL34	CSSL33	CSSL32

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-19 **Unimplemented:** Read as '0'

bit 18-0 **CSSL<50:32>**: ADC Input Pin Scan Selection bits

1 = Select ANx for input scan; CSSLx = ANx, where 'x' = 32-50

0 = Skip ANx for input scan; CSSLx = ANx, where 'x' = 32-50

Note 1: For devices with 100 or more pins, CSSL48 selects IVREF (Band Gap) for scan; CSSL49 selects CTMU temperature diode for scan; and CSSL50 selects CTMU input for scan

Note: The ANx inputs in this register only support devices with 100 or more pins.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 23-2: C1CFG: CAN BAUD RATE CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	WAKFIL	—	—	—	SEG2PH<2:0> ^(1,4)		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEG2PHTS ⁽¹⁾	SAM ⁽²⁾	SEG1PH<2:0>			PRSEG<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SJW<1:0> ⁽³⁾		BRP<5:0>					

Legend:	HC = Hardware Clear	S = Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit
 1 = Use CAN bus line filter for wake-up
 0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as '0'

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits^(1,4)
 111 = Length is 8 x T_Q

•
•
•

000 = Length is 1 x T_Q

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit⁽¹⁾
 1 = Freely programmable
 0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit⁽²⁾
 1 = Bus line is sampled three times at the sample point
 0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits⁽⁴⁾
 111 = Length is 8 x T_Q

•
•
•

000 = Length is 1 x T_Q

- Note 1:** $SEG2PH \leq SEG1PH$. If SEG2PHTS is clear, SEG2PH will be set automatically.
Note 2: 3 Time bit sampling is not allowed for BRP < 2.
Note 3: $SJW \leq SEG2PH$.
Note 4: The Time Quanta per bit must be greater than 7 (that is, T_{QBIT} > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = 100).

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

24.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. “Comparator”** (DS60001110) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

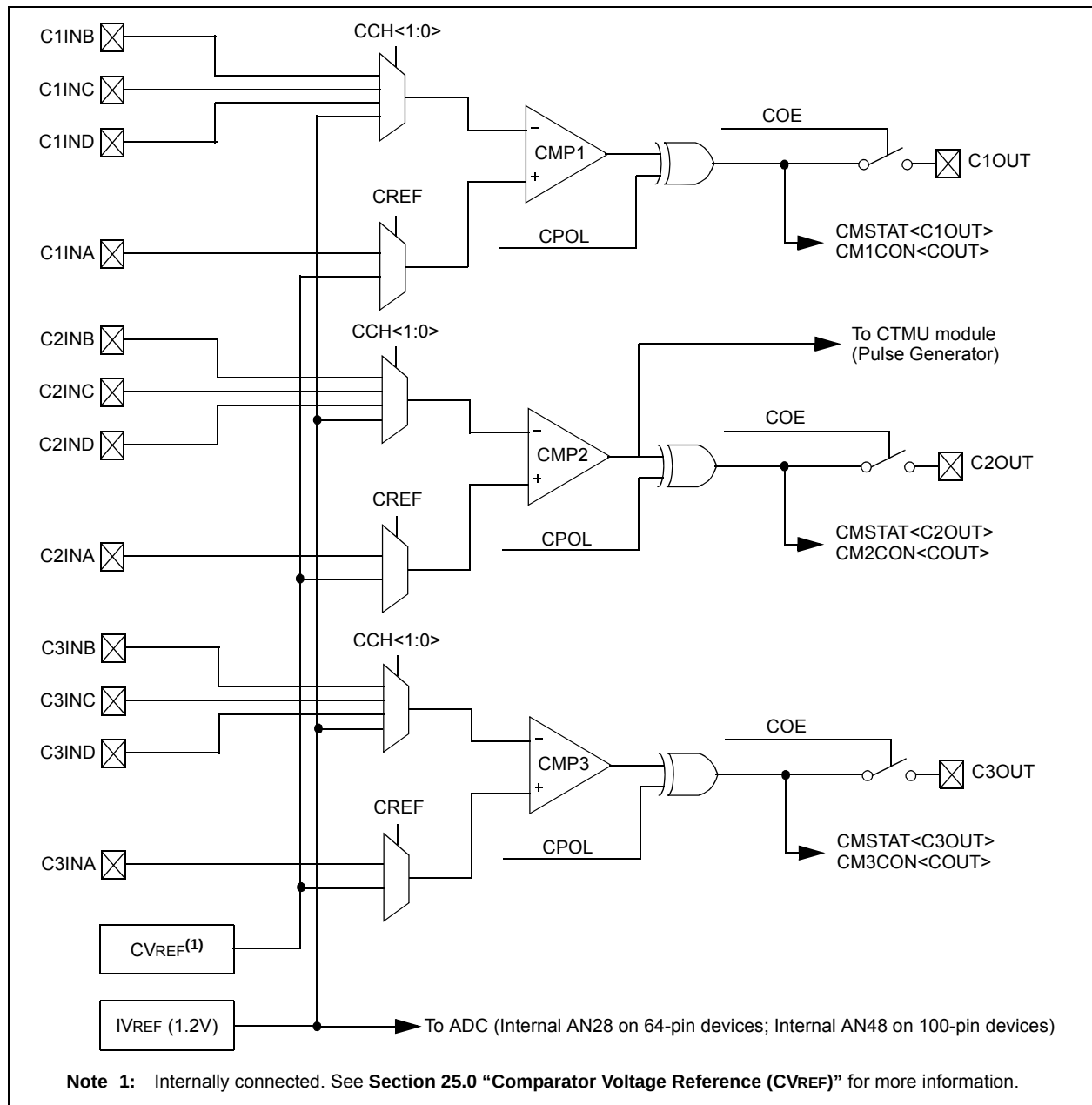
The Analog Comparator module contains three comparators that can be configured in a variety of ways.

The following are the key features of this module:

- Selectable inputs available include:
 - Analog inputs multiplexed with I/O pins
 - On-chip internal absolute voltage reference (IVREF)
 - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the comparator module is provided in Figure 24-1.

FIGURE 24-1: COMPARATOR BLOCK DIAGRAM



PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

26.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 37. “Charge Time Measurement Unit (CTMU)”** (DS60001167) in the “*PIC32 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

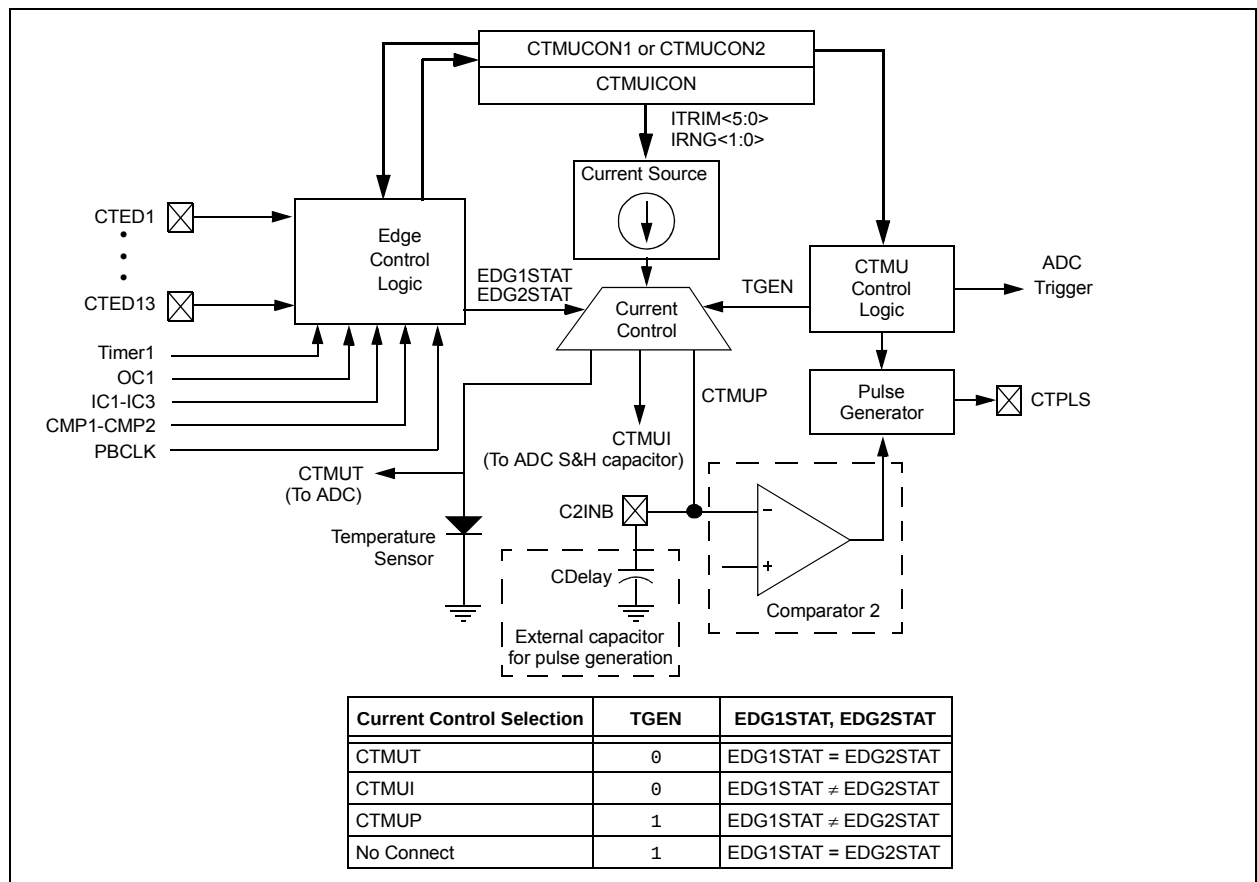
The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.

The CTMU module includes the following key features:

- Up to 13 channels available for capacitive or time measurement input
- On-chip precision current source
- 16-edge input trigger sources
- Selection of edge or level-sensitive inputs
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- Integrated temperature sensing diode
- Control of current source during auto-sampling
- Four current source ranges
- Time measurement resolution of one nanosecond

A block diagram of the CTMU is shown in Figure 26-1.

FIGURE 26-1: CTMU BLOCK DIAGRAM



PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

FIGURE 31-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

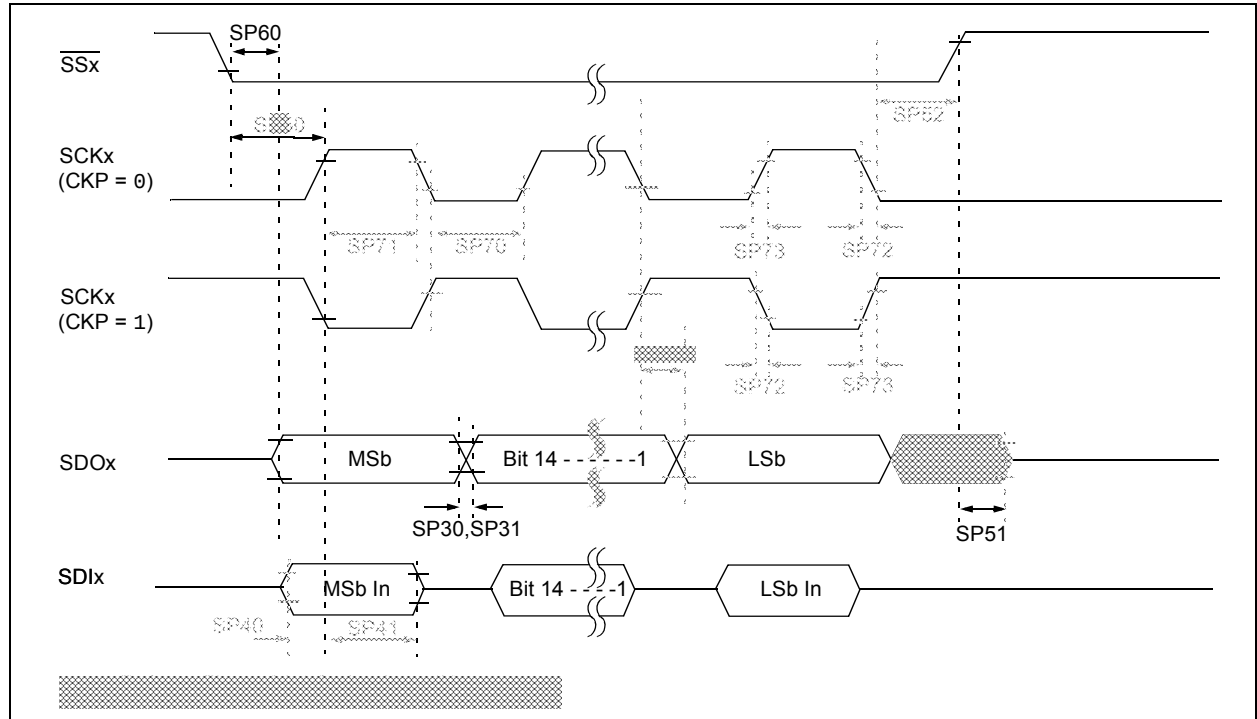


TABLE 31-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time (Note 3)	Tsck/2	—	—	ns	—
SP71	Tsch	SCKx Input High Time (Note 3)	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	5	10	ns	—
SP73	TscR	SCKx Input Rise Time	—	5	10	ns	—
SP30	TdoF	SDOx Data Output Fall Time (Note 4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time (Note 4)	—	—	—	ns	See parameter DO31
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	20	ns	VDD > 2.7V
			—	—	30	ns	VDD < 2.7V
SP40	TdIV2sch, TdIV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP50	Tssl2sch, Tssl2scL	SSx ↓ to SCKx ↓ or SCKx ↑ Input	175	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns.

4: Assumes 50 pF load on all SPIx pins.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

32.1 DC Characteristics

TABLE 32-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts) ⁽¹⁾	Temp. Range (in °C)	Max. Frequency
			PIC32MX1XX/2XX/5XX 64/100-pin Family
MDC5	VBOR-3.6V	-40°C to +85°C	50 MHz

Note 1: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below V_{DDMIN} . Refer to parameter BO10 in Table 31-10 for BOR values.

TABLE 32-2: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial	
Parameter No.	Typical ⁽³⁾	Max.	Units	Conditions
Operating Current (IDD) (Note 1, 2)				
MDC24	25	40	mA	50 MHz

Note 1: A device's I_{DD} supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for I_{DD} measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to Vss
- $MCLR = V_{DD}$
- CPU executing while(1) statement from Flash

3: RTCC and JTAG are disabled

4: Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

DEVCFG0 (Device Configuration Word 0)	293
DEVCFG1 (Device Configuration Word 1)	295
DEVCFG2 (Device Configuration Word 2)	297
DEVCFG3 (Device Configuration Word 3)	299
DEVID (Device and Revision ID)	301
DMAADDR (DMA Address)	91
DMAADDR (DMR Address)	91
DMACON (DMA Controller Control)	90
DMASTAT (DMA Status)	91
I2CxCON (I2C 'x' Control Register ('x' = 1 and 2))	194
I2CxSTAT (I2C Status Register)	196
ICxCON (Input Capture x Control)	175
IFSx (Interrupt Flag Status)	60
INTCON (Interrupt Control)	58
INTSTAT (Interrupt Status)	59
IPCx (Interrupt Priority Control)	61
IPTMR Interrupt Proximity Timer	59
NVMADDR (Flash Address)	66
NVMCON (Programming Control)	65
NVMDATA (Flash Program Data)	67
NVMKEY (Programming Unlock)	66
NVMSRCADDR (Source Data Address)	67
OCxCON (Output Compare x Control)	179
OSCCON (Oscillator Control)	77
PMADDR (Parallel Port Address)	213
PMAEN (Parallel Port Pin Enable)	215
PMCON (Parallel Port Control)	209
PMDIN (Parallel Port Input Data)	214, 219
PMDOUT (Parallel Port Output Data)	214
PMMODE (Parallel Port Mode)	211
PMRADDR (Parallel Port Read Address)	218
PMSTAT (Parallel Port Status (Slave Modes Only))	216
PMWADDR (Parallel Port Write Address)	217
REFOCON (Reference Oscillator Control)	81
REFOTRIM (Reference Oscillator Trim)	83
RPnR (Peripheral Pin Select Output)	157
RSWRST (Software Reset)	72
RTCCON (RTC Control)	223
RTCDATE (RTC Date Value)	228
RTCTIME (RTC Time Value)	227
SPIxCON (SPI Control)	184
SPIxCON2 (SPI Control 2)	187
SPIxSTAT (SPI Status)	188
T1CON (Type A Timer Control)	161
TxCON (Type B Timer Control)	166
U1ADDR (USB Address)	123
U1BDTP1 (USB BDT Page 1)	125
U1BDTP2 (USB BDT Page 2)	126
U1BDTP3 (USB BDT Page 3)	126
U1CNFG1 (USB Configuration 1)	127
U1CON (USB Control)	121
U1EIE (USB Error Interrupt Enable)	119
U1EIR (USB Error Interrupt Status)	117
U1EP0-U1EP15 (USB Endpoint Control)	128
U1FRMH (USB Frame Number High)	124
U1FRML (USB Frame Number Low)	123
U1IE (USB Interrupt Enable)	116
U1IR (USB Interrupt)	115
U1OTGCON (USB OTG Control)	113
U1OTGIE (USB OTG Interrupt Enable)	111
U1OTGIR (USB OTG Interrupt Status)	110
U1OTGSTAT (USB OTG Status)	112
U1PWRC (USB Power Control)	114
U1SOF (USB SOF Threshold)	125
U1STAT (USB Status)	120

U1TOK (USB Token)	124
WDTCON (Watchdog Timer Control)	171
Reset SFR Summary	70
Resets	69
Revision History	375
RTCALRM (RTC ALARM Control)	225

S

Serial Peripheral Interface (SPI)	181
Software Simulator (MPLAB SIM)	307
Special Features	291

T

Timer1 Module	159
Timer2/3, Timer4/5 Modules	163
Timing Diagrams	
10-Bit Analog-to-Digital Conversion (ASAM = 0, SSRC<2:0> = 000)	345
10-Bit Analog-to-Digital Conversion (ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)	346
EJTAG	352
External Clock	321
I/O Characteristics	324
I2Cx Bus Data (Master Mode)	335
I2Cx Bus Data (Slave Mode)	338
I2Cx Bus Start/Stop Bits (Master Mode)	335
I2Cx Bus Start/Stop Bits (Slave Mode)	338
Input Capture (CAPx)	328
OCx/PWM	329
Output Compare (OCx)	329
Parallel Master Port Read	348
Parallel Master Port Write	349
Parallel Slave Port	347
SPIx Master Mode (CKE = 0)	330
SPIx Master Mode (CKE = 1)	331
SPIx Slave Mode (CKE = 0)	332
SPIx Slave Mode (CKE = 1)	333
Timer1, 2, 3, 4, 5 External Clock	327
UART Reception	206
UART Transmission (8-bit or 9-bit Data)	206
Timing Requirements	
CLKO and I/O	324
Timing Specifications	
I2Cx Bus Data Requirements (Master Mode)	336
I2Cx Bus Data Requirements (Slave Mode)	339
Input Capture Requirements	328
Output Compare Requirements	329
Simple OCx/PWM Mode Requirements	329
SPIx Master Mode (CKE = 0) Requirements	330
SPIx Master Mode (CKE = 1) Requirements	331
SPIx Slave Mode (CKE = 1) Requirements	333
SPIx Slave Mode Requirements (CKE = 0)	332
Timing Specifications (50 MHz)	
SPIx Master Mode (CKE = 0) Requirements	356
SPIx Master Mode (CKE = 1) Requirements	356
SPIx Slave Mode (CKE = 1) Requirements	357
SPIx Slave Mode Requirements (CKE = 0)	357

U

UART	199
USB On-The-Go (OTG)	105

V

VCAP pin	302
Voltage Regulator (On-Chip)	302

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

Revision D (April 2016)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-2.

TABLE A-3: MAJOR SECTION UPDATES

Section Name	Update Description
1.0 “Device Overview”	Removed the USBOEN pin and all trace-related pins from the Pinout I/O Descriptions (see Table 1-1).
2.0 “Guidelines for Getting Started with 32-bit MCUs”	Section 2.7 “Trace” was removed. Section 2.10 “Sosc Design Recommendation” was removed.
3.0 “CPU”	References to the Shadow Register Set (SRS), which is not supported by PIC32MX1XX/2XX/5XX 64/100-pin Family devices, were removed from 3.1 “Features” , 3.2.1 “Execution Unit” , and Coprocessor 0 Registers (Table 3-2).
4.0 “Memory Organization”	The SFR Memory Map was added (see Table 4-1).
5.0 “Interrupt Controller”	The Single Vector Shadow Register Set (SSO) bit (INTCON<16>) was removed (see Register 5-1).
10.0 “USB On-The-Go (OTG)”	The UOEMON bit (U1CNFG1<6>) was removed (see Register 10-20).
23.0 “Controller Area Network (CAN)”	The CAN features (number of messages and FIFOs) were updated. The PIC32 CAN Block Diagram was updated (see Figure 23-1). The following registers were updated: • C1FSTAT (see Register 23-6) • C1RXOVF (see Register 23-7) • C1RXFn (see Register 23-14) • C1FIFOCONn (see Register 23-16) • C1FIFOINTn (see Register 23-17) • C1FIFOUAn (see Register 23-18) • C1FIFOCIn (see Register 23-19) The C1FLTCON4 through C1FLTCON7 registers were removed.
28.0 “Special Features”	The virtual addresses for the Device Configuration Word registers were updated (see Table 28-1).
31.0 “40 MHz Electrical Characteristics”	The EJTAG Timing Characteristics diagram was updated (see Figure 31-23).