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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx130f128lt-v-pt

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1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32). This document contains device-specific information for PIC32MX1XX/2XX/5XX 64/100-pin devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX/ 5XX 64/100-pin family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: PIC32MX1XX/2XX/5XX 64/100-PIN BLOCK DIAGRAM



	Pin N	umber			
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	Pin Type	Buffer Type	Description
AN0	16	25	I	Analog	
AN1	15	24	Ι	Analog	
AN2	14	23	Ι	Analog	
AN3	13	22	I	Analog	
AN4	12	21	I	Analog	
AN5	11	20	Ι	Analog	
AN6	17	26	I	Analog	
AN7	18	27	I	Analog	
AN8	21	32	Ι	Analog	
AN9	22	33	Ι	Analog	
AN10	23	34	Ι	Analog	
AN11	24	35	I	Analog	
AN12	27	41	Ι	Analog	
AN13	28	42	I	Analog	
AN14	29	43	I	Analog	
AN15	30	44	I	Analog	
AN16	4	10	I	Analog	
AN17	5	11	I	Analog	
AN18	6	12	I	Analog	
AN19	8	14	Ι	Analog	
AN20	62	98	I	Analog	
AN21	64	100	I	Analog	
AN22	1	3	Ι	Analog	
AN23	2	4	Ι	Analog	
AN24	49	76	Ι	Analog	
AN25	50	77	Ι	Analog	
AN26	51	78	Ι	Analog	
AN27	3	5	Ι	Analog	
AN28	—	1	Ι	Analog	
AN29	—	6	Ι	Analog	
AN30	—	7	Ι	Analog	
AN31		8	Ι	Analog	
AN32		18	Ι	Analog	
AN33	_	19	I	Analog	
AN34	_	39	I	Analog	
AN35	_	40	I	Analog	
Legend:	CMOS = CN	IOS compat	ible inpu	it or output	Analog = Analog input I = Input O = Output

TABLE 1-1:PINOUT I/O DESCRIPTIONS

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUS

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2.1 Basic Connection Requirements

Getting started with the PIC32MX1XX/2XX/5XX 64/ 100-pin family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins (see 2.2 "Decoupling Capacitors")
- All AVDD and AVss pins, even if the ADC module is not used (see 2.2 "Decoupling Capacitors")
- VCAP pin (see 2.3 "Capacitor on Internal Voltage Regulator (VCAP)")
- MCLR pin (see 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins, used for In-Circuit Serial Programming (ICSP[™]) and debugging purposes (see **2.5** "ICSP Pins")
- OSC1 and OSC2 pins, when external oscillator source is used (see 2.7 "External Oscillator Pins")

The following pins may be required:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A value of $0.1 \ \mu F$ (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high frequency noise: If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μ F in parallel with 0.001 μ F.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

Without proper signal isolation, on non-5V tolerant pins, the remote signal can power the PIC32 device through the high side ESD protection diodes. Besides violating the absolute maximum rating specification when VDD of the PIC32 device is restored and ramping up or ramping down, it can also negatively affect the internal Power-on Reset (POR) and Brown-out Reset (BOR) circuits, which can lead to improper initialization of internal PIC32 logic circuits. In these cases, it is recommended to implement digital or analog signal isolation as depicted in Figure 2-6, as appropriate. This is indicative of all industry microcontrollers and not just Microchip products.

TABLE 2-1: EXAMPLES OF DIGITAL/ ANALOG ISOLATORS WITH OPTIONAL LEVEL TRANSLATION

Example Digital/Analog Signal Isolation Circuits	Inductive Coupling	Capacitive Coupling	Opto Coupling	Analog/Digital Switch
ADuM7241 / 40 ARZ (1 Mbps)	Х			
ADuM7241 / 40 CRZ (25 Mbps)	Х			
ISO721		Х		
LTV-829S (2 Channel)			Х	
LTV-849S (4 Channel)			Х	
FSA266 / NC7WB66	_		_	Х

FIGURE 2-6: DIGITAL/ANALOG SIGNAL ISOLATION CIRCUITS



TABLE 5-2: INTERRUPT REGISTER MAP (CONTINUED)

ess			Bits																
Virtual Addr (BF88_#)	Register Name ⁽³⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1050	IDC5	31:16	_	—		A	01IP<2:0>		AD1IS	i<1:0>	_	—	_		OC5IP<2:0>	>	OC5IS	i<1:0>	0000
IUEU	IFC5	15:0	_	_	_	IC	5IP<2:0>		IC5IS	<1:0>	_	_			T5IP<2:0>		T5IS∙	<1:0>	0000
10E0	IPC6	31:16		_		CM	P1IP<2:0>		CMP1	S<1:0>	_	_			FCEIP<2:0>	•	FCEIS	<1:0>	0000
101.0	11 00	15:0		_		RT	RTCCIP<2:0>		RTCCI	S<1:0>	_	-		FSCMIP<2:0>			FSCM	S<1:0>	0000
1100	IPC7	31:16	_	—	_	U1IP<2:0>		U1IS	<1:0>	—	—	_	SPI1IP<2:0>		SPI1IS	S<1:0>	0000		
1100	11 07	15:0	—	_	_	USI	USBIP<2:0> ⁽²⁾		USBIS<	<1:0> ⁽²⁾	—	—	-	CMP2IP<2:0>		CMP2I	S<1:0>	0000	
1110	IPC8	31:16	-	—	-	SF	12IP<2:0>		SPI2IS	S<1:0>	—	—	-	PMPIP<2:0>		PMPIS	S<1:0>	0000	
1110	11 00	15:0	—	—	—	С	NIP<2:0>		CNIS	<1:0>	—	—	_	I2C1IP<2:0>		12C115	5<1:0>	0000	
1120	IPC9	31:16	-	—	-	U	4IP<2:0>		U4IS-	<1:0>	—	—	-	U3IP<2:0>		U3IS•	<1:0>	0000	
1120	11 00	15:0	—	—	—	120	C2IP<2:0>		12C2I5	S<1:0>	—	—	_		U2IP<2:0>		U2IS·	<1:0>	0000
1130	IPC10	31:16	—	—	—	DM	A1IP<2:0>		DMA1	S<1:0>	—	—	_		DMA0IP<2:0	>	DMA0I	S<1:0>	0000
1100	11 010	15:0	_	—	_	CTI	MUIP<2:0>	•	CTMUI	S<1:0>	—	—	_		U5IP<2:0>		U5IS•	<1:0>	0000
11/10		31:16	-	—	-	CAI	VIP<2:0> ⁽⁵⁾		CANIS	<1:0> (5)	—	—	-		CMP3IP<2:0	>	CMP3I	S<1:0>	0000
11-0		15:0	-	—	-	DM	A3IP<2:0>	•	DMA3IS<1:0> — — DMA2IP<2:0>		DMA2I	S<1:0>	0000						
1150	IPC12	31:16	—	—	_		_	—	—	_	_	—	_	_	—	—	—		0000
1130	11 012	15:0	_	_	_	SPI	4P<2:0>(1))	SPI4S<	:1:0>(1)	_	_	-		SPI3P<2:0>	•	SPI3S	<1:0>	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This bit is only available on 100-pin devices.

2: This bit is only implemented on devices with a USB module.

3: With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

4: This register does not have associated CLR, SET, and INV registers.

5: This bit is only implemented on devices with a CAN module.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
31:24	NVMKEY<31:24>										
00.40	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
23:10	NVMKEY<23:16>										
15.0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
15:8	NVMKEY<15:8>										
7.0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
7:0				NVMK	EY<7:0>						

REGISTER 6-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMKEY<31:0>:** Unlock Register bits These bits are write-only, and read as '0' on any read.

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

REGISTER 6-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	NVMADDR<31:24>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23.10	NVMADDR<23:16>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	NVMADDR<15:8>										
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
				NVMA	DDR<7:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMADDR<31:0>: Flash Address bits Bulk/Chip/PFM Erase: Address is ignored Page Erase: Address identifies the page to erase Row Program: Address identifies the row to program Word Program: Address identifies the word to program

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	—	—	—	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	—	—	—	—	—	—		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	CHSSIZ<15:8>									
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7.0				CHSSIZ	<7:0>					

REGISTER 9-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSSIZ<15:0>: Channel Source Size bits

1111111111111111 = 65,535 byte source size

REGISTER 9-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	—	—	—	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:10	—	—	—	—	—	—	—	—		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	CHDSIZ<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				CHDSIZ	<u>/</u> <7:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

REGISTER 10-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—		—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—		—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	_	—		_	—	_	_	—
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	STALLE				TDNIE	SOEIE		URSTIE ⁽²⁾
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE		JULIE		DETACHIE ⁽³⁾
1	1	1				1		

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7	STALLIE: STALL Handshake Interrupt Enable bit
	1 = STALL interrupt enabled
	0 = STALL interrupt disabled

bit 6 **ATTACHIE:** ATTACH Interrupt Enable bit 1 = ATTACH interrupt enabled

0 = ATTACH interrupt disabled

bit 5 **RESUMEIE:** RESUME Interrupt Enable bit

- 1 = RESUME interrupt enabled
- 0 = RESUME interrupt disabled
- bit 4 IDLEIE: Idle Detect Interrupt Enable bit
 - 1 = Idle interrupt enabled
 - 0 = Idle interrupt disabled
- bit 3 TRNIE: Token Processing Complete Interrupt Enable bit
 - 1 = TRNIF interrupt enabled
 - 0 = TRNIF interrupt disabled
- bit 2 SOFIE: SOF Token Interrupt Enable bit
 - 1 = SOFIF interrupt enabled
 - 0 = SOFIF interrupt disabled
- bit 1 UERRIE: USB Error Interrupt Enable bit⁽¹⁾
 - 1 = USB Error interrupt enabled
 - 0 = USB Error interrupt disabled
- bit 0 **URSTIE:** USB Reset Interrupt Enable bit⁽²⁾
 - 1 = URSTIF interrupt enabled
 - 0 = URSTIF interrupt disabled
 - DETACHIE: USB Detach Interrupt Enable bit⁽³⁾
 - 1 = DATTCHIF interrupt enabled
 - 0 = DATTCHIF interrupt disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.

- 2: Device mode.
- 3: Host mode.

REGISTER 10-10: U1STAT: USB STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—		—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—		—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—		—	—	—	—	—
7.0	R-x	R-x	R-x	R-x	R-x	R-x	U-0	U-0
7:0		ENDP.	T<3:0>		DIR	PPBI	_	_

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits (Represents the number of the BDT, updated by the last USB transfer.)
 - 1111 = Endpoint 15 1110 = Endpoint 14 . . 0001 = Endpoint 1 0000 = Endpoint 0
- bit 3 **DIR:** Last BD Direction Indicator bit
 - 1 = Last transaction was a transmit transfer (TX)
 - 0 = Last transaction was a receive transfer (RX)
- bit 2 **PPBI:** Ping-Pong BD Pointer Indicator bit
 - 1 = The last transaction was to the ODD BD bank
 - 0 = The last transaction was to the EVEN BD bank
- bit 1-0 Unimplemented: Read as '0'

Note: The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. U1STAT value is only valid when the TRNIF bit (U1IR<3>) is active. Clearing the TRNIF bit advances the FIFO. Data in register is invalid when the TRNIF bit = 0.

TABLE 11-1: INPUT PIN SELECTION

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[<i>pin name</i>]R Value to RPn Pin Selection
INT3	INT3R	INT3R<3:0>	0000 = RPD2
T2CK	T2CKR	T2CKR<3:0>	0010 = RPF4
IC3	IC3R	IC3R<3:0>	
U1RX	U1RXR	U1RXR<3:0>	0101 = RPB9 0110 = RPB10
U2RX	U2RXR	U2RXR<3:0>	0111 = RPC14
U5CTS ⁽³⁾	U5CTSR	U5CTSR<3:0>	1000 = Rr B30 = 10000 = 10000 = 10000 = 100000 = 100000 = 100000 = 100000 = 100000 = 100000 = 100000000
SDI3	SDI3R	SDI3R<3:0>	$= 1010 = \text{RPC1}^{(3)}$ $1011 = \text{RPD14}^{(3)}$
SDI4 ⁽³⁾	SDI4R	SDI4R<3:0>	
REFCLKI	REFCLKIR	REFCLKIR<3:0>	1110 = Reserved 1111 = RPF2 ⁽¹⁾
INT4	INT4R	INT4R<3:0>	0000 = RPD3
T5CK	T5CKR	T5CKR<3:0>	0010 = RPF5
IC4	IC4R	IC4R<3:0>	0100 = RPF0 0101 = PPB1
U3RX	U3RXR	U3RXR<3:0>	0110 = RPE5
U4CTS	U4CTSR	U4CTSR<3:0>	$\frac{1000 = \text{RPB3}}{1001 = \text{PPE12}(3)}$
SDI1	SDI1R	SDI1R<3:0>	$\frac{1001 - RP12^{(3)}}{1010 = RPC4^{(3)}}$
SDI2	SDI2R	SDI2R<3:0>	$\frac{10011 - \text{RPD}(3)}{1100 = \text{RPG}(3)}$
C1RX ⁽⁵⁾	C1RXR ⁽⁵⁾	C1RXR<3:0> ⁽⁵⁾	$\frac{1101 - RPF2^{(1)}}{1110 = RPF2^{(2)}}$
INT2	INT2R	INT2R<3:0>	0000 = RPD9
T4CK	T4CKR	T4CKR<3:0>	0001 = RPG6 0010 = RPB8
IC2	IC2R	IC2R<3:0>	
IC5	IC5R	IC5R<3:0>	0101 = RPB0 0110 = RPF3
U1CTS	U1CTSR	U1CTSR<3:0>	0111 = RPB7
U2CTS	U2CTSR	U2CTSR<3:0>	1000 = Reserved $1001 = \text{RPF12}^{(3)}$
SS1	SS1R	SS1R<3:0>	1010 = RPD12 ⁽³⁾ 1011 = RPF8 ⁽³⁾
SS3	SS3R	SS1R<3:0>	1100 = RPC3 ⁽³⁾ 1101 = RPE9 ⁽³⁾
<u> </u>	SS3R	SS3R<3:0>	1110 = RPD14 ⁽³⁾ 1111 = RPB2

Note 1: This selection is not available on 64-pin USB devices.

2: This selection is only available on 100-pin General Purpose devices.

3: This selection is not available on 64-pin devices.

4: This selection is not available when USBID functionality is used on USB devices.

5: This selection is not available on devices without a CAN module.

6: This selection is not available on USB devices.

7: This selection is not available when VBUSON functionality is used on USB devices.

REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 4 DISSDI: Disable SDI bit
 - 1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
 - 0 = SDI pin is controlled by the SPI module
- bit 3-2 STXISEL<1:0>: SPI Transmit Buffer Empty Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
 - 10 = Interrupt is generated when the buffer is empty by one-half or more
 - 01 = Interrupt is generated when the buffer is completely empty
 - 00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete
- bit 1-0 SRXISEL<1:0>: SPI Receive Buffer Full Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is full
 - 10 = Interrupt is generated when the buffer is full by one-half or more
 - 01 = Interrupt is generated when the buffer is not empty
 - 00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)
- **Note 1:** When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - **2:** This bit can only be written when the ON bit = 0.
 - **3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
 - 4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31.24	—	—	—	—	—	—	—	—		
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:10	_	—	_	_	—	_	_	_		
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	CS2 ⁽¹⁾	CS1 ⁽³⁾		ADDR<13:8>						
	ADDR15 ⁽²⁾	ADDR14 ⁽⁴⁾								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				ADDR<	7:0>					

REGISTER 20-3: PMADDR: PARALLEL PORT ADDRESS REGISTER

Legend:

3						
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-16 **Unimplemented:** Read as '0'

- bit 15 CS2: Chip Select 2 bit⁽¹⁾
 - 1 = Chip Select 2 is active
 - 0 = Chip Select 2 is inactive
- bit 15 ADDR<15>: Target Address bit 15⁽²⁾
- bit 14 CS1: Chip Select 1 bit⁽³⁾
 - 1 = Chip Select 1 is active
 - 0 = Chip Select 1 is inactive
- bit 14 ADDR<14>: Target Address bit 14⁽⁴⁾
- bit 13-0 ADDR<13:0>: Address bits
- **Note 1:** When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
 - **2:** When the CSF<1:0> bits (PMCON<7:6>) = 00.
 - **3:** When the CSF<1:0> bits (PMCON<7:6>) = 10.
 - **4:** When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

Note: If the DUALBUF bit (PMCON<17>) = 0, the bits in this register control both read and write target addressing. If the DUALBUF bit = 1, the bits in this register are not used. In this instance, use the PMRADDR register for Read operations and the PMWADDR register for Write operations.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0						
31.24	—	—	—	—	—	—	—	—
22.16	U-0	U-0						
23.10	—	—	—	—	—	—	—	—
15.0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
10.0	ON ⁽¹⁾	—	SIDL	—	—	FORM<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
7:0	SSRC<2:0>			CLRASAM		ASAM	SAMP ⁽²⁾	DONE ⁽³⁾

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1

Legend:

bit 14

R = Readable bit	W = Writable bit	U = Unimplemented bit, re-	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** ADC Operating Mode bit⁽¹⁾
 - 1 = ADC module is operating
 - 0 = ADC module is not operating
 - Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation in Idle mode
- bit 12-11 Unimplemented: Read as '0'
- bit 10-8 **FORM<2:0>:** Data Output Format bits
 - 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
 - 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)

 - 000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
 - 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000)
 - 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000)
 - 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss dddd dddd)
 - 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 SSRC<2:0>: Conversion Trigger Source Select bits

- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing SAMP bit ends sampling and starts conversion
- **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ 0, this bit is automatically cleared by hardware to end sampling and start conversion.
 - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

REGISTER 23-11: C1FLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED) bit 20-16 FSEL6<4:0>: FIFO Selection bits 11111 = Reserved 10000 = Reserved 01111 = Message matching filter is stored in FIFO buffer 15 00000 = Message matching filter is stored in FIFO buffer 0 FLTEN5: Filter 17 Enable bit bit 15 1 = Filter is enabled 0 = Filter is disabled bit 14-13 MSEL5<1:0>: Filter 5 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected bit 12-8 FSEL5<4:0>: FIFO Selection bits 11111 = Reserved 10000 = Reserved 01111 = Message matching filter is stored in FIFO buffer 15 00000 = Message matching filter is stored in FIFO buffer 0 bit 7 FLTEN4: Filter 4 Enable bit 1 = Filter is enabled 0 = Filter is disabled bit 6-5 MSEL4<1:0>: Filter 4 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected FSEL4<4:0>: FIFO Selection bits bit 4-0 11111 = Reserved 10000 = Reserved 01111 = Message matching filter is stored in FIFO buffer 15 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTE	R 26-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)
bit 10	EDGSEQEN: Edge Sequence Enable bit
	1 = Edge 1 must occur before Edge 2 can occur
	0 = No edge sequence is needed
bit 9	IDISSEN: Analog Current Source Control bit ⁽²⁾
	1 = Analog current source output is grounded
	0 = Analog current source output is not grounded
bit 8	CTTRIG: Trigger Control bit
	1 = Trigger output is enabled
	0 = Trigger output is disabled
bit 7-2	ITRIM<5:0>: Current Source Trim bits
	011111 = Maximum positive change from nominal current
	011110
	•
	000001 = Minimum positive change from nominal current
	000000 = Nominal current output specified by IRNG<1:0>
	111111 = Minimum negative change from nominal current
	•
	100010
	100001 = Maximum negative change from nominal current
bit 1-0	IRNG<1:0>: Current Range Select bits ⁽³⁾
	11 = 100 times base current
	10 = 10 times base current
	01 = Base current level
	00 = 1000 times base current ⁽⁴⁾

- Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
 - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
 - 3: Refer to the CTMU Current Source Specifications (Table 31-41) in Section 31.0 "40 MHz Electrical Characteristics" for current values.
 - 4: This bit setting is not available for the CTMU temperature diode.

29.0 INSTRUCTION SET

The PIC32MX1XX/2XX/5XX 64/100-pin family instruction set complies with the MIPS32[®] Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- · Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note: Refer to *"MIPS32[®] Architecture for Programmers Volume II: The MIPS32[®] Instruction Set"* at www.imgtec.com for more information.

DC CHA		STICS	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Comments
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time.		_	10	μs	See Note 1
D313	DACREFH	CVREF Input Voltage Reference Range	AVss	_	AVDD	V	CVRSRC with CVRSS = 0
			VREF-		VREF+	V	CVRSRC with CVRSS = 1
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size
			0.25 x DACREFH	—	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/ 32 step size
D315	DACRES	Resolution	—	—	DACREFH/24		CVRCON <cvrr> = 1</cvrr>
			—	—	DACREFH/32		CVRCON <cvrr> = 0</cvrr>
D316	DACACC	Absolute Accuracy ⁽²⁾	—	—	1/4	LSB	DACREFH/24, CVRCON <cvrr> = 1</cvrr>
			_	_	1/2	LSB	DACREFH/32, CVRCON <cvrr> = 0</cvrr>

TABLE 31-14: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

TABLE 31-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D321	Cefc	External Filter Capacitor Value	8	10	_	μF	Capacitor must be low series resistance (\leq 3 ohm). Typical voltage on the VCAP pin is 1.8V.





TABLE 31-29: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHA		$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time (Note 3)	Tsck/2	_		ns	—
SP11	TscH	SCKx Output High Time (Note 3)	Tsck/2	—	_	ns	—
SP20	TscF	SCKx Output Fall Time (Note 4)		—	_	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time (Note 4)		_		ns	See parameter DO31
SP30	TDOF	SDOx Data Output Fall Time (Note 4)		_		ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	_	—		ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
				—	20	ns	VDD < 2.7V
SP36	TDOV2SC, TDOV2SCL	SDOx Data Output Setup to First SCKx Edge	15	_		ns	
SP40	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	15	—		ns	VDD > 2.7V
			20	—	_	ns	VDD < 2.7V
SP41	TscH2DIL, TscL2DIL	Hold Time of SDIx Data Input to SCKx Edge	15	—	_	ns	VDD > 2.7V
			20	—	_	ns	VDD < 2.7V

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 31-20: PARALLEL SLAVE PORT TIMING



TABLE 31-41: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 3):2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$									
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions					
CTMU CURRENT SOURCE												
CTMUI1	IOUT1	Base Range ⁽¹⁾	_	0.55		μA	CTMUCON<9:8> = 01					
CTMUI2	IOUT2	10x Range ⁽¹⁾	—	5.5	_	μA	CTMUCON<9:8> = 10					
CTMUI3	Ιουτ3	100x Range ⁽¹⁾	_	55		μA	CTMUCON<9:8> = 11					
CTMUI4	IOUT4	1000x Range ⁽¹⁾	—	550	_	μA	CTMUCON<9:8> = 00					
CTMUFV1	VF	Temperature Diode Forward Voltage ^(1,2)	_	0.598	_	V	TA = +25°C, CTMUCON<9:8> = 01					
			_	0.658	_	V	TA = +25°C, CTMUCON<9:8> = 10					
			_	0.721	_	V	TA = +25°C, CTMUCON<9:8> = 11					
CTMUFV2	Vfvr	Temperature Diode Rate of Change ^(1,2)	—	-1.92	_	mV/ºC	CTMUCON<9:8> = 01					
			—	-1.74	_	mV/ºC	CTMUCON<9:8> = 10					
			_	-1.56		mV/ºC	CTMUCON<9:8> = 11					

Note 1: Nominal value at center point of current trim range (CTMUCON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksps
- All PMD bits are cleared (PMDx = 0)
- Executing a while(1) statement
- Device operating from the FRC with no PLL
- **3:** The CTMU module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.