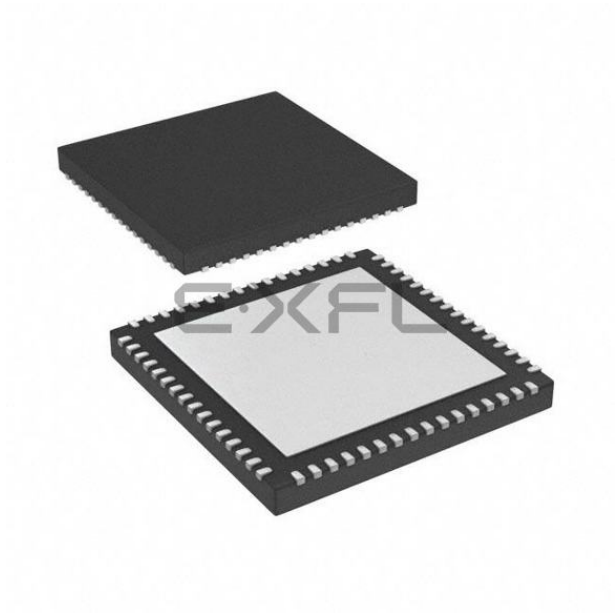

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Applications of "Embedded - Microcontrollers"

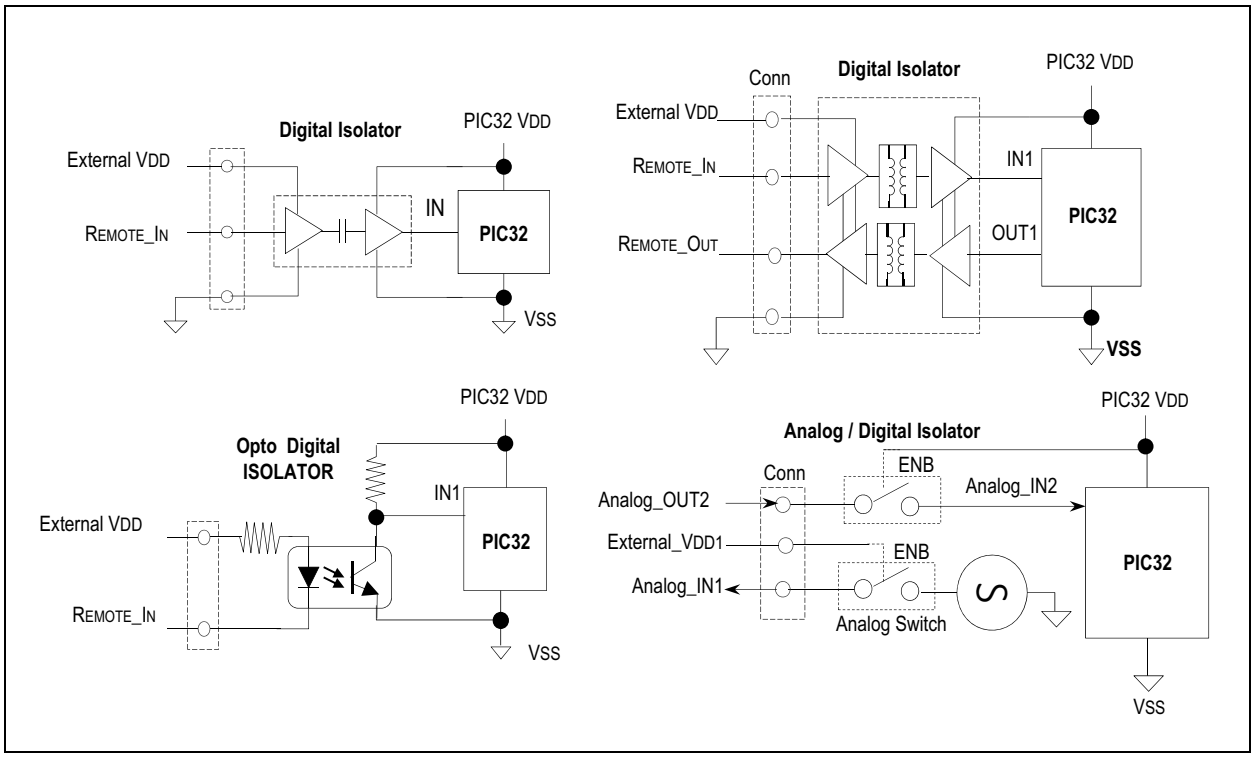
Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx150f256h-50i-mr

Without proper signal isolation, on non-5V tolerant pins, the remote signal can power the PIC32 device through the high side ESD protection diodes. Besides violating the absolute maximum rating specification when VDD of the PIC32 device is restored and ramping up or ramping down, it can also negatively affect the internal Power-on Reset (POR) and Brown-out Reset (BOR) circuits, which can lead to improper initialization of internal PIC32 logic circuits. In these cases, it is recommended to implement digital or analog signal isolation as depicted in Figure 2-6, as appropriate. This is indicative of all industry microcontrollers and not just Microchip products.

TABLE 2-1: EXAMPLES OF DIGITAL/ ANALOG ISOLATORS WITH OPTIONAL LEVEL TRANSLATION

Example Digital/Analog Signal Isolation Circuits	Inductive Coupling	Capacitive Coupling	Opto Coupling	Analog/Digital Switch
ADuM7241 / 40 ARZ (1 Mbps)	X	—	—	—
ADuM7241 / 40 CRZ (25 Mbps)	X	—	—	—
ISO721	—	X	—	—
LTV-829S (2 Channel)	—	—	X	—
LTV-849S (4 Channel)	—	—	X	—
FSA266 / NC7WB66	—	—	—	X

FIGURE 2-6: DIGITAL/ANALOG SIGNAL ISOLATION CIRCUITS



5.1 Interrupts Control Registers

TABLE 5-2: INTERRUPT REGISTER MAP

Virtual Address (BF88_#)	Register Name(3)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	FCEIF	RTCCIF	FSCMIF	AD1IF	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
		15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	U3RXIF	U3EIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	SPI2RXIF	SPI2EIF	PMPEIF	PMPIF	CNGIF	CNFIF	CNEIF	0000
		15:0	CNDIF	CNCIF	CNBIF	CNAIF	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1TXIF	SPI1RXIF	SPI1EIF	USBIF(2)	CMP2IF	CMP1IF	0000
1050	IFS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SPI4TXIF(1)	SPI4RXIF(1)	SPI4EIF(1)	SPI3TXIF	0000
		15:0	SPI3RXIF	SPI3EIF	CANIF	CMP3IF	DMA3IF	DMA2IF	DMA1IF	DMA0IF	CTMUIF	U5TXIF(1)	U5RXIF(1)	U5EIF(1)	U4TXIF	U4RXIF	U4EIF	U3TXIF	0000
1060	IEC0	31:16	FCEIE	RTCCIE	FSCMIE	AD1IE	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
		15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	U3RXIE	U3EIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2TXIE	SPI2RXIE	SPI2EIE	PMPEIE	PMPIE	CNGIE	CNFIE	CNEIE	0000
		15:0	CNDIE	CNCIE	CNBIE	CNAIE	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1TXIE	SPI1RXIE	SPI1EIE	USBIE(2)	CMP2IE	CMP1IE	0000
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE	CTMUIE	U5TXIE(1)	U5RXIE(1)	U5EIE(1)	U4TXIE	U4RXIE	U4EIE	U3TXIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This bit is only available on 100-pin devices.

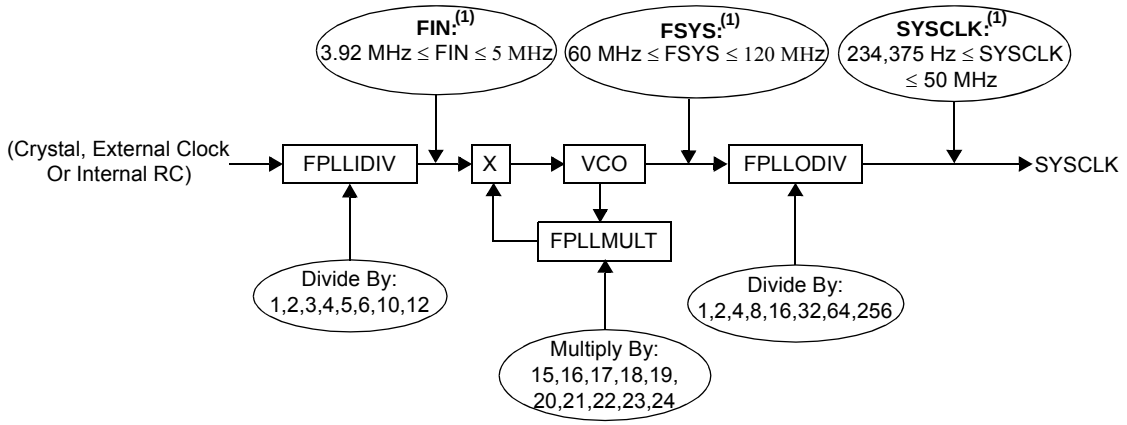
2: This bit is only implemented on devices with a USB module.

3: With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

4: This register does not have associated CLR, SET, and INV registers.

5: This bit is only implemented on devices with a CAN module.

FIGURE 8-2: PIC32MX1XX/2XX/5XX PLL BLOCK DIAGRAM



Note 1: This frequency range must be satisfied at all times if the PLL is enabled and software is updating the corresponding bits in the OSCON register.

10.1 Control Registers

TABLE 10-1: USB REGISTER MAP

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5040	U1OTGIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
5050	U1OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
5060	U1OTGSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
5070	U1OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND(4)	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR	0000
5200	U1IR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF	0000
																		DETACHIF	0000
5210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000
																		DETACHIE	0000
5220	U1EIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	0000
																	EOFEF		0000
5230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE	0000
																	EOFEE		0000
5240	U1STAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0>				DIR	PPBI	—	—	0000
5250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE	SE0	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN	0000
													TOKBUSY					SOFEN	0000
5260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
5270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<15:9>							—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

TABLE 11-2: OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD2	RPD2R	RPD2R<3:0>	0000 = No Connect 0001 = U3TX 0010 = U4RTS 0011 = Reserved 0100 = Reserved 0101 = Reserved 0110 = SDO2 0111 = Reserved 1000 = Reserved 1001 = Reserved 1010 = Reserved 1011 = OC3 1100 = C1TX(5) 1101 = C2OUT 1110 = SDO3 1111 = SDO4(3)
RPG8	RPG8R	RPG8R<3:0>	
RPF4	RPF4R	RPF4R<3:0>	
RPD10	RPD10R	RPD10R<3:0>	
RPF1	RPF1R	RPF1R<3:0>	
RPB9	RPB9R	RPB9R<3:0>	
RPB10	RPB10R	RPB10R<3:0>	
RPC14	RPC14R	RPC14R<3:0>	
RPB5(7)	RPB5R	RPB5R<3:0>	
RPC1(3)	RPC1R	RPC1R<3:0>	
RPD14(3)	RPD14R	RPD14R<3:0>	
RPG1(3)	RPG1R	RPG1R<3:0>	
RPA14(3)	RPA14R	RPA14R<3:0>	
RPD3	RPD3R	RPD3R<3:0>	0000 = No Connect 0001 = U2TX 0010 = Reserved 0011 = U1TX 0100 = U5RTS(3) 0101 = Reserved 0110 = SDO2 0111 = Reserved 1000 = SDO1 1001 = Reserved 1010 = Reserved 1011 = OC4 1100 = Reserved 1101 = C3OUT 1110 = SDO3 1111 = SDO4(3)
RPG7	RPG7R	RPG7R<3:0>	
RPF5	RPF5R	RPF5R<3:0>	
RPD11	RPD11R	RPD11R<3:0>	
RPF0	RPF0R	RPF0R<3:0>	
RPB1	RPB1R	RPB1R<3:0>	
RPE5	RPE5R	RPE5R<3:0>	
RPC13	RPC13R	RPC13R<3:0>	
RPB3	RPB3R	RPB3R<3:0>	
RPF3(4)	RPF3R	RPF3R<3:0>	
RPC4(3)	RPC4R	RPC4R<3:0>	
RPD15(3)	RPD15R	RPD15R<3:0>	
RPG0(3)	RPG0R	RPG0R<3:0>	
RPA15(3)	RPA15R	RPA15R<3:0>	

Note 1: This selection is not available on 64-pin USB devices.

2: This selection is only available on 100-pin General Purpose devices.

3: This selection is not available on 64-pin devices.

4: This selection is not available when USBID functionality is used on USB devices.

5: This selection is not available on devices without a CAN module.

6: This selection is not available on USB devices.

7: This selection is not available when VBUSON functionality is used on USB devices.

REGISTER 13-1: TxCON: TYPE B TIMER 'x' CONTROL REGISTER (CONTINUED)('x' = 2 THROUGH 5)

bit 3 **T32:** 32-Bit Timer Mode Select bit(2)
1 = Odd numbered and even numbered timers form a 32-bit timer
0 = Odd numbered and even numbered timers form a separate 16-bit timer

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(3)
1 = External clock from TxCK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit is available only on even numbered timers (Timer2 and Timer4).

3: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3 and Timer5). All timer functions are set through the even numbered timers.

4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0
	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend:	C = Clearable bit	HS = Set in hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR:** SPI Frame Error status bit
1 = Frame error detected
0 = No Frame error detected
This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY:** SPI Activity Status bit
1 = SPI peripheral is currently busy with some transactions
0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** Transmit Under Run bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or writing a '0' to SPITUR.

bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
1 = When SPI module shift register is empty
0 = When SPI module shift register is not empty

bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred
This bit is set in hardware; can bit only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or by writing a '0' to SPIROV.

bit 5 **SPIRBE:** RX FIFO Empty bit (valid only when ENHBUF = 1)
1 = RX FIFO is empty (CRPTR = SWPTR)
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

NOTES:

18.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit (I^2C)"** (DS60001116) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard. Figure 18-1 illustrates the I^2C module block diagram.

Each I^2C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I^2C module offers the following key features:

- I^2C interface supporting both master and slave operation
- I^2C Slave mode supports 7-bit and 10-bit addressing
- I^2C Master mode supports 7-bit and 10-bit addressing
- I^2C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I^2C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I^2C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking

REGISTER 18-2: I2CxSTAT: I^{2}C STATUS REGISTER (CONTINUED)

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 2 **R_W:** Read/Write Information bit (when operating as I^{2}C slave)
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
Hardware set or clear after reception of I^{2}C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty
Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty
Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0, HC	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
	RDSTART	—	—	—	—	—	DUALBUF	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>(2)		ALP(2)	CS2P(2)	CS1P(2)	—	WRSP	RDSP

Legend:	HC = Hardware cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **RDSTART:** Start a Read on the PMP Bus bit(3)
- 1 = Start a read cycle on the PMP bus
- 0 = No effect

This bit is cleared by hardware at the end of the read cycle when the BUSY bit (PMMODE<15>) = 0.

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **DUALBUF:** Parallel Master Port Dual Read/Write Buffer Enable bit

This bit is only valid in Master mode.
- 1 = PMP uses separate registers for reads and writes
  Reads: PMRADDR and PMRDIN
  Writes: PMRWADDR and PMDOUT
- 0 = PMP uses legacy registers for reads and writes
  Reads/Writes: PMADDR and PMRDIN

bit 16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit(1)
- 1 = PMP enabled
- 0 = PMP disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
- 11 = Lower 8 bits of address are multiplexed on PMD<15:0> pins
- 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
- 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>
- 00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
- 1 = PMP module uses TTL input buffers
- 0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
- 1 = PMWR/PMENB port enabled
- 0 = PMWR/PMENB port disabled

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

21.1 Control Registers

TABLE 21-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>										0000
		15:0	ON	—	SIDL	—	—	—	—	—	RTSECSEL	RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0210	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>				ARPT<7:0>								0000
0220	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0230	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>				xxxx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx00
0240	ALRMTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0250	ALRMDATE	31:16	—	—	—	—	—	—	—	—	MONTH10<3:0>				MONTH01<3:0>				00xx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

TABLE 23-1: CAN1 REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B340	C1FIFOBA	31:16	C1FIFOBA<31:0>																0000
		15:0																	0000
B350	C1FIFOCONn (n = 0-15)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
B360	C1FIFOINTn (n = 0-15)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
B370	C1FIFOUAn (n = 0-15)	31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
B380	C1FIFOCIn (n = 0-15)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C1FIFOCIn<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 23-12: C1FLTCON2: CAN FILTER CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN11	MSEL11<1:0>		FSEL11<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN10	MSEL10<1:0>		FSEL10<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN9	MSEL9<1:0>		FSEL9<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN8	MSEL8<1:0>		FSEL8<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN11:** Filter 11 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL11<1:0>:** Filter 11 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL11<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN10:** Filter 10 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL10<1:0>:** Filter 10 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 23-13: C1FLTCON3: CAN FILTER CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN15	MSEL15<1:0>		FSEL15<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN14	MSEL14<1:0>		FSEL14<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN13	MSEL13<1:0>		FSEL13<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN12	MSEL12<1:0>		FSEL12<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN15:** Filter 15 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL15<1:0>:** Filter 15 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL15<4:0>:** FIFO Selection bits
11111 = Reserved
•
•
•
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
•
•
•
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN14:** Filter 14 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL14<1:0>:** Filter 14 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 23-15: C1FIFOBA: CAN MESSAGE BUFFER BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	C1FIFOBA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	C1FIFOBA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	C1FIFOBA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0(1)	R-0(1)
	C1FIFOBA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **C1FIFOBA<31:0>:** CAN FIFO Base Address bits

These bits define the base address of all message buffers. Individual message buffers are located based on the size of the previous message buffers. This address is a physical address. Bits <1:0> are read-only and read as '0', forcing the messages to be 32-bit word-aligned in device RAM.

Note 1: This bit is unimplemented and will always read '0', which forces word-alignment of messages.

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = 100).

TABLE 27-2: PERIPHERAL MODULE DISABLE REGISTER SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F240	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CVRMD	—	—	—	CTMUMD	—	—	—	—	—	—	—	AD1MD	0000
F250	PMD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP3MD	CMP2MD	CMP1MD	0000
F260	PMD3	31:16	—	—	—	—	—	—	—	—	—	—	—	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000
F270	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	T5MD	T4MD	T3MD	T2MD	T1MD	0000
F280	PMD5	31:16	—	—	—	CAN1MD	—	—	—	USBMD(1)	—	—	—	—	—	—	I2C1MD	I2C1MD	0000
		15:0	—	—	—	—	SPI4MD	SPI3MD	SPI2MD	SPI1MD	—	—	—	U5MD	U4MD	U3MD	U2MD	U1MD	0000
F290	PMD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PMPMD	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	RTCCMD	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This bit is only available on devices with a USB module.

30.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

30.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

32.1 DC Characteristics

TABLE 32-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)(1)	Temp. Range (in °C)	Max. Frequency
			PIC32MX1XX/2XX/5XX 64/100-pin Family
MDC5	VBOR-3.6V	-40°C to +85°C	50 MHz

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for BOR values.

TABLE 32-2: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial	
Parameter No.	Typical(3)	Max.	Units	Conditions
Operating Current (IDD) (Note 1, 2)				
MDC24	25	40	mA	50 MHz

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash

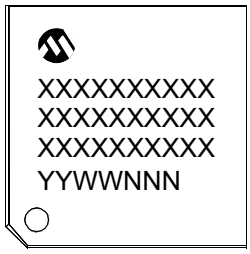
3: RTCC and JTAG are disabled

4: Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

34.0 PACKAGING INFORMATION

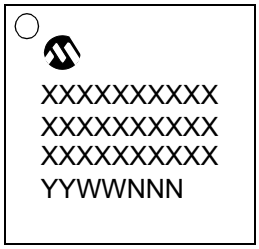
34.1 Package Marking Information

64-Lead TQFP (10x10x1 mm)

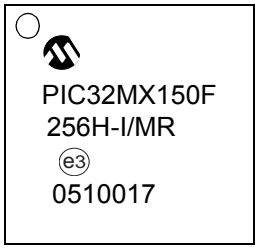


Example

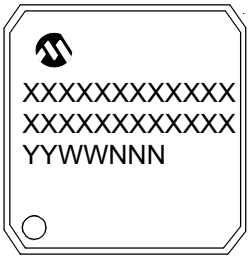
64-Lead QFN (9x9x0.9 mm)



Example

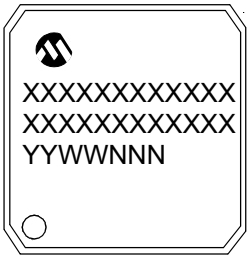


100-Lead TQFP (14x14x1 mm)



Example

100-Lead TQFP (12x12x1 mm)



Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.