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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

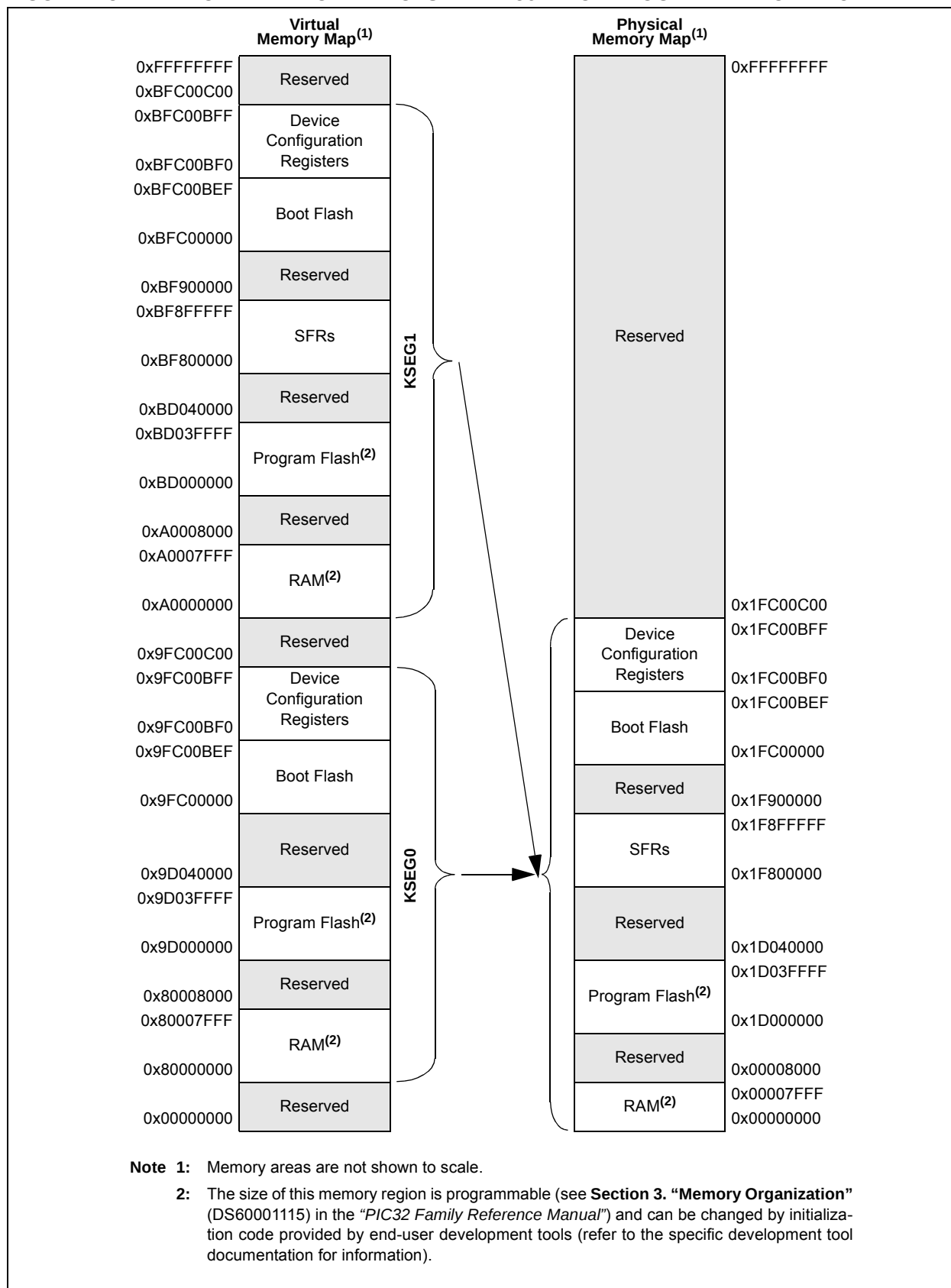
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx150f256l-i-pt

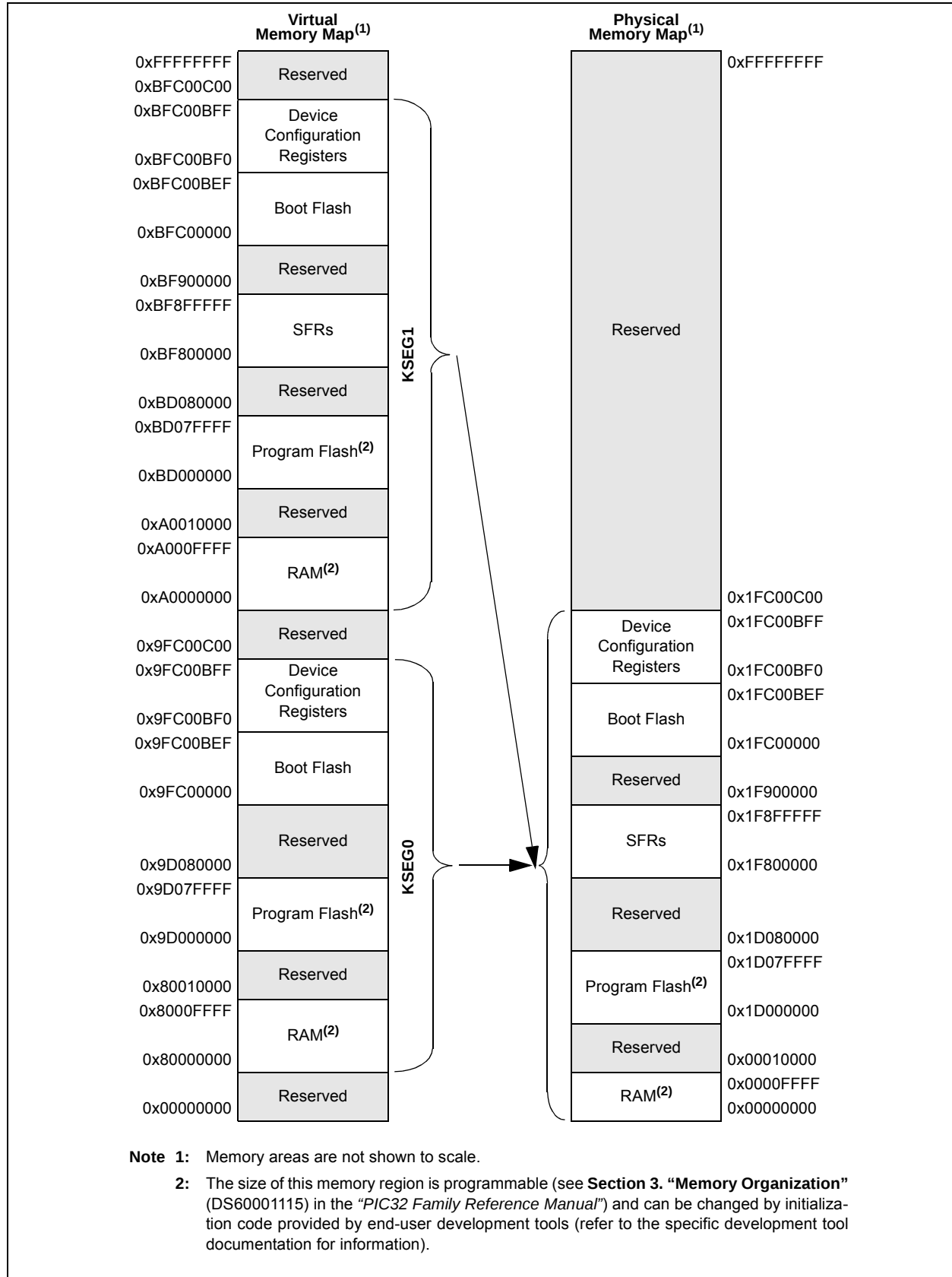
PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 256 KB OF PROGRAM MEMORY + 32 KB RAM



PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

FIGURE 4-4: MEMORY MAP FOR DEVICES WITH 512 KB OF PROGRAM MEMORY + 64 KB RAM



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REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
0 = No interrupt is pending
- bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
0 = No interrupt is pending
- bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
0 = No interrupt is pending
- bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
0 = No interrupt is pending
- bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
1 = A channel address error has been detected
 Either the source or the destination address is invalid.
0 = No interrupt is pending

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 9-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSSIZ<15:0>:** Channel Source Size bits

1111111111111111 = 65,535 byte source size

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0000000000000010 = 2 byte source size

0000000000000001 = 1 byte source size

0000000000000000 = 65,536 byte source size

REGISTER 9-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDSIZ<15:0>:** Channel Destination Size bits

1111111111111111 = 65,535 byte destination size

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0000000000000010 = 2 byte destination size

0000000000000001 = 1 byte destination size

0000000000000000 = 65,536 byte destination size

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 10-21: U1EP0-U1EP15: USB ENDPOINT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPD:** Low-Speed Direct Connection Enable bit (Host mode and U1EP0 only)

1 = Direct connection to a low-speed device enabled

0 = Direct connection to a low-speed device disabled; hub required with PRE_PID

bit 6 **RETRYDIS:** Retry Disable bit (Host mode and U1EP0 only)

1 = Retry NAKed transactions disabled

0 = Retry NAKed transactions enabled; retry done in hardware

bit 5 **Unimplemented:** Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit

If EPTXEN = 1 and EPRXEN = 1:

1 = Disable Endpoint n from Control transfers; only TX and RX transfers allowed

0 = Enable Endpoint n for Control (SETUP) transfers; TX and RX transfers also allowed

Otherwise, this bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit

1 = Endpoint n receive enabled

0 = Endpoint n receive disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit

1 = Endpoint n transmit enabled

0 = Endpoint n transmit disabled

bit 1 **EPSTALL:** Endpoint Stall Status bit

1 = Endpoint n was stalled

0 = Endpoint n was not stalled

bit 0 **EPHSK:** Endpoint Handshake Enable bit

1 = Endpoint Handshake enabled

0 = Endpoint Handshake disabled (typically used for isochronous endpoints)

TABLE 11-6: PORTC REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	ANSELC3	ANSELC2	ANSELC1	—	000E
6210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
6220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
6230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
6240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
6250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
6260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
6270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6280	CNENC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEC15	CNIEC14	CNIEC13	CNIEC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
6290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATC15	CNSTATC14	CNSTATC13	CNSTATC12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 18-1: I2CxCON: I²C 'x' CONTROL REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
	ON ⁽¹⁾	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

Legend:	HC = Cleared in Hardware
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** I²C Enable bit⁽¹⁾

1 = Enables the I²C module and configures the SDA and SCL pins as serial port pins

0 = Disables the I²C module; all I²C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)

1 = Release SCLx clock

0 = Hold SCLx clock low (clock stretch)

If STREN = 1:

Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:

Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.

bit 11 **STRICT:** Strict I²C Reserved Address Rule Enable bit

1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.

0 = Strict I²C Reserved Address Rule not enabled

bit 10 **A10M:** 10-bit Slave Address bit

1 = I2CxADD is a 10-bit slave address

0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit

1 = Slew rate control disabled

0 = Slew rate control enabled

bit 8 **SMEN:** SMBus Input Levels bit

1 = Enable I/O pin thresholds compliant with SMBus specification

0 = Disable SMBus input thresholds

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 19-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 5 **ABAUD**: Auto-Baud Enable bit
1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement disabled or completed
- bit 4 **RXINV**: Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'
- bit 3 **BRGH**: High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock enabled
0 = Standard Speed mode – 16x baud clock enabled
- bit 2-1 **PDSEL<1:0>**: Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity
- bit 0 **STSEL**: Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ADM_EN
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-1
	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT
7:0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/W-0	R-0
	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ADM_EN:** Automatic Address Detect Mode Enable bit

1 = Automatic Address Detect mode is enabled

0 = Automatic Address Detect mode is disabled

bit 23-16 **ADDR<7:0>:** Automatic Address Mask bits

When the ADM_EN bit is '1', this value defines the address character to use for automatic address detection.

bit 15-14 **UTXISEL<1:0>:** TX Interrupt Mode Selection bits

11 = Reserved, do not use

10 = Interrupt is generated and asserted while the transmit buffer is empty

01 = Interrupt is generated and asserted when all characters have been transmitted

00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV:** Transmit Polarity Inversion bit

If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is '0'):

1 = UxTX Idle state is '0'

0 = UxTX Idle state is '1'

If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):

1 = IrDA encoded UxTX Idle state is '1'

0 = IrDA encoded UxTX Idle state is '0'

bit 12 **URXEN:** Receiver Enable bit

1 = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON = 1)

0 = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module. UxRX pin is controlled by the port.

bit 11 **UTXBRK:** Transmit Break bit

1 = Send Break on next transmission. Start bit followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion

0 = Break transmission is disabled or completed

bit 10 **UTXEN:** Transmit Enable bit

1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1)

0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset. UxTX pin is controlled by the port.

bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)

1 = Transmit buffer is full

0 = Transmit buffer is not full, at least one more character can be written

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 20-7: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HSC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HSC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:	HSC = Set by Hardware; Cleared by Software		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit

1 = All writable input buffer registers are full

0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit

1 = A write attempt to a full input byte buffer occurred (must be cleared in software)

0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits

1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)

0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit

1 = All readable output buffer registers are empty

0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit

1 = A read occurred from an empty output byte buffer (must be cleared in software)

0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits

1 = Output buffer is empty (writing data to the buffer will clear this bit)

0 = Output buffer contains data that has not been transmitted

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 22-4: AD1CHS: ADC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NB	—	CH0SB<5:0>					
23:16	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NA	—	CH0SA<5:0>					
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **CH0NB:** Negative Input Select bit for Sample B

1 = Channel 0 negative input is AN1

0 = Channel 0 negative input is VREFL

bit 30 **Unimplemented:** Read as '0'

bit 29-24 **CH0SB<5:0>:** Positive Input Select bits for Sample B

For 64-pin devices:

011110 = Channel 0 positive input is Open⁽¹⁾

011101 = Channel 0 positive input is CTMU temperature sensor (CTMUT)⁽²⁾

011100 = Channel 0 positive input is IVREF⁽³⁾

011011 = Channel 0 positive input is AN27

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000001 = Channel 0 positive input is AN1

000000 = Channel 0 positive input is AN0

For 100-pin devices:

110010 = Channel 0 positive input is Open⁽¹⁾

110001 = Channel 0 positive input is CTMU temperature sensor (CTMUT)⁽²⁾

110000 = Channel 0 positive input is IVREF⁽³⁾

101111 = Channel 0 positive input is AN47

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0000001 = Channel 0 positive input is AN1

0000000 = Channel 0 positive input is AN0

bit 23 **CH0NA:** Negative Input Select bit for Sample A Multiplexer Setting⁽³⁾

1 = Channel 0 negative input is AN1

0 = Channel 0 negative input is VREFL

bit 22 **Unimplemented:** Read as '0'

Note 1: This selection is only used with CTMU capacitive and time measurement.

2: See **Section 26.0 "Charge Time Measurement Unit (CTMU)"** for more information.

3: Internal precision 1.2V reference. See **Section 24.0 "Comparator"** for more information.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 22-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL31 ⁽²⁾	CSSL30 ⁽¹⁾	CSSL29 ⁽¹⁾	CSSL28 ⁽¹⁾	CSSL27	CSSL26	CSSL25	CSSL24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL23	CSSL21	CSSL21	CSSL20	CSSL19	CSSL18	CSSL17	CSSL16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CSSL<31:0>**: ADC Input Pin Scan Selection bits

1 = Select ANx for input scan; CSSLx = ANx, where 'x' = 0-31

0 = Skip ANx for input scan; CSSLx = ANx, where 'x' = 0-31

Note 1: For devices with 64 pins, CSSL28 selects IVREF (Band Gap) for scan; CSSL29 selects CTMU temperature diode for scan; and CSSL30 selects CTMU input for scan

2: On devices with less than 32 analog inputs, all CSSLx bits can be selected; however, inputs selected for scan without a corresponding input on the device will convert to VREFL.

REGISTER 22-6: AD1CSSL2: ADC INPUT SCAN SELECT REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	CSSL50 ⁽¹⁾	CSSL49 ⁽¹⁾	CSSL48 ⁽¹⁾
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL47	CSSL46	CSSL45	CSSL44	CSSL43	CSSL42	CSSL41	CSSL40
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL39	CSSL38	CSSL37	CSSL36	CSSL35	CSSL34	CSSL33	CSSL32

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-19 **Unimplemented:** Read as '0'

bit 18-0 **CSSL<50:32>**: ADC Input Pin Scan Selection bits

1 = Select ANx for input scan; CSSLx = ANx, where 'x' = 32-50

0 = Skip ANx for input scan; CSSLx = ANx, where 'x' = 32-50

Note 1: For devices with 100 or more pins, CSSL48 selects IVREF (Band Gap) for scan; CSSL49 selects CTMU temperature diode for scan; and CSSL50 selects CTMU input for scan

Note: The ANx inputs in this register only support devices with 100 or more pins.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 28-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
23:16	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	R/P FPLLODIV<2:0>	R/P	R/P
15:8	R/P UPLLEN ⁽¹⁾	r-1 —	r-1 —	r-1 —	r-1 —	R/P UPLLDIV<2:0> ⁽¹⁾	R/P	R/P
7:0	r-1 —	R/P-1 FPLLMUL<2:0>	R/P	R/P-1	r-1 —	R/P FPLLDIV<2:0>	R/P	R/P

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLLODIV<2:0>:** Default PLL Output Divisor bits

111 = PLL output divided by 256
110 = PLL output divided by 64
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit⁽¹⁾
1 = Disable and bypass USB PLL
0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLLDIV<2:0>:** USB PLL Input Divider bits⁽¹⁾

111 = 12x divider
110 = 10x divider
101 = 6x divider
100 = 5x divider
011 = 4x divider
010 = 3x divider
010 = 3x divider
001 = 2x divider
000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits

111 = 24x multiplier
110 = 21x multiplier
101 = 20x multiplier
100 = 19x multiplier
011 = 18x multiplier
010 = 17x multiplier
001 = 16x multiplier
000 = 15x multiplier

bit 3 **Reserved:** Write '1'

Note 1: This bit is available on PIC32MX2XX/5XX devices only.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 28-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 2-0 **FPLLIDIV<2:0>**: PLL Input Divider bits

111 = 12x divider

110 = 10x divider

101 = 6x divider

100 = 5x divider

011 = 4x divider

010 = 3x divider

001 = 2x divider

000 = 1x divider

Note 1: This bit is available on PIC32MX2XX/5XX devices only.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 31-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp	
Parameter No.	Typical ⁽³⁾	Max.	Units	Conditions
Operating Current (IDD) (Notes 1, 2, 5)				
DC20	2	8	mA	4 MHz (Note 4)
DC21	7	13	mA	10 MHz
DC22	10	18	mA	20 MHz (Note 4)
DC23	15	25	mA	30 MHz (Note 4)
DC24	20	32	mA	40 MHz
DC25	180	250	μA	+25°C, 3.3V LPRC (31 kHz) (Note 4)

- Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.
- 2:** The test conditions for IDD measurements are as follows:
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
 - CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
 - No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
 - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to Vss
 - MCLR = VDD
 - CPU executing while(1) statement from Flash
 - RTCC and JTAG are disabled
- 3:** Data in the "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.
- 4:** This parameter is characterized, but not tested in manufacturing.
- 5:** IPD electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

FIGURE 31-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS

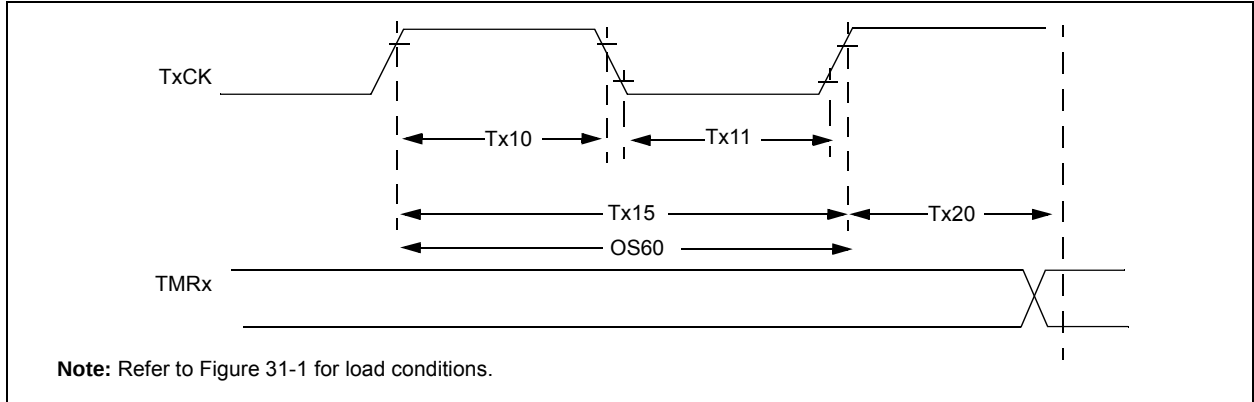


TABLE 31-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS ⁽¹⁾				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics ⁽²⁾		Min.	Typical	Max.	Units	Conditions
TA10	TtxH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TtxL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TtxP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 25 ns or 2 TPB)/N] + 30 ns	—	—	ns	VDD > 2.7V
				[(Greater of 25 ns or 2 TPB)/N] + 50 ns	—	—	ns	VDD < 2.7V
			Asynchronous, with prescaler	20	—	—	ns	VDD > 2.7V (Note 3)
				50	—	—	ns	VDD < 2.7V (Note 3)
OS60	Ft1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting the TCS (T1CON<1>) bit)		32	—	100	kHz	—
TA20	TckEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—		1	TPB	—

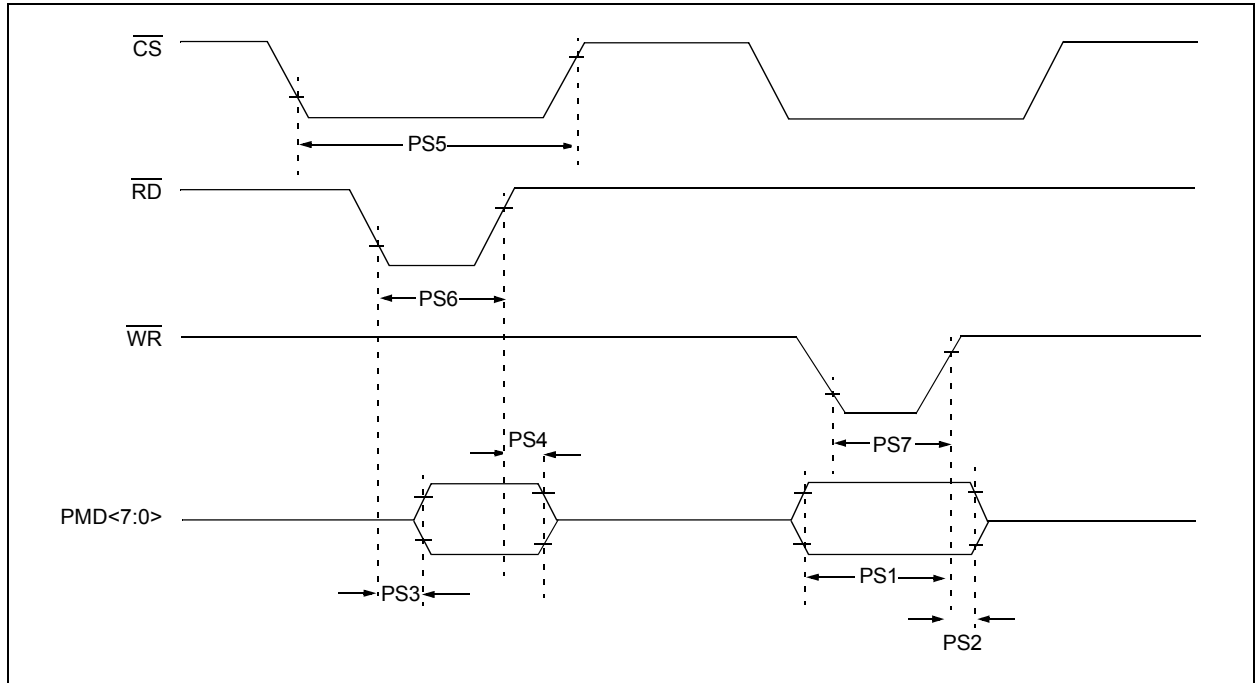
Note 1: Timer1 is a Type A timer.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

FIGURE 31-20: PARALLEL SLAVE PORT TIMING



33.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 33-1: V_{OH} – 4x DRIVER PINS

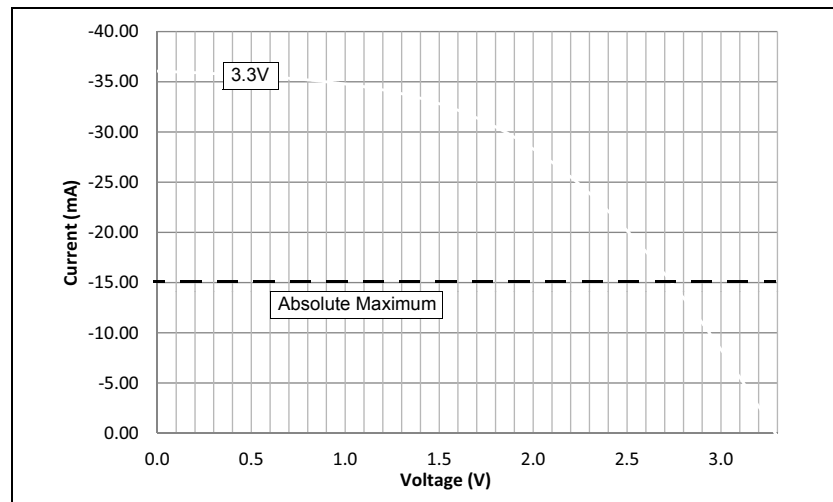


FIGURE 33-3: V_{OL} – 4x DRIVER PINS

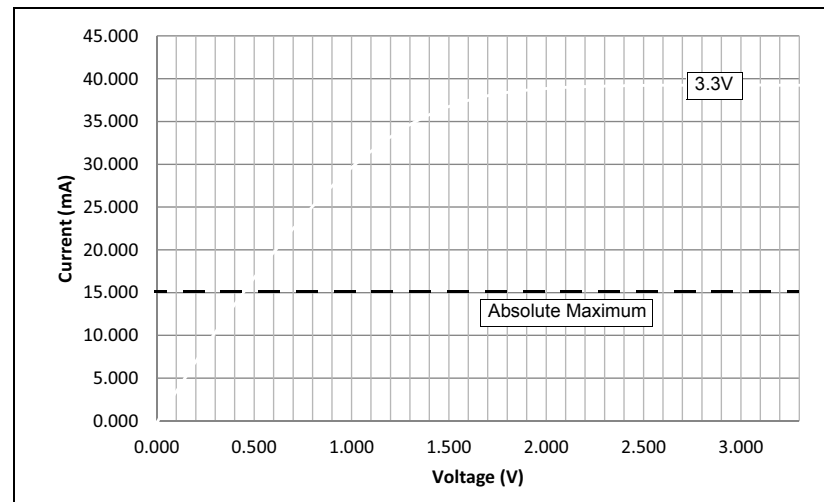


FIGURE 33-2: V_{OH} – 8x DRIVER PINS

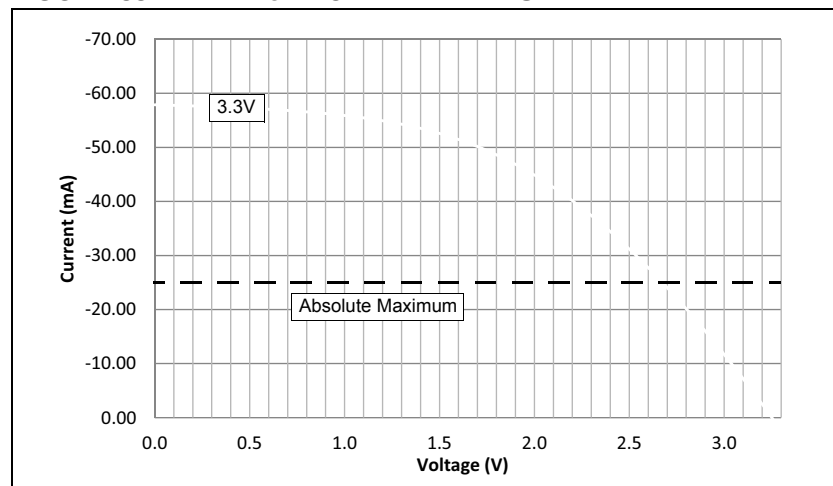
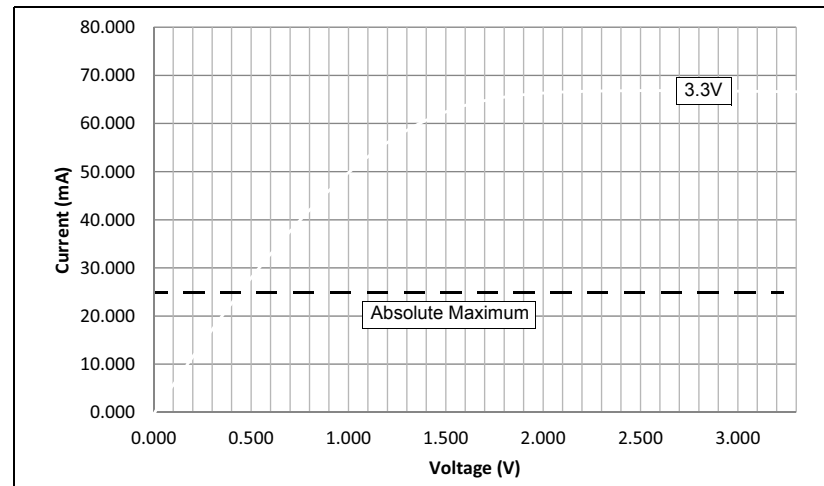


FIGURE 33-4: V_{OL} – 8x DRIVER PINS



PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

MPLAB PM3 Device Programmer.....	307
MPLAB REAL ICE In-Circuit Emulator System.....	307
MPLINK Object Linker/MPLIB Object Librarian	306

O

Oscillator Configuration.....	73
Output Compare.....	177

P

Packaging	361
Details	362
Marking	361
Parallel Master Port (PMP)	207
PIC32 Family USB Interface Diagram.....	106
Pinout I/O Descriptions (table)	14
Power-on Reset (POR)	
and On-Chip Voltage Regulator	302
Power-Saving Features.....	285
CPU Halted Methods	285
Operation	285
with CPU Running.....	285

R

Real-Time Clock and Calendar (RTCC).....	221
Register Map	
ADC	233
Bus Matrix	45
Comparator	272
Comparator Voltage Reference	276
CTMU	280
Device and Revision ID Summary	292
Device Configuration Word Summary.....	292
DMA Channel 0-3	87
DMA CRC	86
DMA Global.....	86
Flash Controller.....	64
I2C1 and I2C2	193
Input Capture 1-5	174
Interrupt.....	56
Oscillator Configuration.....	76, 170
Output Compare1-5	178
Parallel Master Port	208
Peripheral Pin Select Input	151
Peripheral Pin Select Output.....	153
PORTA (100-pin Devices Only)	137
PORTB.....	138
PORTB (100-pin Devices Only)	139
PORTC (64-pin Devices Only)	140
PORTD (100-pin Devices Only)	141
PORTD (64-pin Devices Only)	142
PORTE (100-pin Devices Only)	143
PORTE (64-pin Devices Only)	144
PORTF (100-pin General Purpose Devices Only)	145
PORTF (100-pin USB Devices Only)	146
PORTF (64-pin General Purpose Devices Only)	147
PORTF (64-pin USB Devices Only)	148
PORTG (100-pin Devices Only)	149
PORTG (64-pin Devices Only)	150
RTCC	222
SPI1 through SPI4	182
Timer1	160
Timer2-5.....	165
UART1-5	200
USB.....	107
Registers	
[<i>pin name</i>]R (Peripheral Pin Select Input).....	157

AD1CHS (ADC Input Select)	239
AD1CON1 (A/D Control 1).....	230
AD1CON1 (ADC Control 1)	230, 235
AD1CON2 (ADC Control 2)	237
AD1CON3 (ADC Control 3)	238
AD1CSSL (ADC Input Scan Select)	241
AD1CSSL2 (ADC Input Scan Select 2)	241
ALRMDATE (Alarm Date Value).....	230
ALRMDATECLR (ALRMDATE Clear)	230
ALRMTIME (Alarm Time Value)	229
ALRMTIMECLR (ALRMTIME Clear)	230
ALRMTIMEINV (ALRMTIME Invert)	230
ALRMTIMESET (ALRMTIME Set).....	230
BMXBOOTSZ (Boot Flash (IFM) Size)	51
BMXCON (Bus Matrix Configuration)	46
BMXDKPBA (Data RAM Kernel Program Base Address).....	47
BMXDRMSZ (Data RAM Size Register).....	50
BMXDUDBA (Data RAM User Data Base Address)....	48
BMXDUPBA (Data RAM User Program Base Address).....	49
BMXPFMSZ (Program Flash (PFM) Size).....	51
BMXPUPBA (Program Flash (PFM) User Program Base Address).....	50
CiCFG (CAN Baud Rate Configuration)	248
CiCON (CAN Module Control).....	246
CiFIFOBA (CAN Message Buffer Base Address).....	265
CiFIFOCINn (CAN Module Message Index Register 'n') 270	270
CiFIFOCINn (CAN FIFO Control Register 'n')	266
CiFIFOINTn (CAN FIFO Interrupt Register 'n').....	268
CiFIFOUAn (CAN FIFO User Address Register 'n') ..	270
CiFLTCON0 (CAN Filter Control 0)	256
CiFLTCON1 (CAN Filter Control 1)	258
CiFLTCON2 (CAN Filter Control 2)	260
CiFLTCON3 (CAN Filter Control 3)	262
CiFSTAT (CAN FIFO Status).....	253
CiINT (CAN Interrupt).....	250
CiRXFn (CAN Acceptance Filter 'n').....	264
CiRXMn (CAN Acceptance Filter Mask 'n')	255
CiRXOVF (CAN Receive FIFO Overflow Status)	254
CiTMR (CAN Timer)	254
CiTREC (CAN Transmit/Receive Error Count).....	253
CiVEC (CAN Interrupt Code).....	252
CM1CON (Comparator 1 Control).....	273
CMSTAT (Comparator Control Register).....	274
CNCONx (Change Notice Control for PORTx).....	158
CTMUCON (CTMU Control).....	281
CVRCON (Comparator Voltage Reference Control) 277	
DCHxCON (DMA Channel x Control).....	95
DCHxCPTR (DMA Channel x Cell Pointer)	102
DCHxCSIZ (DMA Channel x Cell-Size).....	102
DCHxDAT (DMA Channel x Pattern Data)	103
DCHxDPTR (Channel x Destination Pointer)	101
DCHxDSA (DMA Channel x Destination Start Address).....	99
DCHxDSIZ (DMA Channel x Destination Size)	100
DCHxECON (DMA Channel x Event Control)	96
DCHxINT (DMA Channel x Interrupt Control).....	97
DCHxSPTR (DMA Channel x Source Pointer)	101
DCHxSSA (DMA Channel x Source Start Address)...	99
DCHxSSIZ (DMA Channel x Source Size)	100
DCRCCON (DMA CRC Control).....	92
DCRCDATA (DMA CRC Data)	94
DCRCXOR (DMA CRCXOR Enable)	94

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

DEVCFG0 (Device Configuration Word 0)	293
DEVCFG1 (Device Configuration Word 1)	295
DEVCFG2 (Device Configuration Word 2)	297
DEVCFG3 (Device Configuration Word 3)	299
DEVID (Device and Revision ID)	301
DMAADDR (DMA Address)	91
DMAADDR (DMR Address)	91
DMACON (DMA Controller Control)	90
DMASTAT (DMA Status)	91
I2CxCON (I2C 'x' Control Register ('x' = 1 and 2))	194
I2CxSTAT (I2C Status Register)	196
ICxCON (Input Capture x Control)	175
IFSx (Interrupt Flag Status)	60
INTCON (Interrupt Control)	58
INTSTAT (Interrupt Status)	59
IPCx (Interrupt Priority Control)	61
IPTMR Interrupt Proximity Timer	59
NVMADDR (Flash Address)	66
NVMCON (Programming Control)	65
NVMDATA (Flash Program Data)	67
NVMKEY (Programming Unlock)	66
NVMSRCADDR (Source Data Address)	67
OCxCON (Output Compare x Control)	179
OSCCON (Oscillator Control)	77
PMADDR (Parallel Port Address)	213
PMAEN (Parallel Port Pin Enable)	215
PMCON (Parallel Port Control)	209
PMDIN (Parallel Port Input Data)	214, 219
PMDOUT (Parallel Port Output Data)	214
PMMODE (Parallel Port Mode)	211
PMRADDR (Parallel Port Read Address)	218
PMSTAT (Parallel Port Status (Slave Modes Only))	216
PMWADDR (Parallel Port Write Address)	217
REFOCON (Reference Oscillator Control)	81
REFOTRIM (Reference Oscillator Trim)	83
RPnR (Peripheral Pin Select Output)	157
RSWRST (Software Reset)	72
RTCCON (RTC Control)	223
RTCDATE (RTC Date Value)	228
RTCTIME (RTC Time Value)	227
SPIxCON (SPI Control)	184
SPIxCON2 (SPI Control 2)	187
SPIxSTAT (SPI Status)	188
T1CON (Type A Timer Control)	161
TxCON (Type B Timer Control)	166
U1ADDR (USB Address)	123
U1BDTP1 (USB BDT Page 1)	125
U1BDTP2 (USB BDT Page 2)	126
U1BDTP3 (USB BDT Page 3)	126
U1CNFG1 (USB Configuration 1)	127
U1CON (USB Control)	121
U1EIE (USB Error Interrupt Enable)	119
U1EIR (USB Error Interrupt Status)	117
U1EP0-U1EP15 (USB Endpoint Control)	128
U1FRMH (USB Frame Number High)	124
U1FRML (USB Frame Number Low)	123
U1IE (USB Interrupt Enable)	116
U1IR (USB Interrupt)	115
U1OTGCON (USB OTG Control)	113
U1OTGIE (USB OTG Interrupt Enable)	111
U1OTGIR (USB OTG Interrupt Status)	110
U1OTGSTAT (USB OTG Status)	112
U1PWRC (USB Power Control)	114
U1SOF (USB SOF Threshold)	125
U1STAT (USB Status)	120

U1TOK (USB Token)	124
WDTCON (Watchdog Timer Control)	171
Reset SFR Summary	70
Resets	69
Revision History	375
RTCALRM (RTC ALARM Control)	225

S

Serial Peripheral Interface (SPI)	181
Software Simulator (MPLAB SIM)	307
Special Features	291

T

Timer1 Module	159
Timer2/3, Timer4/5 Modules	163
Timing Diagrams	
10-Bit Analog-to-Digital Conversion (ASAM = 0, SSRC<2:0> = 000)	345
10-Bit Analog-to-Digital Conversion (ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)	346
EJTAG	352
External Clock	321
I/O Characteristics	324
I2Cx Bus Data (Master Mode)	335
I2Cx Bus Data (Slave Mode)	338
I2Cx Bus Start/Stop Bits (Master Mode)	335
I2Cx Bus Start/Stop Bits (Slave Mode)	338
Input Capture (CAPx)	328
OCx/PWM	329
Output Compare (OCx)	329
Parallel Master Port Read	348
Parallel Master Port Write	349
Parallel Slave Port	347
SPIx Master Mode (CKE = 0)	330
SPIx Master Mode (CKE = 1)	331
SPIx Slave Mode (CKE = 0)	332
SPIx Slave Mode (CKE = 1)	333
Timer1, 2, 3, 4, 5 External Clock	327
UART Reception	206
UART Transmission (8-bit or 9-bit Data)	206
Timing Requirements	
CLKO and I/O	324
Timing Specifications	
I2Cx Bus Data Requirements (Master Mode)	336
I2Cx Bus Data Requirements (Slave Mode)	339
Input Capture Requirements	328
Output Compare Requirements	329
Simple OCx/PWM Mode Requirements	329
SPIx Master Mode (CKE = 0) Requirements	330
SPIx Master Mode (CKE = 1) Requirements	331
SPIx Slave Mode (CKE = 1) Requirements	333
SPIx Slave Mode Requirements (CKE = 0)	332
Timing Specifications (50 MHz)	
SPIx Master Mode (CKE = 0) Requirements	356
SPIx Master Mode (CKE = 1) Requirements	356
SPIx Slave Mode (CKE = 1) Requirements	357
SPIx Slave Mode Requirements (CKE = 0)	357

U

UART	199
USB On-The-Go (OTG)	105

V

VCAP pin	302
Voltage Regulator (On-Chip)	302