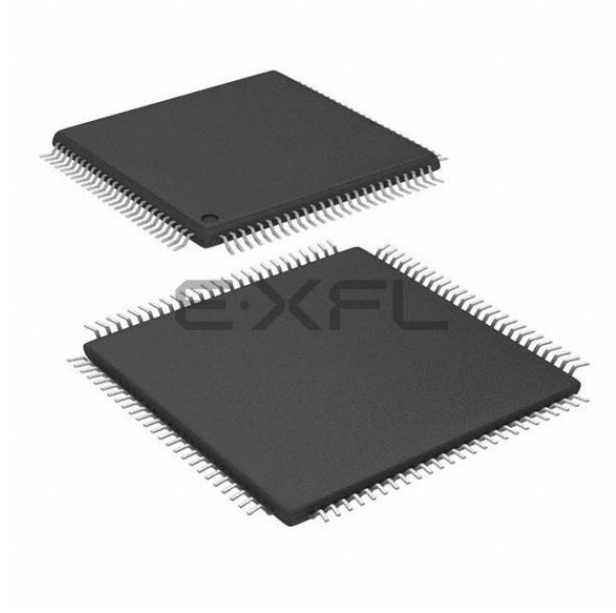
# Microchip Technology - PIC32MX150F256LT-50I/PT Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 48x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx150f256lt-50i-pt |

**TABLE 4: PIN NAMES FOR 100-PIN GENERAL PURPOSE DEVICES (CONTINUED)**

**100-PIN TQFP (TOP VIEW)**

**PIC32MX130F128L**
**PIC32MX150F256L**
**PIC32MX170F512L**

100

1

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 71 | RPD11/PMA14/RD11 | 86 | VDD |
| 72 | RPD0/RD0 | 87 | AN44/C3INA/RPF0/PMD11/RF0 |
| 73 | SOSCI/RPC13/RC13 | 88 | AN45/RPF1/PMD10/RF1 |
| 74 | SOSCO/RPC14/T1CK/RC14 | 89 | RPG1/PMD9/RG1 |
| 75 | VSS | 90 | RPG0/PMD8/RG0 |
| 76 | AN24/RPD1/RD1 | 91 | RA6 |
| 77 | AN25/RPD2/RD2 | 92 | CTED8/RA7 |
| 78 | AN26/C3IND/RPD3/RD3 | 93 | AN46/PMD0/RE0 |
| 79 | AN40/RPD12/PMD12/RD12 | 94 | AN47/PMD1/RE1 |
| 80 | AN41/PMD13/RD13 | 95 | RG14 |
| 81 | RPD4/PMWR/RD4 | 96 | RG12 |
| 82 | RPD5/PMRD/RD5 | 97 | RG13 |
| 83 | AN42/C3INC/PMD14/RD6 | 98 | AN20/PMD2/RE2 |
| 84 | AN43/C3INB/PMD15/RD7 | 99 | RPE3/CTPLS/PMD3/RE3 |
| 85 | VCAP | 100 | AN21/PMD4/RE4 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** Shaded pins are 5V tolerant.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| RTCC | 42 | 68 | O | — | Real-Time Clock Alarm Output |
| CVREFOUT | 23 | 34 | O | Analog | Comparator Voltage Reference (Output) |
| C1INA | 11 | 20 | I | Analog | Comparator 1 Inputs |
| C1INB | 12 | 21 | I | Analog | |
| C1INC | 5 | 11 | I | Analog | |
| C1IND | 4 | 10 | I | Analog | |
| C2INA | 13 | 22 | I | Analog | Comparator 2 Inputs |
| C2INB | 14 | 23 | I | Analog | |
| C2INC | 8 | 14 | I | Analog | |
| C2IND | 6 | 12 | I | Analog | |
| C3INA | 58 | 87 | I | Analog | Comparator 3 Inputs |
| C3INB | 55 | 84 | I | Analog | |
| C3INC | 54 | 83 | I | Analog | |
| C3IND | 51 | 78 | I | Analog | |
| C1OUT | PPS | PPS | O | — | Comparator 1 Output |
| C2OUT | PPS | PPS | O | — | Comparator 2 Output |
| C3OUT | PPS | PPS | O | — | Comparator 3 Output |
| PMALL | 30 | 44 | O | TTL/ST | Parallel Master Port Address Latch Enable Low Byte |
| PMALH | 29 | 43 | O | TTL/ST | Parallel Master Port Address Latch Enable High Byte |
| PMA0 | 30 | 44 | O | TTL/ST | Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes) |
| PMA1 | 29 | 43 | O | TTL/ST | Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes) |

**Legend:** CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

**Note 1:** This pin is only available on devices without a USB module.

**2:** This pin is only available on devices with a USB module.

**3:** This pin is not available on 64-pin devices with a USB module.

**4:** This pin is only available on 100-pin devices without a USB module.

**REGISTER 6-1: NVMCON: PROGRAMMING CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 | U-0 | U-0 | U-0 |
| | WR | WREN(1) | WRERR(2) | LVDERR(2) | LVDSTAT(2) | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | NVMOP<3:0> | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit
This bit is writable when WREN = 1 and the unlock sequence is followed.
1 = Initiate a Flash operation. Hardware clears this bit when the operation completes
0 = Flash operation complete or inactive

bit 14 **WREN:** Write Enable bit(1)
1 = Enable writes to WR bit and enables LVD circuit
0 = Disable writes to WR bit and disables LVD circuit
This is the only bit in this register reset by a device Reset.

bit 13 **WRERR:** Write Error bit(2)
This bit is read-only and is automatically set by hardware.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit (LVD circuit must be enabled)(2)
This bit is read-only and is automatically set by hardware.
1 = Low-voltage detected (possible data corruption, if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11 **LVDSTAT:** Low-Voltage Detect Status bit (LVD circuit must be enabled)(2)
This bit is read-only and is automatically set, and cleared, by hardware.
1 = Low-voltage event active
0 = Low-voltage event NOT active

bit 10-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation bits
These bits are writable when WREN = 0.
1111 =Reserved
•
•
•
0111 = Reserved
0110 =No operation
0101 =Program Flash (PFM) erase operation: erases PFM, if all pages are not write-protected
0100 =Page erase operation: erases page selected by NVMADDR, if it is not write-protected
0011 =Row program operation: programs row selected by NVMADDR, if it is not write-protected
0010 =No operation
0001 =Word program operation: programs word selected by NVMADDR, if it is not write-protected
0000 = No operation

**Note 1:** This bit is cleared by any reset (i.e., POR, BOR, WDT, $\overline{\text{MCLR}}$, SWR).

**2:** This bit is only cleared by setting NVMOP = 0000, and initiating a Flash WR operation or a POR. Any other kind of reset (i.e., BOR, WDT, $\overline{\text{MCLR}}$) does not clear this bit.

**REGISTER 9-16: DCHxCSIZ: DMA CHANNEL 'x' CELL-SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHCSIZ<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHCSIZ<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>:** Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event
.
.
.
0000000000000010 = 2 bytes transferred on an event
0000000000000001= 1 byte transferred on an event
0000000000000000 = 65,536 bytes transferred on an event

**REGISTER 9-17: DCHxCPTR: DMA CHANNEL 'x' CELL POINTER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHCPTR<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHCPTR<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<7:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event
.
.
.
0000000000000001 = 1 byte has been transferred since the last event
0000000000000000 = 0 bytes have been transferred since the last event

**Note:** When in Pattern Detect mode, this register is reset on a pattern detect.

**REGISTER 10-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | U-0 | R/WC-0, HS |
| | IDIF | T1MSECIF | LSTATEIF | ACTVIF | SESVDIF | SESENDIF | — | VBUSVDIF |

| **Legend:** | WC = Write '1' to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
- 1 = Change in ID state detected
- 0 = No change in ID state detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
- 1 = USB line state has been stable for 1millisecond, but different from last time
- 0 = USB line state has not been stable for 1 millisecond

bit 4 **ACTVIF:** Bus Activity Indicator bit
- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
- 1 = Change on the session valid input detected
- 0 = No change on the session valid input detected

**REGISTER 10-5: U1PWRC: USB POWER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | UACTPND | — | — | USLPGRD | USBBUSY | — | USUSPEND | USBPWR |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
- 1 = USB bus activity has been detected; but an interrupt is pending, it has not been generated yet
- 0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit
- 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
- 0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit(1)
- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled

**Note:** When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit
- 1 = USB module is placed in Suspend mode (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit
- 1 = USB module is turned on
- 0 = USB module is disabled (Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

**REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS |
| | BTSEF | BMXEF | DMAEF(1) | BTOEF(2) | DFN8EF | CRC16EF | CRC5EF(4) / EOFEF(3,5) | PIDEF |

| Legend: | WC = Write ‘1’ to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **BTSEF:** Bit Stuff Error Flag bit
- 1 = Packet rejected due to bit stuff error
- 0 = Packet accepted

bit 6 **BMXEF:** Bus Matrix Error Flag bit
- 1 = The base address, of the BDT, or the address of an individual buffer pointed to by a BDT entry, is invalid.
- 0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit(1)
- 1 = USB DMA error condition detected
- 0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-Out Error Flag bit(2)
- 1 = Bus turnaround time-out has occurred
- 0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit
- 1 = Data field received is not an integral number of bytes
- 0 = Data field received is an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
- 1 = Data packet rejected due to CRC16 error
- 0 = Data packet accepted

**Note 1:** This type of error occurs when the module’s request for the DMA bus is not granted in time to service the module’s demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

**2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

**3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

**4:** Device mode.

**5:** Host mode.

**REGISTER 10-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | — | FRMH<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-3 **Unimplemented:** Read as '0'

bit 2-0 **FRMH<2:0>:** The Upper 3 bits of the Frame Numbers bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

**REGISTER 10-15: U1TOK: USB TOKEN REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PID<3:0>(1) | | | | EP<3:0> | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits(1)
0001 = OUT (TX) token type transaction
1001 = IN (RX) token type transaction
1101 = SETUP (TX) token type transaction
**Note:** All other values are reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits
The four bit value must specify a valid endpoint.

**Note 1:** All other values are reserved and must not be used.

## 11.4 Control Registers

**TABLE 11-3: PORTA REGISTER MAP 100-PIN DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6000 | ANSELA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | ANSELA10 | ANSELA9 | — | — | — | — | — | — | — | — | — | 0060 |
| 6010 | TRISA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISA15 | TRISA14 | — | — | — | TRISA10 | TRISA9 | — | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | C6FF |
| 6020 | PORTA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RA15 | RA14 | — | — | — | RA10 | RA9 | — | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | xxxx |
| 6030 | LATA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATA15 | LATA14 | — | — | — | LATA10 | LATA9 | — | LATA7 | LATA6 | LATA5 | LATA4 | LATA3 | LATA2 | LATA1 | LATA0 | xxxx |
| 6040 | ODCA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCA15 | ODCA14 | — | — | — | ODCA10 | ODCA9 | — | ODCA7 | ODCA6 | ODCA5 | ODCA4 | ODCA3 | ODCA2 | ODCA1 | ODCA0 | 0000 |
| 6050 | CNPUA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUA15 | CNPUA14 | — | — | — | CNPUA10 | CNPUA9 | — | CNPUA7 | CNPUA6 | CNPUA5 | CNPUA4 | CNPUA3 | CNPUA2 | CNPUA1 | CNPUA0 | 0000 |
| 6060 | CNPDA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDA15 | CNPDA14 | — | — | — | CNPDA10 | CNPDA9 | — | CNPDA7 | CNPDA6 | CNPDA5 | CNPDA4 | CNPDA3 | CNPDA2 | CNPDA1 | CNPDA0 | 0000 |
| 6070 | CNCONA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6080 | CNENA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIEA15 | CNIEA14 | — | — | — | CNIEA10 | CNIEA9 | — | CNIEA7 | CNIEA6 | CNIEA5 | CNIEA4 | CNIEA3 | CNIEA2 | CNIEA1 | CNIEA0 | 0000 |
| 6090 | CNSTATA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CN STATA15 | CN STATA14 | — | — | — | CN STATA10 | CN STATA9 | — | CN STATA7 | CN STATA6 | CN STATA5 | CN STATA4 | CN STATA3 | CN STATA2 | CN STATA1 | CN STATA0 | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**REGISTER 15-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER ('x' = 1 THROUGH 5)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | — | — | — | FEDGE | C32 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 |
| | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit | |
| -n = Bit Value at POR: ('0', '1', x = unknown) | | P = Programmable bit | r = Reserved bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit(1)
- 1 = Module enabled
- 0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Halt in CPU Idle mode
- 0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
- 1 = Capture rising edge first
- 0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
- 1 = 32-bit timer resource capture
- 0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
- 0 = Timer3 is the counter source for capture
- 1 = Timer2 is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture overflow occurred
- 0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty; at least one more capture value can be read
- 0 = Input capture buffer is empty

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**TABLE 17-1: SPI1 THROUGH SPI4 REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name[1] | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5C40 | SPI3CON2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SPI SGNEXT | — | — | FRM ERREN | SPI ROVEN | SPI TUREN | IGNROV | IGNTUR | AUDEN | — | — | — | AUD MONO | — | AUDMOD<1:0> | | 0000 |
| 5E00 | SPI4CON(2) | 31:16 | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | | MCLKSEL | — | — | — | — | — | SPIFE | ENHBUF | 0000 |
| | | 15:0 | ON | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | DISSDI | STXISEL<1:0> | | SRXISEL<1:0> | | 0000 |
| 5E10 | SPI4STAT(2) | 31:16 | — | — | — | RXBUFELM<4:0> | | | | | — | — | — | TXBUFELM<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | FRMERR | SPIBUSY | — | — | SPITUR | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF | 19EB |
| 5E20 | SPI4BUF(2) | 31:16 | DATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 5E30 | SPI4BRG(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | BRG<8:0> | | | | | | | | | 0000 |
| 5E40 | SPI4CON2(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SPI SGNEXT | — | — | FRM ERREN | SPI ROVEN | SPI TUREN | IGNROV | IGNTUR | AUDEN | — | — | — | AUD MONO | — | AUDMOD<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**2:** This register is only available on 100-pin devices.

## 18.1 Control Registers

**TABLE 18-1: I2C1 AND I2C2 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5000 | I2C1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | BFFF |
| 5010 | I2C1STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| 5020 | I2C1ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Register | | | | | | | | | | 0000 |
| 5030 | I2C1MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Mask Register | | | | | | | | | | 0000 |
| 5040 | I2C1BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | Baud Rate Generator Register | | | | | | | | | | | | 0000 |
| 5050 | I2C1TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 |
| 5060 | I2C1RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 |
| 5100 | I2C2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | BFFF |
| 5110 | I2C2STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| 5120 | I2C2ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Register | | | | | | | | | | 0000 |
| 5130 | I2C2MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Mask Register | | | | | | | | | | 0000 |
| 5140 | I2C2BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | Baud Rate Generator Register | | | | | | | | | | | | 0000 |
| 5150 | I2C2TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 |
| 5160 | I2C2RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

## 23.0 CONTROLLER AREA NETWORK (CAN)

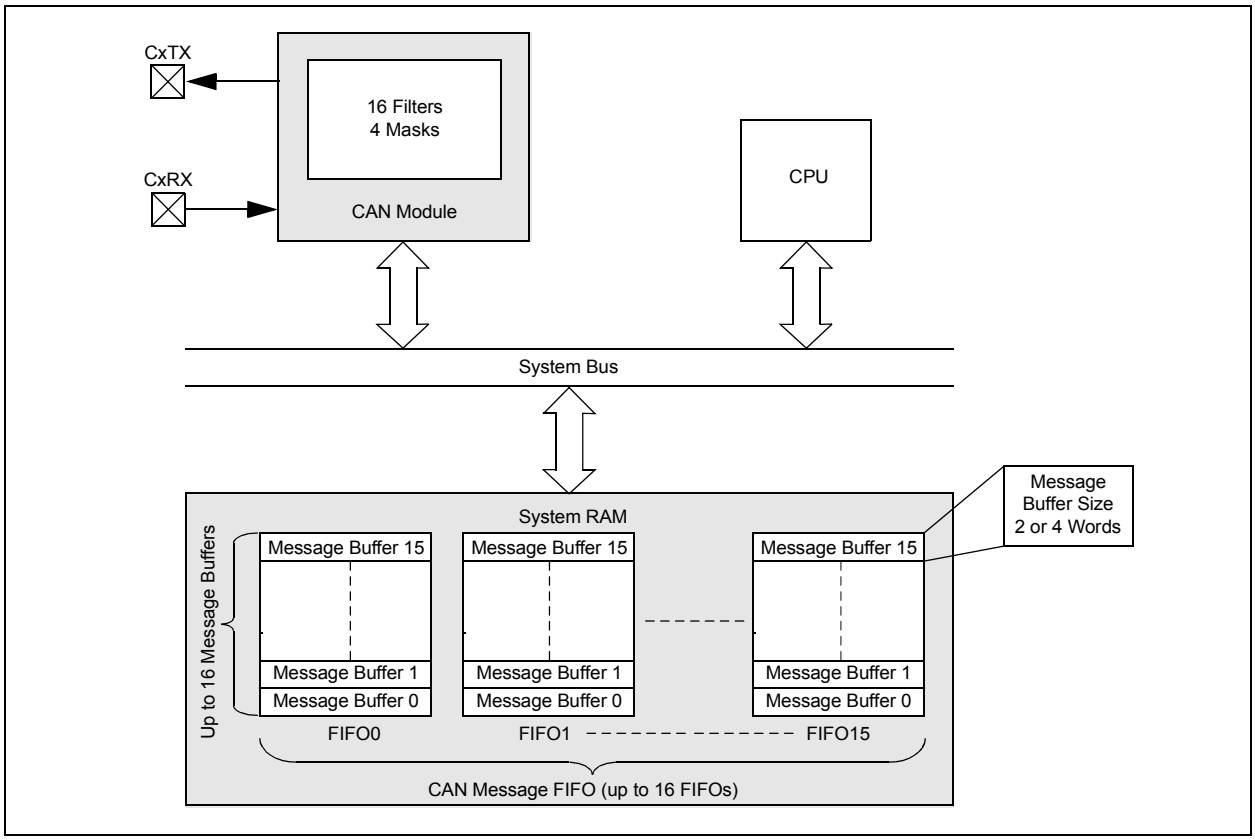
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 34. "Controller Area Network (CAN)"** (DS60001154) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Controller Area Network (CAN) module supports the following key features:

- Standards Compliance:
  - Full CAN 2.0B compliance
  - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
  - 16 message FIFOs
  - Each FIFO can have up to 16 messages for a total of 256 messages
  - FIFO can be a transmit message FIFO or a receive message FIFO
  - User-defined priority levels for message FIFOs used for transmission
  - 16 acceptance filters for message filtering
  - Four acceptance filter mask registers for message filtering
  - Automatic response to remote transmit request
  - DeviceNet™ addressing support
- Additional Features:
  - Loopback, Listen All Messages, and Listen Only modes for self-test, system diagnostics and bus monitoring
  - Low-power operating modes
  - CAN module is a bus master on the PIC32 system bus
  - Use of DMA is not required
  - Dedicated time-stamp timer
  - Dedicated DMA channels
  - Data-only Message Reception mode

Figure 23-1 illustrates the general structure of the CAN module.

**FIGURE 23-1: PIC32 CAN MODULE BLOCK DIAGRAM**



**REGISTER 23-10: C1FLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)**

bit 20-16 **FSEL2<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 15 **FLTEN1:** Filter 1 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL1<1:0>:** Filter 1 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL1<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN0:** Filter 0 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL0<1:0>:** Filter 0 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL0<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 23-13: C1FLTCON3: CAN FILTER CONTROL REGISTER 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN15 | MSEL15<1:0> | | FSEL15<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN14 | MSEL14<1:0> | | FSEL14<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN13 | MSEL13<1:0> | | FSEL13<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN12 | MSEL12<1:0> | | FSEL12<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN15:** Filter 15 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL15<1:0>:** Filter 15 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL15<4:0>:** FIFO Selection bits
11111 = Reserved
•
•
•
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
•
•
•
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN14:** Filter 14 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL14<1:0>:** Filter 14 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 23-17: C1FIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('n' = 0 THROUGH 15)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | TXNFULLIE | TXHALFIE | TXEMPTYIE |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | RXOVFLIE | RXFULLIE | RXHALFIE | RXNEMPTYIE |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | — | TXNFULLIF(1) | TXHALFIF | TXEMPTYIF(1) |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | RXOVFLIF | RXFULLIF(1) | RXHALFIF(1) | RXNEMPTYIF(1) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit
1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is not full
0 = FIFO is full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

**Note 1:** This bit is read-only and reflects the status of the FIFO.

**REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EDG1MOD | EDG1POL | EDG1SEL<3:0> | | | | EDG2STAT | EDG1STAT |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | EDG2MOD | EDG2POL | EDG2SEL<3:0> | | | | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON | — | CTMUSIDL | TGEN(1) | EDGEN | EDGSEQEN | IDISSEN(2) | CTTRIG |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ITRIM<5:0> | | | | | | IRNG<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **EDG1MOD:** Edge 1 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 30 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 programmed for a positive edge response
0 = Edge 1 programmed for a negative edge response

bit 29-26 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = IC4 Capture Event is selected
1110 = C2OUT pin is selected
1101 = C1OUT pin is selected
1100 = IC3 Capture Event is selected
1011 = IC2 Capture Event is selected
1010 = IC1 Capture Event is selected
1001 = CTED8 pin is selected
1000 = CTED7 pin is selected
0111 = CTED6 pin is selected
0110 = CTED5 pin is selected
0101 = CTED4 pin is selected
0100 = CTED3 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 25 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control edge source
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

**Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

**2:** The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

**3:** Refer to the CTMU Current Source Specifications (Table 31-41) in **Section 31.0 "40 MHz Electrical Characteristics"** for current values.

**4:** This bit setting is not available for the CTMU temperature diode.

**TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | | **Min.** | **Max.** | **Units** | **Conditions** |
| IS34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | 4000 | — | ns | — |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode **(Note 1)** | 250 | | ns | |
| IS40 | TAA:SCL | Output Valid from Clock | 100 kHz mode | 0 | 3500 | ns | — |
| | | | 400 kHz mode | 0 | 1000 | ns | |
| | | | 1 MHz mode **(Note 1)** | 0 | 350 | ns | |
| IS45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | The amount of time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode **(Note 1)** | 0.5 | — | µs | |
| IS50 | CB | Bus Capacitive Loading | | — | 400 | pF | — |

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**TABLE 31-37: PARALLEL SLAVE PORT REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param.No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| PS1 | TdtV2wrH | Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time) | 20 | — | — | ns | — |
| PS2 | TwrH2dtI | $\overline{WR}$ or $\overline{CS}$ Inactive to Data-In Invalid (hold time) | 40 | — | — | ns | — |
| PS3 | TrdL2dtV | $\overline{RD}$ and $\overline{CS}$ Active to Data-Out Valid | — | — | 60 | ns | — |
| PS4 | TrdH2dtI | $\overline{RD}$ Active or $\overline{CS}$ Inactive to Data-Out Invalid | 0 | — | 10 | ns | — |
| PS5 | Tcs | $\overline{CS}$ Active Time | TPB + 40 | — | — | ns | — |
| PS6 | TWR | $\overline{WR}$ Active Time | TPB + 25 | — | — | ns | — |
| PS7 | TRD | $\overline{RD}$ Active Time | TPB + 25 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 31-21: PARALLEL MASTER PORT READ TIMING DIAGRAM**