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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

	Pin N	umber							
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	Pin Type	Buffer Type	Description				
RF0	58	87	I/O	ST					
RF1	59	88	I/O	ST					
RF2	34 ⁽³⁾	52	I/O	ST					
RF3	33	51	I/O	ST					
RF4	31	49	I/O	ST					
RF5	32	50	I/O	ST	PORTF is a bidirectional I/O port				
RF6	35(1)	55 ⁽¹⁾	I/O	ST					
RF7	_	54 (4)	I/O	ST					
RF8	_	53	I/O	ST					
RF12	_	40	I/O	ST					
RF13	_	39	I/O	ST					
RG0	_	90	I/O	ST					
RG1	_	89	I/O	ST					
RG2	37(1)	57 ⁽¹⁾	I/O	ST	-				
RG3	36 ⁽¹⁾	56 ⁽¹⁾	I/O	ST					
RG6	4	10	I/O	ST					
RG7	5	11	I/O	ST					
RG8	6	12	I/O	ST	PORTG is a bidirectional I/O port				
RG9	8	14	I/O	ST					
RG12	_	96	I/O	ST	-				
RG13	_	97	I/O	ST					
RG14	_	95	I/O	ST					
RG15	_	1	I/O	ST	-				
T1CK	48	74	I	ST	Timer1 External Clock Input				
T2CK	PPS	PPS	I	ST	Timer2 External Clock Input				
T3CK	PPS	PPS	Ι	ST	Timer3 External Clock Input				
T4CK	PPS	PPS	I	ST	Timer4 External Clock Input				
T5CK	PPS	PPS	I	ST	Timer5 External Clock Input				
U1CTS	PPS	PPS	I	ST	UART1 Clear to Send				
U1RTS	PPS	PPS	0	_	UART1 Ready to Send				
U1RX	PPS	PPS	I	ST	UART1 Receive				
U1TX	PPS	PPS	0		UART1 Transmit				
U2CTS	PPS	PPS	I	ST	UART2 Clear to Send				
U2RTS	PPS	PPS	0		UART2 Ready to Send				
U2RX	PPS	PPS	1	ST	UART2 Receive				
U2TX	PPS	PPS	0		UART2 Transmit				
Legend:	CMOS = CM ST = Schmit	IOS compat	ible inpu ut with (it or output CMOS leve	Analog = Analog input I = Input O = Output Is TTL = TTL input buffer P = Power				

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

2.9 Considerations When Interfacing to Remotely Powered Circuits

2.9.1 NON-5V TOLERANT INPUT PINS

A quick review of the absolute maximum rating section in **31.0** "**40 MHz Electrical Characteristics**" will indicate that the voltage on any non-5v tolerant pin may not exceed AVDD/VDD + 0.3V. Figure 2-5 shows an example of a remote circuit using an independent power source, which is powered while connected to a PIC32 non-5V tolerant circuit that is not powered.

FIGURE 2-5: PIC32 NON-5V TOLERANT CIRCUIT EXAMPLE



Bit Range	Bit Bit Bit Bit 31/23/15/7 30/22/14/6 29/21/		Bit 29/21/13/5	Bit Bit Bit Bit 1/13/5 28/20/12/4 27/19/11/3 26/18		Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	_	—	_	—	_		—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:10	-	—	_	—	_	—	—	—		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0		
15:8	BMXDUDBA<15:8>									
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
7:0				BMXDU	DBA<7:0>					

REGISTER 4-3: BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER

Legend:

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 BMXDUDBA<15:10>: DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 BMXDUDBA<9:0>: Read-Only bits Value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	—	—	—	—	—	—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—		—	—			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0			
15:8		BMXDUPBA<15:8>									
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
7:0				BMXDU	PBA<7:0>						

REGISTER 4-4: BMXDUPBA: DATA RAM USER PROGRAM BASE ADDRESS REGISTER

Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 BMXDUPBA<15:10>: DRM User Program Base Address bits

When non-zero, the value selects the relative base address for User mode program space in RAM, BMXDUPBA must be greater than BMXDUDBA.

bit 9-0 BMXDUPBA<9:0>: Read-Only bits Value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

NOTES:

5.0 INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS60001108) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The PIC32MX1XX/2XX/5XX 64/100-pin interrupt module includes the following features:

- Up to 76 interrupt sources
- Up to 46 interrupt vectors
- · Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Software can generate any interrupt
- User-configurable interrupt vector table location
- User-configurable interrupt vector spacing

Note: The dedicated shadow register set is not available on these devices.



FIGURE 5-1: INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	-	—	—	—	—	—	
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—		—	—	
45.0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	
15:8	—	—	—	MVEC	—	TPC<2:0>			
7.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7.0	_	—		INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	

REGISTER 5-1: INTCON: INTERRUPT CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 Unimplemented: Read as '0'

bit 12 MVEC: Multi Vector Configuration bit

- 1 = Interrupt controller configured for multi vectored mode
- 0 = Interrupt controller configured for single vectored mode
- bit 11 Unimplemented: Read as '0'

bit 10-8 TPC<2:0>: Interrupt Proximity Timer Control bits

- 111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer
- 110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer
- 101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer
- 100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer
- 011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer
- 010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer
- 001 = Interrupts of group priority 1 start the Interrupt Proximity timer
- 000 = Disables Interrupt Proximity timer
- bit 7-5 Unimplemented: Read as '0'
- bit 4 INT4EP: External Interrupt 4 Edge Polarity Control bit
 - 1 = Rising edge
 - 0 = Falling edge
- bit 3 INT3EP: External Interrupt 3 Edge Polarity Control bit
 - 1 = Rising edge
 - 0 = Falling edge
- bit 2 INT2EP: External Interrupt 2 Edge Polarity Control bit
 - 1 = Rising edge
 - 0 = Falling edge
- bit 1 INT1EP: External Interrupt 1 Edge Polarity Control bit
 - 1 = Rising edge
 - 0 = Falling edge
- bit 0 INTOEP: External Interrupt 0 Edge Polarity Control bit
 - 1 = Rising edge
 - 0 = Falling edge

TABLE 9-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP (CONTINUED)

ess		6								Bi	its								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2000		31:16	—	_	-	—	—	—	—	—	-	-	-	-	-	-	—	—	0000
3280	DCH2CPTR	15:0								CHCPT	R<15:0>								0000
	DOUGDAT	31:16	_	_	_	_		_		_	_	_	_	_	_	_	_	_	0000
3290	DCH2DAI	15:0			_			_		_		•	•	CHPDA	AT<7:0>	•	•		0000
2240	DOUDOON	31:16	_		_			_		_	_	_	_	_	_	—	_		0000
32A0	DCH3CON	15:0	CHBUSY		—	—		_		CHCHNS	CHEN	CHAED	CHCHN	CHAEN	_	CHEDET	CHPR	l<1:0>	0000
32B0		31:16	6 — — — — — — — — CHAIRQ<7:0>									00FF							
5200	DONISLOON	15:0				CHSIR	Q<7:0>				CFORCE	CABORT	PATEN	SIRQEN	AIRQEN		—	—	FFF8
3200	DCH3INT	31:16	—	—	—	—	—	—	—		CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
0200	Donointi	15:0	_	—	—	_		—		—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
32D0	DCH3SSA	31:16								CHSSA	\<31:0>								0000
		15:0																	0000
32E0	DCH3DSA	31:16 15:0								CHDSA	\<31:0>								0000
		31:16	_		_	_		_		_	_	_	_	_	_	_	_		0000
32F0	DCH3SSIZ	15:0								CHSSIZ	Z<15:0>								0000
2200	DOUDDOIZ	31:16	—	_	_	_		_	_	_	_	_	—	—	—	—	_	—	0000
3300	DCH3DSIZ	15:0			•			•		CHDSIZ	Z<15:0>	•							0000
2210	ПСЦЗЕПТВ	31:16	—	_	_	_	_	—	_	—	_	-	_	—	_	—	_	_	0000
3310	DOI133FTR	15:0								CHSPT	R<15:0>								0000
3320		31:16	—	—	—	—	—	—	—	—	—	-	—	—	—	—	—	—	0000
3320		15:0								CHDPT	R<15:0>								0000
3330	DCH3CSIZ	31:16	—	—	—	—		—	—	—	—	—	—	—	—	—	—	—	0000
	DONOCOL	15:0								CHCSIZ	Z<15:0>								0000
3340	DCH3CPTR	31:16		—	—	—		—	—	—	—	—	—	—	—	—	_	—	0000
		15:0								CHCPT	R<15:0>								0000
3350	DCH3DAT	31:16	—	_	—	—	_		—	-	—	—	—	-	— T :7 0:	—	—		0000
		15:0	—	_	_	_	_	_	_	_				CHPDA	AT<7:0>				0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	—	—	—	—	—	—			
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—	—	—	—			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	CHSSIZ<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7.0				CHSSIZ	<7:0>						

REGISTER 9-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSSIZ<15:0>: Channel Source Size bits

1111111111111111 = 65,535 byte source size

REGISTER 9-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
	—	—	—	—	—	—	—	—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:10	—	—	—	—	—	—	—	—			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	CHDSIZ<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7.0		CHDSIZ<7:0>									

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0							
31.24	—	_	_	—	—	—	—	—	
22.16	U-0	U-0							
23.10	—	—	—	—	—	—	—	—	
15.0	U-0	U-0							
15.0	—	—	—	—	—	—	—	—	
	R/W-0	R/W-0							
7:0	BISEE	BMYEE		BTOEE			CRC5EE ⁽¹⁾	DIDEE	
	DIGLE	DWIXEE	DWALL	BIOLL	DINOLL	ONCIDEL	EOFEE ⁽²⁾	FIDEE	

REGISTER 10-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7 BTSEE: Bit Stuff Error Interrupt Enable bit
 - 1 = BTSEF interrupt enabled
 - 0 = BTSEF interrupt disabled
- bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
 - 1 = BMXEF interrupt enabled
 - 0 = BMXEF interrupt disabled
- bit 5 **DMAEE:** DMA Error Interrupt Enable bit
 - 1 = DMAEF interrupt enabled
 - 0 = DMAEF interrupt disabled
- bit 4 BTOEE: Bus Turnaround Time-out Error Interrupt Enable bit
 - 1 = BTOEF interrupt enabled
 - 0 = BTOEF interrupt disabled
- bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
 - 1 = DFN8EF interrupt enabled
 - 0 = DFN8EF interrupt disabled
- bit 2 CRC16EE: CRC16 Failure Interrupt Enable bit
 - 1 = CRC16EF interrupt enabled
 - 0 = CRC16EF interrupt disabled
- bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit⁽¹⁾
 - 1 = CRC5EF interrupt enabled
 - 0 = CRC5EF interrupt disabled
 - EOFEE: EOF Error Interrupt Enable bit⁽²⁾
 - 1 = EOF interrupt enabled
 - 0 = EOF interrupt disabled
- bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
 - 1 = PIDEF interrupt enabled
 - 0 = PIDEF interrupt disabled
- Note 1: Device mode.
 - 2: Host mode.

Note: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.

Peripheral Pin	[pin name]R SFR	[<i>pin name</i>]R bits	[<i>pin name</i>]R Value to RPn Pin Selection
INT1	INT1R	INT1R<3:0>	0000 = RPD1 0001 = RPG9
ТЗСК	T3CKR	T3CKR<3:0>	0010 = RPB14 0011 = RPD0
IC1	IC1R	IC1R<3:0>	0100 = RPD8 0101 = RPB6
U3CTS	U3CTSR	U3CTSR<3:0>	0110 = RPD5 0111 = RPB2
U4RX	U4RXR	U4RXR<3:0>	1000 = RPF3 ⁽⁴⁾ 1001 = RPF13 ⁽³⁾
U5RX	U5RXR	U5RXR<3:0>	1010 = Reserved 1011 = RPF2 ⁽¹⁾
SS2	SS2R	SS2R<3:0>	1100 = RPC2 ⁽³⁾ 1101 = RPE8 ⁽³⁾
OCFA	OCFAR	OCFAR<3:0>	1110 = Reserved 1111 = Reserved

TABLE 11-1:INPUT PIN SELECTION (CONTINUED)

Note 1: This selection is not available on 64-pin USB devices.

- 2: This selection is only available on 100-pin General Purpose devices.
- 3: This selection is not available on 64-pin devices.
- 4: This selection is not available when USBID functionality is used on USB devices.
- 5: This selection is not available on devices without a CAN module.
- 6: This selection is not available on USB devices.
- 7: This selection is not available when VBUSON functionality is used on USB devices.

TABLE 11-9: PORTE REGISTER MAP FOR 100-PIN DEVICES ONLY

ess										E	Bits								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	AII Resets
6400	ANSELE	31:16	_	_	—	_	—		—	_	_	—	—	_	_	_	_		0000
0400	ANOLLE	15:0	—	—	—	_	—		ANSELE9	ANSELE8	ANSELE7	ANSELE6	ANSELE5	ANSELE4	_	ANSELE2	ANSELE1	ANSELE0	03F7
6410	TRISE	31:16	—	—	—	—	—	_	—	—	—	—	—	—	—	—	—	_	0000
0110	INICE	15:0	—	—	—	—	—	—	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
6420	PORTE	31:16	—	—	—	—	—	—	—	—	—			—	—	—	—	—	0000
0120	TORRE	15:0	—	—	—	—	—	—	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6440		31:16	—	—	—	—	—		—	_	_		—	_	_	_	_		0000
0440	L/(I L	15:0	—	—	—	_	—		LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6440	ODCE	31:16	_	—	—	—	—	_	—	-	-	_	_	_	—	_	-	_	0000
0440	ODOL	15:0	_	—	—	—	—	_	ODCE9	ODCE8	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000
6450		31:16	_	—	—	—	—	_	—	-	-	_	_	_	—	_	-	_	0000
0400		15:0	_	—	—	—	—	_	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPDE3	CNPUE2	CNPUE1	CNPUE0	0000
6460		31:16	_	—	—	—	—	_	—	-	-	_	_	_	—	_	-	_	0000
0400		15:0	_	—	—	—	—	_	CNPDE9	CNPDE8	CNPDE7	CNPDE6	CNPDE5	CNPDE4	CNPDE3	CNPDE2	CNPDE1	CNPDE0	0000
6470	CNCONE	31:16	_	—	—	—	—	_	—	-	-	_	_	_	—	_	-	_	0000
0470	CINCOME	15:0	ON	_	SIDL	_	—		—	_	_	_	—	_	_	_	_	_	0000
6480		31:16	_	_		_	_		_			_	_						0000
0400	CINEINE	15:0	_	_		_	_		CNIEE9	CNIEE8	CNIEE7	CNIEE6	CNIEE5	CNIEE4	CNIEE3	CNIEE2	CNIEE1	CNIEE0	0000
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6490	CNSTATE	15:0	_	_	_	_	_	_	CN STATE9	CN STATE8	CN STATE7	CN STATE6	CN STATE5	CN STATE4	CN STATE3	CN STATE2	CN STATE1	CN STATE0	0000

Legend: x = Unknown value on Reset; - = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

Control Registers 18.1

TABLE 18-1: I2C1 AND I2C2 REGISTER MAP

ess										Bi	ts								
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5000	120100N	31:16	—	—	—	—	—		—	—	_		_	_	_		—	_	0000
5000	12CTCON	15:0	ON		SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	BFFF
5010		31:16	_		—	—	—	—	—	—		—	—	1		—	—	-	0000
3010	12010171	15:0	ACKSTAT	TRSTAT	—		—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
5020		31:16	_		—		—	—		—	—	—	—	—	—	—	—	—	0000
3020	1201700	15:0	_		—		—	—		-			Address	Register					0000
5030	I2C1MSK	31:16	—	_	—			—			—	—	—	—	_	—	—	_	0000
0000	120110101	15:0	—	_	—	—	—						Address Ma	isk Register					0000
5040	I2C1BRG	31:16	—	_	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0010	1201010	15:0	15:0 — — — Baud Rate Generator Register								0000								
5050	I2C1TRN	31:16	—	_	—	—	—	—		—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—				Transmit	Register				0000
5060	I2C1RCV	31:16	—	_	—	—	—	—		—	—	—	—	—	—	—	—	—	0000
0000	12011101	15:0	—	_	—	—								Receive	Register				0000
5100	12C2CON	31:16	—	_	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0.00		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	BFFF
5110	I2C2STAT	31:16	—	-	—	—	—	—	—	—	-	—	—	-	-	—	—	—	0000
0.10	.2020	15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
5120	I2C2ADD	31:16	—	_	—	—	—	—	-	_	—	—	—	—	—	—	—	—	0000
0.20		15:0	_	_	—	_	—	_					Address	Register					0000
5130	I2C2MSK	31:16	—	_	—	—	—	—	-	_	—	—	—	—	—	—	—	—	0000
0.00		15:0	_	_	-	Address Mask Register									0000				
5140	I2C2BRG	31:16	—	_	—	—	_	—	—	_	—	—	—	—	—	—	—	—	0000
0.10		15:0	_	_	—	_					Βαι	id Rate Ger	nerator Reg	ster					0000
5150	I2C2TRN	31:16	—	_	—	—	—	—		—	_	—	—	—	—	—	—	—	0000
0.00		15:0	_	_	—	—	_	_	—	_		-	-	Transmit	Register	-			0000
5160	I2C2RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0.00	021.07	15:0	—	—		—	—	—	—	—				Receive	Register				0000
Legen	nd: x = unknown value on Reset: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.																		

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x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information. Note 1:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—	—	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	—	—	—	—	—	—		
45.0	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	ON ⁽¹⁾	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN		
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC		
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN		

REGISTER 18-1: I2CxCON: $I^2C'x'$ CONTROL REGISTER ('x' = 1 AND 2)

Legend:	HC = Cleared in Hardware	e	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** I²C Enable bit⁽¹⁾
 - 1 = Enables the I^2C module and configures the SDA and SCL pins as serial port pins
 - 0 = Disables the I²C module; all I²C pins are controlled by PORT functions
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation in Idle mode
 - SCLREL: SCLx Release Control bit (when operating as I²C slave)
 - 1 = Release SCLx clock

bit 12

0 = Hold SCLx clock low (clock stretch)

If STREN = 1:

Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:

Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.

- bit 11 STRICT: Strict I²C Reserved Address Rule Enable bit
 - 1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
 - 0 =Strict I²C Reserved Address Rule not enabled

bit 10 A10M: 10-bit Slave Address bit

- 1 = I2CxADD is a 10-bit slave address
- 0 = I2CxADD is a 7-bit slave address
- bit 9 DISSLW: Disable Slew Rate Control bit
 - 1 = Slew rate control disabled
 - 0 = Slew rate control enabled
- bit 8 SMEN: SMBus Input Levels bit
 - 1 = Enable I/O pin thresholds compliant with SMBus specification
 - 0 = Disable SMBus input thresholds
- **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

20.0 PARALLEL MASTER PORT (PMP)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 13. "Parallel Master Port (PMP)" (DS60001128) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The PMP is a parallel 8-bit or 16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable. The following are the key features of the PMP module:

- 8-bit,16-bit interface
- · Up to 16 programmable address lines
- · Up to two Chip Select lines
- Programmable strobe options:
 - Individual read and write strobes, or
 - Read/write strobe with enable strobe
- Selectable polarity
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support:
 - Legacy addressable
 - Address support
- · Read and Write 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Freeze option for in-circuit debugging

Note: On 64-pin devices, data pins PMD<15:8> are not available in 16-bit Master modes.



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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31.24	FLTEN11	MSEL1	1<1:0>		FSEL11<4:0>						
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23.10	FLTEN10	MSEL1	0<1:0>	FSEL10<4:0>							
15:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15.0	FLTEN9	MSEL	9<1:0>	FSEL9<4:0>							
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7.0	FLTEN8	MSEL	8<1:0>	FSEL8<4:0>							

REGISTER 23-12: C1FLTCON2: CAN FILTER CONTROL REGISTER 2

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	FLTEN11: Filter 11 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 30-29	MSEL11<1:0>: Filter 11 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 28-24	FSEL11<4:0>: FIFO Selection bits
	11111 = Reserved
	•
	•
	• 10000 - Reserved
	01111 = Message matching filter is stored in EIEO buffer 15
	•
	•
	00000 = Message matching filter is stored in FIFO buffer 0
bit 23	FLTEN10: Filter 10 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 22-21	MSEL10<1:0>: Filter 10 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

NOTES:

		-								
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
04.04	R	R	R	R	R	R	R	R		
31:24		VER<	<3:0> ⁽¹⁾		DEVID<27:24> ⁽¹⁾					
00.40	R	R	R	R	R	R	R	R		
23:10	DEVID<23:16> ⁽¹⁾									
45.0	R	R	R	R	R	R	R	R		
15:8				DEVID<	15:8> ⁽¹⁾					
7.0	R	R	R	R	R	R	R	R		
7:0				DEVID<	:7:0>(1)					

REGISTER 28-6: DEVID: DEVICE AND REVISION ID REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 VER<3:0>: Revision Identifier bits⁽¹⁾

bit 27-0 **DEVID<27:0>:** Device ID⁽¹⁾

Note 1: See the "PIC32 Flash Programming Specification" (DS60001145) for a list of Revision and Device ID values.

AC CHARACTERISTICS ⁽²⁾					
ADC Speed	TAD Min.	Sampling Time Min.	Rs Max.	Vdd	ADC Channels Configuration
1 Msps to 400 ksps ⁽¹⁾	65 ns	132 ns	500Ω	3.0V to 3.6V	ANX CHX ADC
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	ANX ADC ANX OF VREF-

TABLE 31-35: 10-BIT CONVERSION RATE PARAMETERS

Note 1: External VREF- and VREF+ pins must be used for correct operation.

2: These parameters are characterized, but not tested in manufacturing.

3: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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