What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx170f512h-i-pt

TABLE 5: PIN NAMES FOR 100-PIN USB DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MX230F128L
PIC32MX530F128L
PIC32MX250F256L
PIC32MX550F256L
PIC32MX270F512L
PIC32MX570F512L

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
71	RPD11/PMA14/RD11	86	V_{DD}
72	RPD0/INT0/RD0	87	AN44/C3INA/RPF0/PMD11/RF0
73	SOSCI/RPC13/RC13	88	AN45/RPF1/PMD10/RF1
74	SOSCO/RPC14/T1CK/RC14	89	RPG1/PMD9/RG1
75	Vss	90	RPG0/PMD8/RG0
76	AN24/RPD1/RD1	91	RA6
77	AN25/RPD2/RD2	92	CTED8/RA7
78	AN26/C3IND/RPD3/RD3	93	AN46/PMD0/RE0
79	AN40/RPD12/PMD12/RD12	94	AN47/PMD1/RE1
80	AN41/PMD13/RD13	95	RG14
81	RPD4/PMWR/RD4	96	RG12
82	RPD5/PMRD/RD5	97	RG13
83	AN42/C3INC/PMD14/RD6	98	AN20/PMD2/RE2
84	AN43/C3INB/PMD15/RD7	99	RPE3/CTPLS/PMD3/RE3
85	V_{CAP}	100	AN21/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

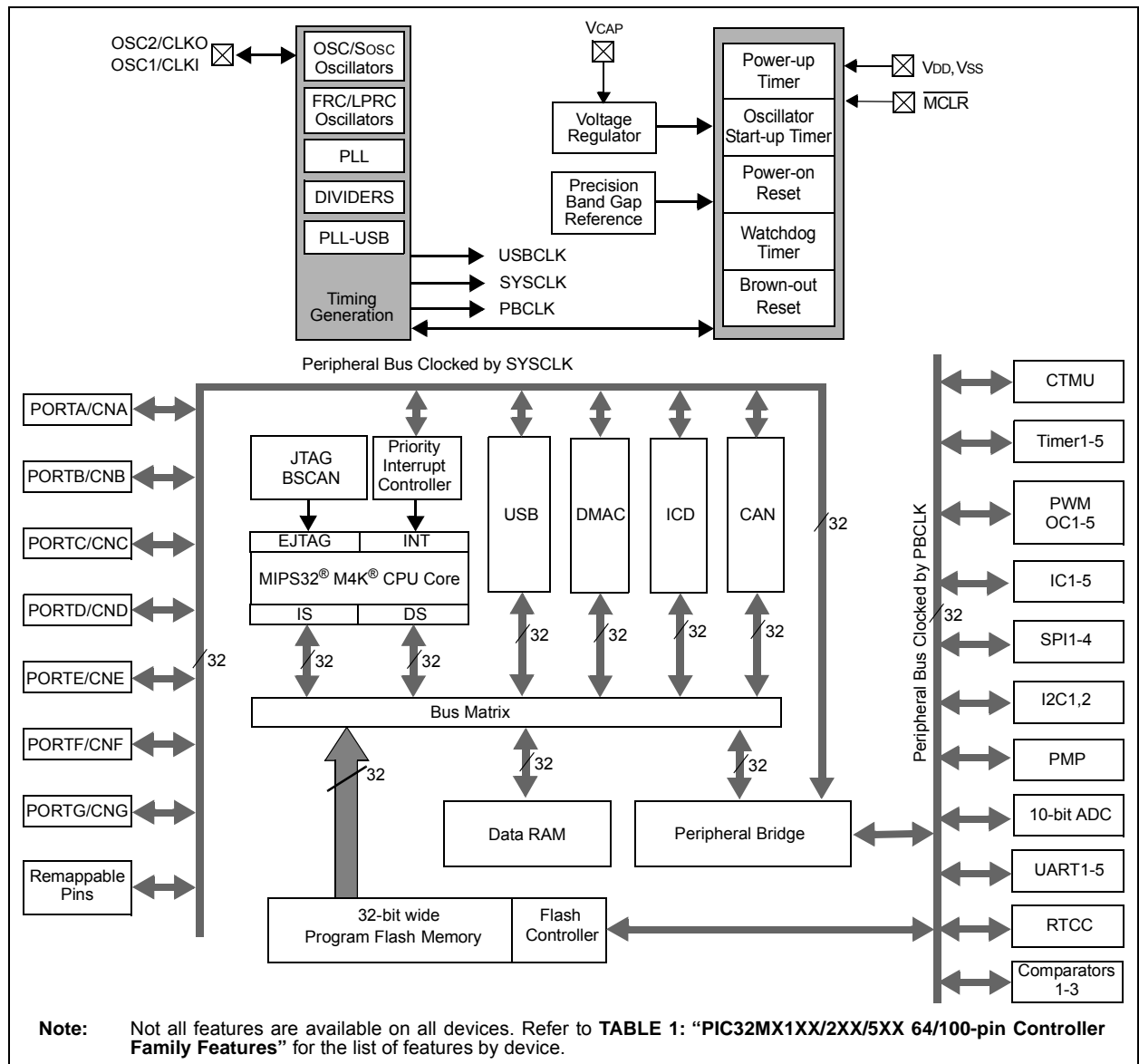# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

1.0   DEVICE OVERVIEW

> **Note 1:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This document contains device-specific information for PIC32MX1XX/2XX/5XX 64/100-pin devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX/5XX 64/100-pin family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1:   **PIC32MX1XX/2XX/5XX 64/100-PIN BLOCK DIAGRAM**

Note: Not all features are available on all devices. Refer to **TABLE 1: "PIC32MX1XX/2XX/5XX 64/100-pin Controller Family Features"** for the list of features by device.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP			
$\overline{MCLR}$	7	13	I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AV$_{DD}$	19	30	P	P	Positive supply for analog modules. This pin must be connected at all times.
AV$_{SS}$	20	31	P	P	Ground reference for analog modules
V$_{DD}$	10, 26, 38, 57	2, 16, 37, 46, 62, 86	P	—	Positive supply for peripheral logic and I/O pins
V$_{CAP}$	56	85	P	—	Capacitor for Internal Voltage Regulator
V$_{SS}$	9, 25, 41	15, 36, 45, 65, 75	P	—	Ground reference for logic and I/O pins
V$_{REF}$+	16	29	P	Analog	Analog Voltage Reference (High) Input
V$_{REF}$-	15	28	P	Analog	Analog Voltage Reference (Low) Input

Legend: CMOS = CMOS compatible input or output   Analog = Analog input   I = Input   O = Output
ST = Schmitt Trigger input with CMOS levels   TTL = TTL input buffer   P = Power

Note 1: This pin is only available on devices without a USB module.
    2: This pin is only available on devices with a USB module.
    3: This pin is not available on 64-pin devices with a USB module.
    4: This pin is only available on 100-pin devices without a USB module.

2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to Vss through a 1k to 10k resistor and configuring the pin as an input.

REGISTER 4-3: **BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDUDBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDUDBA<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUDBA<15:10>:** DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 **BMXDUDBA<9:0>:** Read-Only bits

Value is always '0', which forces 1 KB increments

Note	1:	At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.
	2:	The value in this register must be less than or equal to BMXDRMSZ.

REGISTER 8-1: **OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)**

bit 18-16 **PLLMULT<2:0>:** Phase-Locked Loop (PLL) Multiplier bits

    111 = Clock is multiplied by 24
    110 = Clock is multiplied by 21
    101 = Clock is multiplied by 20
    100 = Clock is multiplied by 19
    011 = Clock is multiplied by 18
    010 = Clock is multiplied by 17
    001 = Clock is multiplied by 16
    000 = Clock is multiplied by 15

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits

    111 = Internal Fast RC (FRC) Oscillator divided by OSCCON<FRCDIV> bits
    110 = Internal Fast RC (FRC) Oscillator divided by 16
    101 = Internal Low-Power RC (LPRC) Oscillator
    100 = Secondary Oscillator (Sosc)
    011 = Primary Oscillator (Posc) with PLL module (XTPLL, HSPLL or ECPLL)
    010 = Primary Oscillator (Posc) (XT, HS or EC)
    001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
    000 = Internal Fast RC (FRC) Oscillator

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits

    111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
    110 = Internal Fast RC Oscillator (FRC) divided by 16
    101 = Internal Low-Power RC (LPRC) Oscillator
    100 = Secondary Oscillator (Sosc)
    011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
    010 = Primary Oscillator (XT, HS or EC)
    001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
    000 = Internal Fast Internal RC Oscillator (FRC)

    On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit

    If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):
    1 = Clock and PLL selections are locked
    0 = Clock and PLL selections are not locked and may be modified

    If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):
    Clock and PLL selections are never locked and may be modified.

bit 6 **ULOCK:** USB PLL Lock Status bit[1]

    1 = Indicates that the USB PLL module is in lock or USB PLL module start-up timer is satisfied
    0 = Indicates that the USB PLL module is out of lock or USB PLL module start-up timer is in progress or USB PLL is disabled

bit 5 **SLOCK:** PLL Lock Status bit

    1 = PLL module is in lock or PLL module start-up timer is satisfied
    0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **SLPEN:** Sleep Mode Enable bit

    1 = Device will enter Sleep mode when a WAIT instruction is executed
    0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit

    1 = FSCM has detected a clock failure
    0 = No clock failure has been detected

Note 1: This bit is available on PIC32MX2XX/5XX devices only.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 8-3: **REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER (CONTINUED)**

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits[1]

    1111 = Reserved; do not use
    •
    •
    •
    1001 = Reserved; do not use
    1000 = REFCLKI
    0111 = System PLL output
    0110 = USB PLL output
    0101 = Sosc
    0100 = LPRC
    0011 = FRC
    0010 = Posc
    0001 = PBCLK
    0000 = SYSCLK

Note 1: The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.

3: While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

REGISTER 9-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
	ON[1]	—	—	SUSPEND	DMABUSY[1]	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** DMA On bit[1]

    1 = DMA module is enabled
    0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **SUSPEND:** DMA Suspend bit

    1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
    0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit[1]

    1 = DMA module is active
    0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DCRCDATA<31:0>:** CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
Bits greater than PLEN will return '0' on any read.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DCRCXOR<31:0>:** CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
1 = Enable the XOR input to the Shift register
0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

REGISTER 9-9: **DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)**

bit 4   **CHDHIF:** Channel Destination Half Full Interrupt Flag bit

     1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
     0 = No interrupt is pending

bit 3   **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit

     1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
     0 = No interrupt is pending

bit 2   **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit

     1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
     0 = No interrupt is pending

bit 1   **CHTAIF:** Channel Transfer Abort Interrupt Flag bit

     1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
     0 = No interrupt is pending

bit 0   **CHERIF:** Channel Address Error Interrupt Flag bit

     1 = A channel address error has been detected
         Either the source or the destination address is invalid.
     0 = No interrupt is pending

REGISTER 18-2:   I2CxSTAT: I²C STATUS REGISTER (CONTINUED)

bit 4   **P:** Stop bit

1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 3   **S:** Start bit

1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 2   **R_W:** Read/Write Information bit (when operating as I²C slave)

1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
Hardware set or clear after reception of I²C device address byte.

bit 1   **RBF:** Receive Buffer Full Status bit

1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty
Hardware set when I2CxRCV is written with received byte. Hardware clear when software
reads I2CxRCV.

bit 0   **TBF:** Transmit Buffer Full Status bit

1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty
Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAITB<1:0>[1]		WAITM<3:0>[1]				WAITE<1:0>[1]	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)

1 = Port is busy
0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits

11 = Reserved, do not use
10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Slave mode only)
01 = Interrupt generated at the end of the read/write cycle
00 = No Interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits

11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)
10 = Decrement ADDR<15:0> by 1 every read/write cycle[2]
01 = Increment ADDR<15:0> by 1 every read/write cycle[2]
00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-bit Mode bit
1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer
0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
11 = Master mode 1 (PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, PMD<7:0> and PMD<8:15>[3])
10 = Master mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, PMD<7:0> and PMD<8:15>[3])
01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>)
00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits[1]
11 = Data wait of 4 T_{PB}; multiplexed address phase of 4 T_{PB}
10 = Data wait of 3 T_{PB}; multiplexed address phase of 3 T_{PB}
01 = Data wait of 2 T_{PB}; multiplexed address phase of 2 T_{PB}
00 = Data wait of 1 T_{PB}; multiplexed address phase of 1 T_{PB} (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 T_{PBCLK} cycle for a write operation; WAITB = 1 T_{PBCLK} cycle, WAITE = 0 T_{PBCLK} cycles for a read operation.

2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

3: These pins are active when MODE16 = 1 (16-bit mode).

REGISTER 21-6: ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<1:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-20 **MONTH10<3:0>:** Binary Coded Decimal value of months bits, 10s place digits; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary Coded Decimal value of days bits, 10s place digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1s place digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary Coded Decimal value of weekdays bits, 1s place digit; contains a value from 0 to 6

REGISTER 23-1: C1CON: CAN MODULE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	S/HC-0	R/W-1	R/W-0	R/W-0
	—	—	—	—	ABAT	REQOP<2:0>		
23:16	R-1	R-0	R-0	R/W-0	U-0	U-0	U-0	U-0
	OPMOD<2:0>			CANCAP	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R-0	U-0	U-0	U-0
	ON(1)	—	SIDLE	—	CANBUSY	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DNCNT<4:0>				

Legend:		
	HC = Hardware Clear	S = Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **ABAT:** Abort All Pending Transmissions bit

    1 = Signal all transmit buffers to abort transmission
    0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits

    111 = Set Listen All Messages mode
    110 = Reserved
    101 = Reserved
    100 = Set Configuration mode
    011 = Set Listen Only mode
    010 = Set Loopback mode
    001 = Set Disable mode
    000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits

    111 = Module is in Listen All Messages mode
    110 = Reserved
    101 = Reserved
    100 = Module is in Configuration mode
    011 = Module is in Listen Only mode
    010 = Module is in Loopback mode
    001 = Module is in Disable mode
    000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit

    1 = CANTMR value is stored on valid message reception and is stored with the message
    0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as '0'

bit 15 **ON:** CAN On bit(1)

    1 = CAN module is enabled
    0 = CAN module is disabled

bit 14 **Unimplemented:** Read as '0'

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

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REGISTER 23-10: C1FLTCON0: CAN FILTER CONTROL REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN3	MSEL3<1:0>		FSEL3<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN2	MSEL2<1:0>		FSEL2<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN1	MSEL1<1:0>		FSEL1<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN0	MSEL0<1:0>		FSEL0<4:0>				

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **FLTEN3:** Filter 3 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL3<1:0>:** Filter 3 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL3<4:0>:** FIFO Selection bits
11111 = Reserved
•
•
•
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
•
•
•
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN2:** Filter 2 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL2<1:0>:** Filter 2 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

Note:	The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

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29.0 INSTRUCTION SET

The PIC32MX1XX/2XX/5XX 64/100-pin family instruction set complies with the MIPS32® Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

> **Note:** Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

FIGURE 31-5: **EXTERNAL RESET TIMING CHARACTERISTICS**
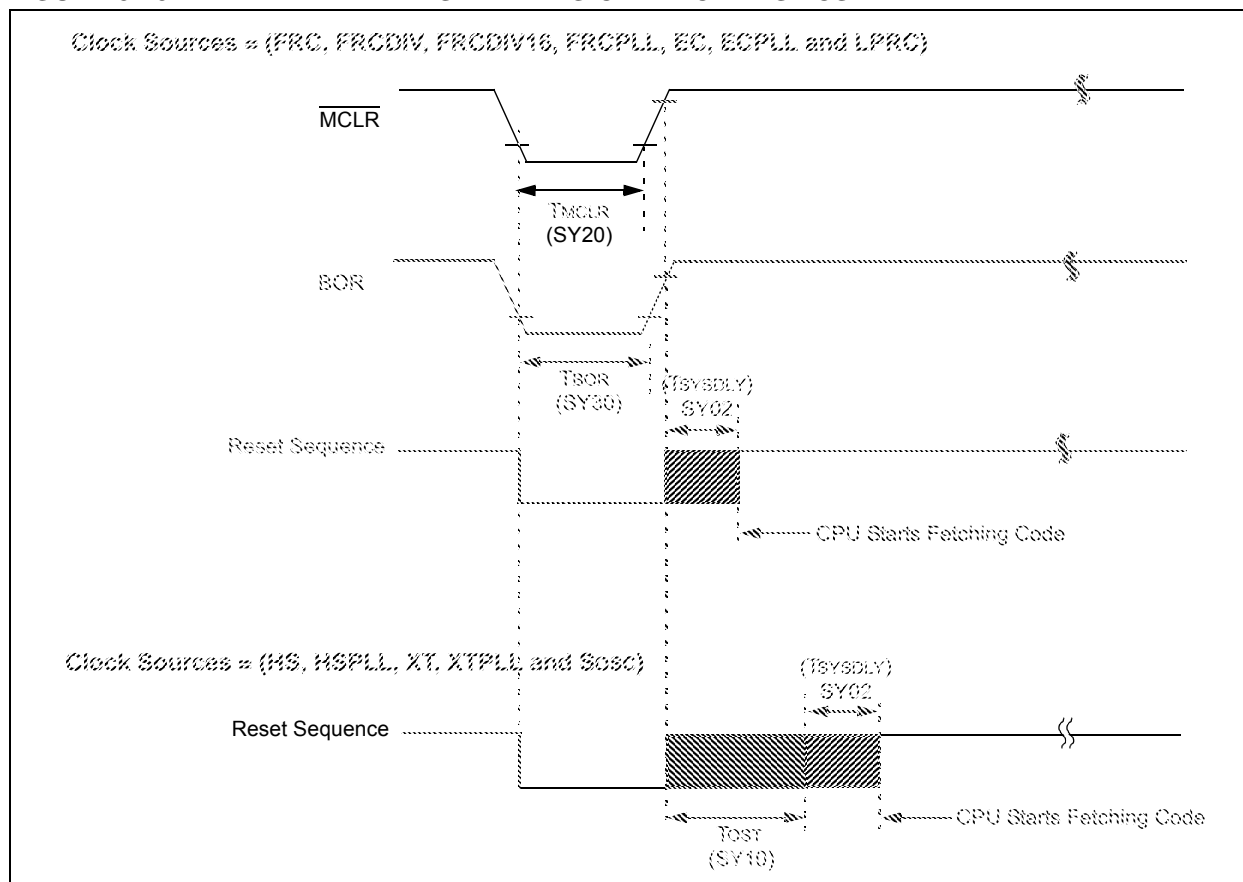
TABLE 31-22: RESETS TIMING

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics[1]	Min.	Typical[2]	Max.	Units	Conditions
SY00	T_{PU}	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μs	—
SY02	T_{SYSDLY}	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.	—	1 μs + 8 SYSCLK cycles	—	—	—
SY20	T_{MCLR}	$\overline{MCLR}$ Pulse Width (low)	2	—	—	μs	—
SY30	T_{BOR}	BOR Pulse Width (low)	—	1	—	μs	—

Note 1: These parameters are characterized, but not tested in manufacturing.
    2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

TABLE 31-36: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical[1]	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period[2]	65	—	—	ns	See Table 31-35
Conversion Rate							
AD55	TCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate (Sampling Speed)	—	—	1000	ksps	AVDD = 3.0V to 3.6V
			—	—	400	ksps	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	1 TAD	—	—	—	TSAMP must be ≥ 132 ns
Timing Parameters							
AD60	TPCS	Conversion Start from Sample Trigger[3]	—	1.0 TAD	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD	—	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1)[3]	—	0.5 TAD	—	—	—
AD63	TDPU	Time to Stabilize Analog Stage from ADC Off to ADC On[3]	—	—	2	µs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

  2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

  3: Characterized by design but not tested.

  4: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 31-38: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp					
Param. No.	Symbol	Characteristics[1]	Min.	Typ.	Max.	Units	Conditions
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPB	—	—	—
PM2	TADSU	Address Out Valid to PMALL/ PMALH Invalid (address setup time)	—	2 TPB	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPB	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPB	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	80	—	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

FIGURE 31-22: PARALLEL MASTER PORT WRITE TIMING DIAGRAM
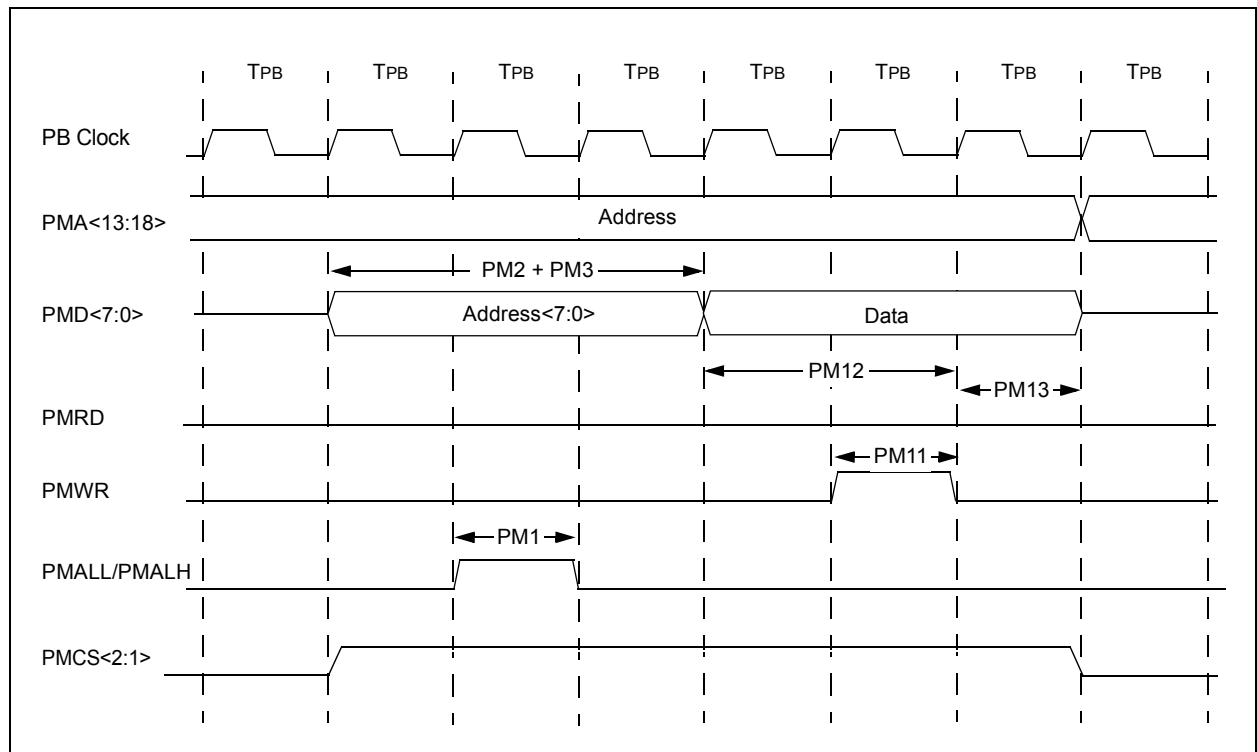
PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
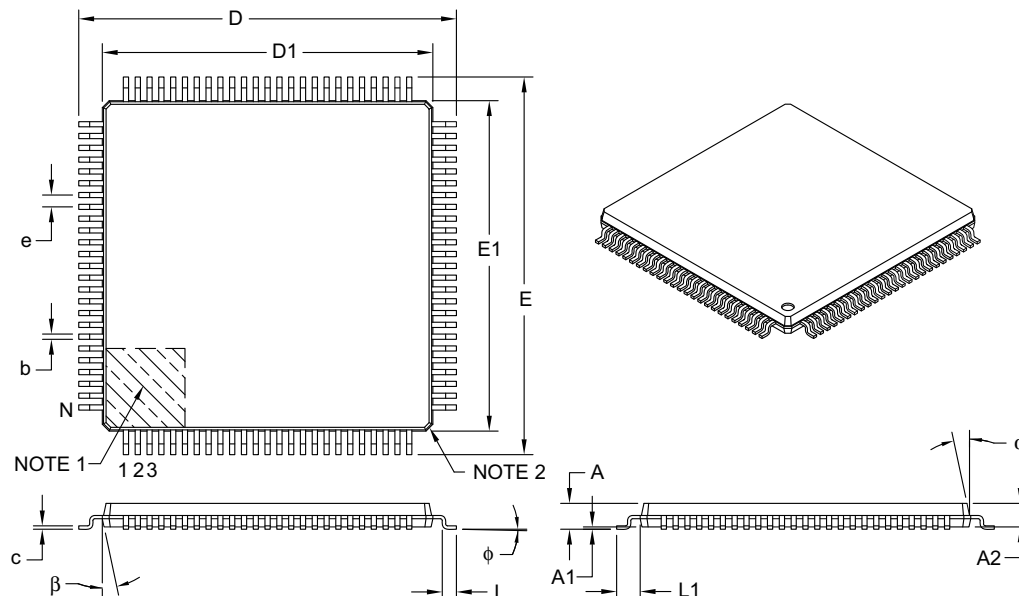
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		16.00 BSC	
Overall Length	D		16.00 BSC	
Molded Package Width	E1		14.00 BSC	
Molded Package Length	D1		14.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B