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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx170f512lt-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 1-1:	PINOUT I/O DESCRIPTIONS ((CONTINUED)	

	Pin N	umber								
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	Pin Type	Buffer Type	Description					
RTCC	42	68	0	—	Real-Time Clock Alarm Output					
CVREFOUT	23	34	0	Analog	Comparator Voltage Reference (Output)					
C1INA	11	20	Ι	Analog						
C1INB	12	21	Ι	Analog	Comportor 1 Innuto					
C1INC	5	11	I	Analog						
C1IND	4	10	I	Analog						
C2INA	13	22	I	Analog						
C2INB	14	23	I	Analog	Comportor 2 Innuito					
C2INC	8	14	I	Analog						
C2IND	6	12	I	Analog	1					
C3INA	58	87	I	Analog						
C3INB	55	84	I	Analog	Comportor 2 Innuito					
C3INC	54	83	I	Analog						
C3IND	51	78	I	Analog						
C10UT	PPS	PPS	0	_	Comparator 1 Output					
C2OUT	PPS	PPS	0	—	Comparator 2 Output					
C3OUT	PPS	PPS	0	_	Comparator 3 Output					
PMALL	30	44	0	TTL/ST	Parallel Master Port Address Latch Enable Low Byte					
PMALH	29	43	0	TTL/ST	Parallel Master Port Address Latch Enable High Byte					
PMA0	30	44	0	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)					
PMA1	29	43	0	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)					
Legend:	CMOS = CN	IOS compati	ible inpu	ut or output	Analog = Analog input I = Input O = Output					

Legend: CMOS = CMOS compatible input or output Analog = Analog input I = Input ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

2.7.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following examples are used to calculate the Primary Oscillator loading capacitor values:

- CIN = PIC32_OSC2_Pin Capacitance = ~4-5 pF
- COUT = PIC32_OSC1_Pin Capacitance = ~4-5 pF
- C1 and C2 = XTAL manufacturing recommended loading capacitance
- Estimated PCB stray capacitance, (i.e.,12 mm length) = 2.5 pF

EXAMPLE 2-1: CRYSTAL LOAD CAPACITOR CALCULATION



The following tips are used to increase oscillator gain, (i.e., to increase peak-to-peak oscillator signal):

- Select a crystal with a lower "minimum" power drive rating
- Select an crystal oscillator with a lower XTAL manufacturing "ESR" rating.
- Add a parallel resistor across the crystal. The smaller the resistor value the greater the gain. It is recommended to stay in the range of 600k to 1M
- C1 and C2 values also affect the gain of the oscillator. The lower the values, the higher the gain.
- C2/C1 ratio also affects gain. To increase the gain, make C1 slightly smaller than C2, which will also help start-up performance.
 - Note: Do not add excessive gain such that the oscillator signal is clipped, flat on top of the sine wave. If so, you need to reduce the gain or add a series resistor, RS, as shown in circuit "C" in Figure 2-4. Failure to do so will stress and age the crystal, which can result in an early failure. Adjust the gain to trim the max peak-to-peak to \sim VDD-0.6V. When measuring the oscillator signal you must use a FET scope probe or a probe with \leq 1.5 pF or the scope probe itself will unduly change the gain and peak-to-peak levels.

2.7.1.1 Additional Microchip References

- AN588 "PICmicro[®] Microcontroller Oscillator Design Guide"
- AN826 "Crystal Oscillator Basics and Crystal Selection for rfPIC[™] and PICmicro[®] Devices"
- AN849 "Basic PICmicro[®] Oscillator Design"



3.0 CPU

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 2. "CPU" (DS60001113) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32). Resources for the MIPS32[®] M4K[®] Processor Core are available at http://www.imgtec.com.

The the MIPS32[®] M4K[®] Processor Core is the heart of the PIC32MX1XX/2XX/5XX 64/100-pin device processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

3.1 Features

- 5-stage pipeline
- · 32-bit address and data paths
- MIPS32[®] Enhanced Architecture (Release 2):
 - Multiply-accumulate and multiply-subtract instructions
 - Targeted multiply instruction
 - Zero/One detect instructions
 - WAIT instruction
 - Conditional move instructions (MOVN, MOVZ)
 - Vectored interrupts
 - Programmable exception vector base
 - Atomic interrupt enable/disable
 - Bit field manipulation instructions

- MIPS16e[®] Code Compression:
 - 16-bit encoding of 32-bit instructions to improve code density
 - Special PC-relative instructions for efficient loading of addresses and constants
 - SAVE and RESTORE macro instructions for setting up and tearing down stack frames within subroutines
 - Improved support for handling 8 and 16-bit data types
- Simple Fixed Mapping Translation (FMT) Mechanism:
- Simple Dual Bus Interface:
 - Independent 32-bit address and data buses
 - Transactions can be aborted to improve interrupt latency
- Autonomous Multiply/Divide Unit (MDU):
 - Maximum issue rate of one 32x16 multiply per clock
 - Maximum issue rate of one 32x32 multiply every other clock
 - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (*rs*) sign extension-dependent)
- Power Control:
 - Minimum frequency: 0 MHz
 - Low-Power mode (triggered by WAIT instruction)
 - Extensive use of local gated clocks
- EJTAG Debug:
 - Support for single stepping
 - Virtual instruction and data address/value
 - Breakpoints

FIGURE 3-1: MIPS32[®] M4K[®] PROCESSOR CORE BLOCK DIAGRAM



Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

Exception	Description
Reset	Assertion MCLR or a Power-on Reset (POR).
DSS	EJTAG debug single step.
DINT	EJTAG debug interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input or by setting the EjtagBrk bit in the ECR register.
NMI	Assertion of NMI signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
DIB	EJTAG debug hardware instruction break matched.
AdEL	Fetch address alignment error. Fetch reference to protected address.
IBE	Instruction fetch bus error.
DBp	EJTAG breakpoint (execution of SDBBP instruction).
Sys	Execution of SYSCALL instruction.
Вр	Execution of BREAK instruction.
RI	Execution of a reserved instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a CorExtend instruction when CorExtend is not enabled.
Ov	Execution of an arithmetic instruction that overflowed.
Tr	Execution of a trap (when trap condition is true).
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
DBE	Load or store bus error.
DDBL	EJTAG data hardware breakpoint matched in load data compare.

TABLE 3-3: MIPS32[®] M4K[®] PROCESSOR CORE EXCEPTION TYPES

3.3 **Power Management**

The MIPS[®] M4K[®] processor core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see Section 27.0 "Power-Saving Features".

3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the PIC32MX-1XX/2XX/5XX 64/100-pin family core is in the clock tree and clocking registers. The PIC32MX family uses extensive use of local gated-clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The MIPS[®] M4K[®] processor core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K[®] core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

5.0 INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS60001108) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The PIC32MX1XX/2XX/5XX 64/100-pin interrupt module includes the following features:

- Up to 76 interrupt sources
- Up to 46 interrupt vectors
- · Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Software can generate any interrupt
- User-configurable interrupt vector table location
- User-configurable interrupt vector spacing

Note: The dedicated shadow register set is not available on these devices.



FIGURE 5-1: INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM

6.1 Control Registers

TABLE 6-1: FLASH CONTROLLER REGISTER MAP

ess		0								Bi	ts								ú
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
E400		31:16		—	—	—								_	—	—	_		0000
1400	NVINCON /	15:0	WR	WR WREN WRERR LVDERR LVDSTAT NVMOP<3:0>								0000							
E410		31:16									V~31·0>								0000
1410		15:0									1~51.02								0000
E420		31:16									D-31.05								0000
1420	NVINADDR	15:0								NVINADL	///////////////////////////////////////								0000
E420		31:16									A-21.0>								0000
1430	NUMDAIA	15:0								NVINDAI	A-31.02								0000
E440	NVMSRC	31:16																	0000
F440	ADDR	15:0								NUNISRCA	JDK~31.02								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
51.24	—	—	—	—		—		—	
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	-	—	-	—	
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15.0	—	—	—	—		—		—	
7.0	R/WC-0, HS	U-0	R/WC-0, HS						
7:0	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	_	VBUSVDIF	

REGISTER 10-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Legend:	WC = Write '1' to clear	HS = Hardware Settable b	bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7 IDIF: ID State Change Indicator bit
 - 1 = Change in ID state detected
 - 0 = No change in ID state detected
- bit 6 T1MSECIF: 1 Millisecond Timer bit
 - 1 = 1 millisecond timer has expired
 - 0 = 1 millisecond timer has not expired

bit 5 LSTATEIF: Line State Stable Indicator bit

- 1 = USB line state has been stable for 1millisecond, but different from last time
- 0 = USB line state has not been stable for 1 millisecond

bit 4 ACTVIF: Bus Activity Indicator bit

- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected
- bit 3 SESVDIF: Session Valid Change Indicator bit
 - 1 = VBUS voltage has dropped below the session end level
 - 0 = VBUS voltage has not dropped below the session end level
- bit 2 SESENDIF: B-Device VBUS Change Indicator bit
 - 1 = A change on the session end input was detected
 - 0 = No change on the session end input was detected
- bit 1 Unimplemented: Read as '0'
- bit 0 VBUSVDIF: A-Device VBUS Change Indicator bit
 - 1 = Change on the session valid input detected
 - 0 = No change on the session valid input detected

12.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). This family of PIC32 devices features one synchronous/ asynchronous 16-bit timer that can operate as a freerunning interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (Sosc) for Real-Time Clock (RTC) applications. The following modes are supported:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

12.1 Additional Supported Features

- · Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the Sosc to function as a Real-Time Clock (RTC)



FIGURE 12-1: TIMER1 BLOCK DIAGRAM

REGISTER 13-1: TxCON: TYPE B TIMER 'x' CONTROL REGISTER ('x' = 2 THROUGH 5)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—		—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	_	_	_		_	_
15.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
15.0	ON ^(1,3)	—	SIDL ⁽⁴⁾	—	—	-	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
7.0	TGATE ⁽³⁾	Т	CKPS<2:0>(3)	T32 ⁽²⁾	_	TCS ⁽³⁾	_

Legena:	I	_ec	jei	nd	:
---------	---	-----	-----	----	---

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Timer On bit^(1,3)
 - 1 = Module is enabled 0 = Module is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit⁽⁴⁾
 - 1 = Discontinue operation when device enters Idle mode
 - 0 = Continue operation even in Idle mode
- bit 12-8 Unimplemented: Read as '0'
- bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit⁽³⁾

When TCS = 1:

This bit is ignored and is read as '0'.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

- bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits⁽³⁾
 - 111 = 1:256 prescale value
 - 110 = 1:64 prescale value
 - 101 = 1:32 prescale value
 - 100 = 1:16 prescale value
 - 011 = 1:8 prescale value
 - 010 = 1:4 prescale value
 - 001 = 1:2 prescale value
 - 000 = 1:1 prescale value
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - **2:** This bit is available only on even numbered timers (Timer2 and Timer4).
 - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3 and Timer5). All timer functions are set through the even numbered timers.
 - 4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

REGISTER 19-1: UXMODE: UARTX MODE REGISTER (CONTINUED)

bit 5	 ABAUD: Auto-Baud Enable bit 1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion 0 = Baud rate measurement disabled or completed
bit 4	RXINV: Receive Polarity Inversion bit 1 = UxRX Idle state is '0' 0 = UxRX Idle state is '1'
bit 3	 BRGH: High Baud Rate Enable bit 1 = High-Speed mode – 4x baud clock enabled 0 = Standard Speed mode – 16x baud clock enabled
bit 2-1	<pre>PDSEL<1:0>: Parity and Data Selection bits 11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity</pre>
bit 0	STSEL: Stop Selection bit 1 = 2 Stop bits 0 = 1 Stop bit

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—	—	—	—	
45.0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	BUSY	IRQM	<1:0>	INCM	<1:0>	MODE16	MODE	=<1:0>	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	WAITB	<1:0>(1)		WAITM	<3:0>(1)		WAITE<1:0>(1)		

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER

Legend:

•			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **BUSY:** Busy bit (Master mode only)
 - 1 = Port is busy
 - 0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits

- 11 = Reserved, do not use
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Slave mode only)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No Interrupt generated
- bit 12-11 INCM<1:0>: Increment Mode bits
 - 11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)
 - 10 = Decrement ADDR<15:0> by 1 every read/write cycle⁽²⁾
 - 01 = Increment ADDR<15:0> by 1 every read/write cycle⁽²⁾
 - 00 = No increment or decrement of address
- bit 10 **MODE16:** 8/16-bit Mode bit
 - 1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer
 - 0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer
- bit 9-8 MODE<1:0>: Parallel Port Mode Select bits
 - 11 = Master mode 1 (PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, PMD<7:0> and PMD<8:15>⁽³⁾)
 - 10 = Master mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, PMD<7:0> and PMD<8:15>⁽³⁾)
 - 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>)
 - 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS and PMD<7:0>)

bit 7-6 WAITB<1:0>: Data Setup to Read/Write Strobe Wait States bits⁽¹⁾

- 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
- 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
- 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
- 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)
- **Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.
 - 2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.
 - 3: These pins are active when MODE16 = 1 (16-bit mode).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	-	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	_	—	—	—	—	—
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	PTEN<1	5:14> ⁽¹⁾						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTEN	<7:2>			PTEN<	<1:0> ⁽²⁾

REGISTER 20-6: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

Legend:

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Write '0'; ignore read

- bit 15-14 **PTEN<15:14>:** PMCSx Address Port Enable bits
 - 1 = PMA15 and PMA14 function as either PMA<15:14> or PMCS2 and PMCS1⁽¹⁾
 - 0 = PMA15 and PMA14 function as port I/O
- bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
 - 1 = PMA<13:2> function as PMP address lines
 - 0 = PMA<13:2> function as port I/O
- bit 1-0 **PTEN<1:0>:** PMALH/PMALL Address Port Enable bits
 - 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL⁽²⁾
 - 0 = PMA1 and PMA0 pads function as port I/O
- Note 1: The use of these pins as PMA15/PMA14 or CS2/CS1 is selected by the CSF<1:0> bits (PMCON<7:6>).
 - 2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by the ADRMUX<1:0> bits in the PMCON register.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R-0	R/W-0, HSC	U-0	U-0	R-0	R-0	R-0	R-0
15:8	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7.0	R-1	R/W-0, HSC	U-0	U-0	R-1	R-1	R-1	R-1
7:0	OBE	OBUF	—	_	OB3E	OB2E	OB1E	OB0E

REGISTER 20-7: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Legend:	HSC = Set by Hardware; Cleared by Software				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-16 Unimplemented: Read as '0'

- bit 15 IBF: Input Buffer Full Status bit
 - 1 = All writable input buffer registers are full
 - 0 = Some or all of the writable input buffer registers are empty
- bit 14 IBOV: Input Buffer Overflow Status bit
 - 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
 0 = No overflow occurred
- bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits

- 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input Buffer does not contain any unread data
- bit 7 OBE: Output Buffer Empty Status bit
 - 1 = All readable output buffer registers are empty
 - 0 = Some or all of the readable output buffer registers are full
- bit 6 **OBUF:** Output Buffer Underflow Status bit
 - 1 = A read occurred from an empty output byte buffer (must be cleared in software)
- 0 = No underflow occurred bit 5-4 **Unimplemented:** Read as '0'
- bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits
 - 1 = Output buffer is empty (writing data to the buffer will clear this bit)
 - 0 = Output buffer contains data that has not been transmitted

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	_	—	—	—	—	—	—	—			
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—	—	—	—			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	RDATAIN<15:8>										
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	RDATAIN<7:0>										

REGISTER 20-10: PMRDIN: PARALLEL PORT READ INPUT DATA REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 **RDATAIN<15:0>:** Port Read Input Data bits

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to '1' and exclusively for reads. If the DUALBUF bit is '0', the PMDIN register (Register 20-5) is used for reads instead of PMRDIN.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTEN7		MSEL7<1:0>			F	SEL7<4:0>		
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	FLTEN6	MSEL6<1:0>		FSEL6<4:0>				
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	FLTEN5	MSEL	5<1:0>	FSEL5<4:0>				
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	FLTEN4	MSEL	4<1:0>		F	SEL4<4:0>		

REGISTER 23-11: C1FLTCON1: CAN FILTER CONTROL REGISTER 1

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	FLTEN7: Filter 7 Enable bit
	1 = Filter is enabled0 = Filter is disabled
bit 30-29	MSEL7<1:0>: Filter 7 Mask Select bits
	 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 28-24	FSEL7<4:0>: FIFO Selection bits
	11111 = Reserved
	•
	10000 = Reserved
	01111 = Message matching filter is stored in FIFO buffer 15
	•
	•
	00000 = Message matching filter is stored in FIFO buffer 0
bit 23	FLTEN6: Filter 6 Enable bit
	1 = Filter is enabled0 = Filter is disabled
bit 22-21	MSEL6<1:0>: Filter 6 Mask Select bits
	11 = Acceptance Mask 3 selected

- - 10 = Acceptance Mask 2 selected
 - 01 = Acceptance Mask 1 selected
 - 00 = Acceptance Mask 0 selected

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

25.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

This data sheet summarizes the features Note: of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 20. "Comparator Voltage Reference (CVREF)" (DS60001109) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them. A block diagram of the module is illustrated in Figure 25-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/Vss or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The CVREF module has the following features:

- High and low range selection
- · Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- · Output can be connected to a pin



FIGURE 25-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- · On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

27.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

- Note 1: Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a Posc of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.
 - 2: Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from Posc to LPRC just prior to entering Sleep in order to save power. No oscillator startup delay would be applied when exiting Idle. However, when switching back to Posc, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a WAIT instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

27.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The peripheral bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

DC CHARACT	ERISTICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Parameter No.	Typical ⁽²⁾	Max.	Units Conditions					
Idle Current (IIDLE): Core Off, Clock on Base Current (Notes 1, 4)								
DC30a	1.5	5	mA	4 MHz (Note 3)				
DC31a	3	8	mA		10 MHz			
DC32a	5	12	mA		20 MHz (Note 3)			
DC33a	6.5	15	mA		30 MHz (Note 3)			
DC34a	8	20	mA		40 MHz			
DC37a	75	100	μA	-40°C LPF +25°C 3.3V +85°C 3.3V		LPRC (31 kHz)		
DC37b	180	250	μA			(Note 3)		
DC37c	280	380	μA					

TABLE 31-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

Note 1: The test conditions for IIDLE current measurements are as follows:

Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 OSC2/CLKO is configured as an I/O input pin

- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1 $\,$
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD
- RTCC and JTAG are disabled
- 2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3: This parameter is characterized, but not tested in manufacturing.
- 4: IIDLE electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions	
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	_	μS	PBCLK must operate at a minimum of 800 kHz	
			400 kHz mode	1.3	_	μS	PBCLK must operate at a minimum of 3.2 MHz	
			1 MHz mode (Note 1)	0.5	_	μS	_	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μS	PBCLK must operate at a minimum of 800 kHz	
			400 kHz mode	0.6	—	μS	PBCLK must operate at a minimum of 3.2 MHz	
			1 MHz mode (Note 1)	0.5	_	μS		
IS20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be from	
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode (Note 1)	—	100	ns		
IS21	TR:SCL	SDAx and SCLx	100 kHz mode	—	1000	ns	CB is specified to be from	
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode (Note 1)	—	300	ns		
IS25	TSU:DAT	Data Input	100 kHz mode	250	—	ns	—	
		Setup Time	400 kHz mode	100	—	ns		
			1 MHz mode (Note 1)	100	_	ns		
IS26	THD:DAT	Data Input	100 kHz mode	0	—	ns	—	
		Hold Time	400 kHz mode	0	0.9	μs		
			1 MHz mode (Note 1)	0	0.3	μS		
IS30	TSU:STA	Start Condition	100 kHz mode	4700	—	ns	Only relevant for Repeated	
		Setup Time	400 kHz mode	600	—	ns	Start condition	
			1 MHz mode (Note 1)	250	_	ns		
IS31	THD:STA	Start Condition	100 kHz mode	4000		ns	After this period, the first	
		Hold Time	400 kHz mode	600	_	ns	clock pulse is generated	
			1 MHz mode (Note 1)	250	—	ns		
IS33	Tsu:sto	Stop Condition	100 kHz mode	4000	—	ns	_	
		Setup Time	400 kHz mode	600	—	ns]	
			1 MHz mode (Note 1)	600		ns		

TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

32.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX/5XX 64/100-pin AC characteristics and timing parameters.

TABLE 32-5:	EXTERNAL CLOCK TIMING REQUIREMENTS
TABLE 32-5:	EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
MOS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4		50 50	MHz MHz	EC (Note 2) ECPLL (Note 1)

Note 1: PLL input requirements: $4 \text{ MHz} \le \text{FPLLIN} \le 5 \text{ MHz}$ (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.

2: This parameter is characterized, but not tested in manufacturing.

TABLE 32-6: SPIX MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
Param. No.	Symbol	Characteristics	Min.	Typical Max. Units Conditio			
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	_	—	ns	_
MSP11	TscH	SCKx Output High Time (Note 1,2)	Тѕск/2		—	ns	_

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

TABLE 32-7:	SPIX MODULE MASTER MODE	(CKE = 1)	TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min. Typ. Max. Units Conditions				
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	—		ns	_
MSP11	TscH	SCKx Output High Time (Note 1,2)	Тѕск/2	—		ns	_

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.