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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT |
| Number of I/O | 81 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 48x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx230f128lt-50i-pf |

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 4-4: BMXDUPBA: DATA RAM USER PROGRAM BASE ADDRESS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 |
| | BMXDUPBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXDUPBA<7:0> | | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUPBA<15:10>:** DRM User Program Base Address bits

When non-zero, the value selects the relative base address for User mode program space in RAM, BMXDUPBA must be greater than BMXDUDBA.

bit 9-0 **BMXDUPBA<9:0>:** Read-Only bits

Value is always '0', which forces 1 KB increments

- Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.
- 2:** The value in this register must be less than or equal to BMXDRMSZ.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 5-1: INTCON: INTERRUPT CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 31:24 | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — |
| 23:16 | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — | U-0 — |
| 15:8 | U-0 — | U-0 — | U-0 — | R/W-0 MVEC | U-0 — | R/W-0 — | R/W-0 — | R/W-0 — |
| 7:0 | U-0 — | U-0 — | U-0 — | R/W-0 INT4EP | R/W-0 INT3EP | R/W-0 INT2EP | R/W-0 INT1EP | R/W-0 INT0EP |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multi Vector Configuration bit

1 = Interrupt controller configured for multi vectored mode

0 = Interrupt controller configured for single vectored mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits

111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer

110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer

101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer

100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer

011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer

010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer

001 = Interrupts of group priority 1 start the Interrupt Proximity timer

000 = Disables Interrupt Proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit

1 = Rising edge

0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit

1 = Rising edge

0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit

1 = Rising edge

0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit

1 = Rising edge

0 = Falling edge

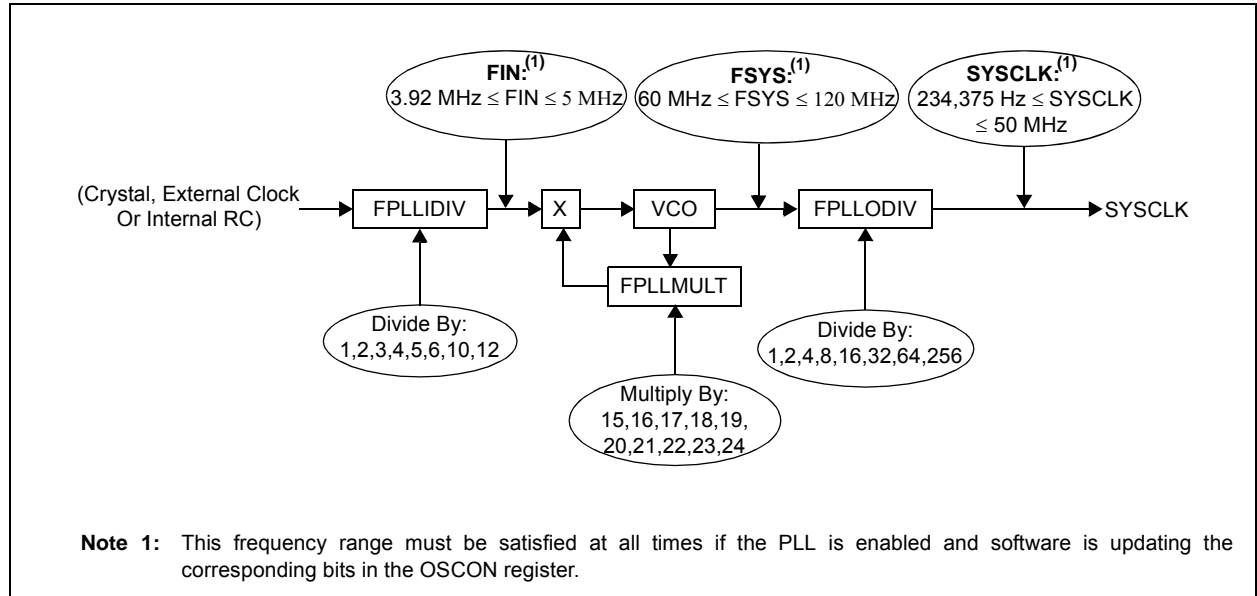
bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit

1 = Rising edge

0 = Falling edge

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

FIGURE 8-2: PIC32MX1XX/2XX/5XX PLL BLOCK DIAGRAM



8.1 Control Registers

TABLE 8-1: OSCILLATOR CONFIGURATION REGISTER MAP

| Virtual Address (BF80_#) | Register Name ⁽¹⁾ | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets | |
|-----------------------------|---------------------------------|-----------|-------------|-------------|--------------|-------|-------|-------------|---------|--------|---------|---------|----------|------------|------------|-----------------------|--------|-------|---------------------|------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | | |
| F000 | OSCCON | 31:16 | — | — | PLLODIV<2:0> | | | FRCDIV<2:0> | | | — | SOSCRDY | PBDIVRDY | PBDIV<1:0> | | PLLMULT<2:0> | | | x1xx ⁽²⁾ | |
| | | 15:0 | — | COSC<2:0> | | | — | NOSC<2:0> | | | CLKLOCK | ULOCK | SLOCK | SLPEN | CF | UFRGEN ⁽³⁾ | SOSCEN | OSWEN | xxxx ⁽²⁾ | |
| F010 | OSCTUN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | TUN<5:0> | | | | | | | 0000 |
| F020 | REFOCON | 31:16 | — | RODIV<14:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | ON | — | SIDL | OE | RSLP | — | DIVSWEN | ACTIVE | — | — | — | — | ROSEL<3:0> | | | | 0000 | |
| F030 | REFOTRIM | 31:16 | ROTRIM<8:0> | | | | | | | | | | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 | |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2** “CLR, SET, and INV Registers” for more information.
- 2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.
- 3:** This bit is only available on devices with a USB module.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 9-5: DCRCDATA: DMA CRC DATA REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DCRCDATA<31:24> | | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DCRCDATA<23:16> | | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DCRCDATA<15:8> | | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DCRCDATA<7:0> | | | | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **DCRCDATA<31:0>**: CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Bits greater than PLEN will return '0' on any read.

REGISTER 9-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DCRCXOR<31:24> | | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DCRCXOR<23:16> | | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DCRCXOR<15:8> | | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DCRCXOR<7:0> | | | | | | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **DCRCXOR<31:0>**: CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = Enable the XOR input to the Shift register

0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

11.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. “I/O Ports”** (DS60001120) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

General purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate functions. These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

The following are the key features of this module:

- Individual output pin open-drain enable or disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

Figure 11-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE

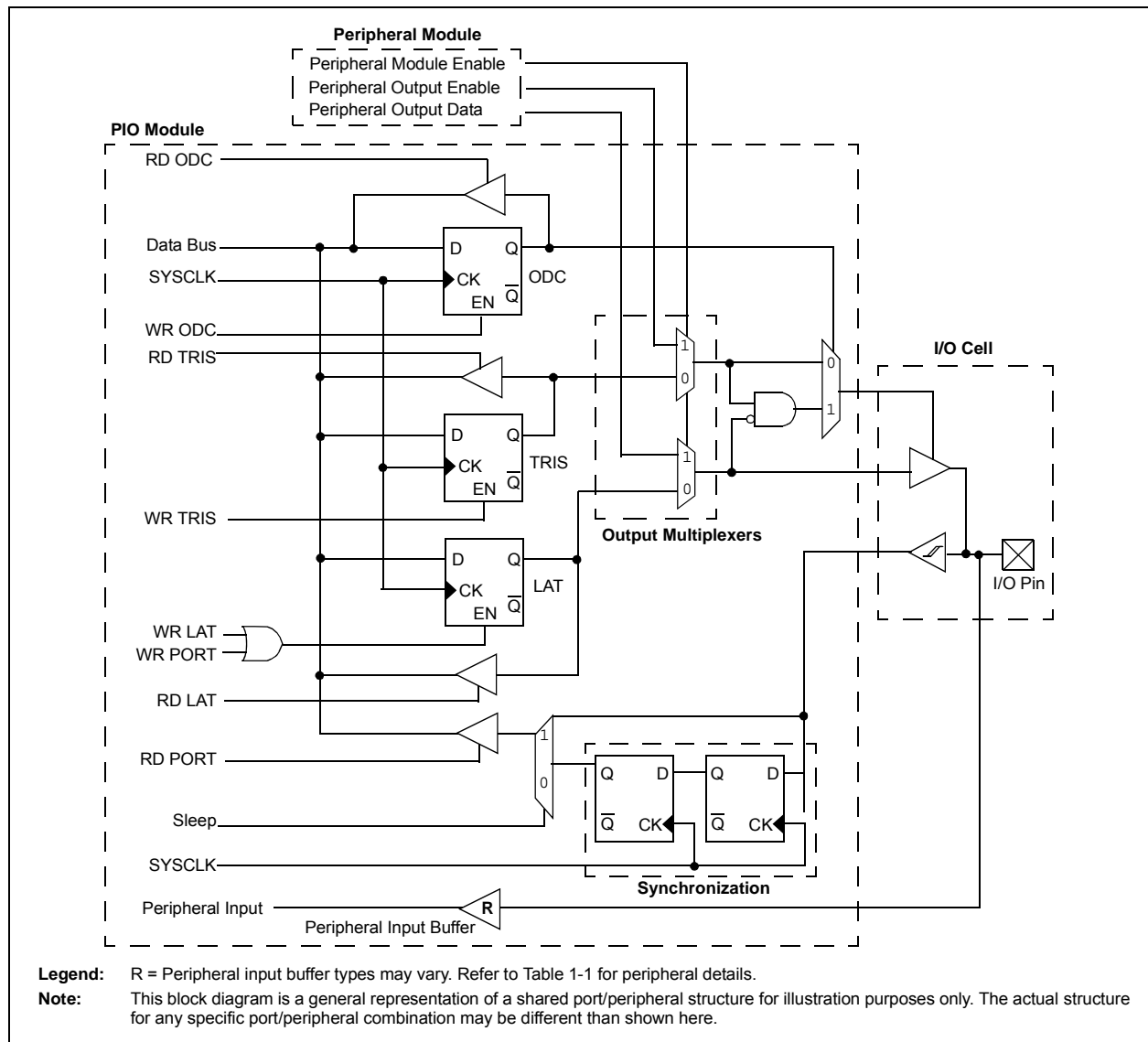


TABLE 11-17: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|-----------------------------|------------------|-----------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|---------------|------|------|------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| FA5C | U2CTSR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U2CTSR<3:0> | | | | 0000 |
| FA60 | U3RXR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U3RXR<3:0> | | | | 0000 |
| FA64 | U3CTSR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U3CTSR<3:0> | | | | 0000 |
| FA68 | U4RXR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U4RXR<3:0> | | | | 0000 |
| FA6C | U4CTSR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U4CTSR<3:0> | | | | 0000 |
| FA70 | U5RXR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U5RXR<3:0> | | | | 0000 |
| FA74 | U5CTSR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | U5CTSR<3:0> | | | | 0000 |
| FA84 | SDI1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SDI1R<3:0> | | | | 0000 |
| FA88 | SS1R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SS1R<3:0> | | | | 0000 |
| FA90 | SDI2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SDI2R<3:0> | | | | 0000 |
| FA94 | SS2R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SS2R<3:0> | | | | 0000 |
| FA9C | SDI3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SDI3R<3:0> | | | | 0000 |
| FAA0 | SS3R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SS3R<3:0> | | | | 0000 |
| FAA8 | SDI4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SDI4R<3:0> | | | | 0000 |
| FAAC | SS4R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | SS4R<3:0> | | | | 0000 |
| FAC8 | C1RXR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | C1RXR<3:0> | | | | 0000 |
| FAD0 | REFCLKIR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | REFCLKIR<3:0> | | | | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 18-2: I2CxSTAT: I²C STATUS REGISTER (CONTINUED)

- bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.
- bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.
- bit 2 **R_W:** Read/Write Information bit (when operating as I²C slave)
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
Hardware set or clear after reception of I²C device address byte.
- bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty
Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.
- bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty
Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

19.1 Control Registers

TABLE 19-1: UART1 THROUGH UART5 REGISTER MAP

| Virtual Address (BF80-#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|-----------------------------|-----------------------|-----------|--------------|-------|--------|-------|--------|-------|----------|--------|------|--------------|-------|-------|------|------------|-------|-------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6000 | U1MODE ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | — | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | STSEL | — | 0000 |
| 6010 | U1STA ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | ADM_EN | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | UTXISEL<1:0> | — | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | — | URXISEL<1:0> | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | FFFF |
| 6020 | U1TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | — | — | — | — | — | — | — | — | 0000 |
| 6030 | U1RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | — | — | — | — | — | — | — | — | 0000 |
| 6040 | U1BRG ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6200 | U2MODE ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | — | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | STSEL | — | 0000 |
| 6210 | U2STA ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | ADM_EN | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | UTXISEL<1:0> | — | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | — | URXISEL<1:0> | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | FFFF |
| 6220 | U2TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | — | — | — | — | — | — | — | — | 0000 |
| 6230 | U2RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | — | — | — | — | — | — | — | — | 0000 |
| 6240 | U2BRG ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6400 | U3MODE ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | — | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | STSEL | — | 0000 |
| 6410 | U3STA ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | ADM_EN | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | UTXISEL<1:0> | — | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | — | URXISEL<1:0> | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | FFFF |
| 6420 | U3TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | — | — | — | — | — | — | — | — | 0000 |
| 6430 | U3RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | — | — | — | — | — | — | — | — | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.
- 2: This register is only available on 100-pin devices.

TABLE 19-1: UART1 THROUGH UART5 REGISTER MAP (CONTINUED)

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|-----------------------------|--------------------------|-----------|-------------------------------|-------|--------|-------|--------|-------|----------|--------|-------------------|--------|-------|-------|------|------------|------|-------|------------|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6440 | U3BRG ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| 6600 | U4MODE ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6610 | U4STA ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | FFFF |
| 6620 | U4TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6630 | U4RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6640 | U4BRG ⁽¹⁾ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| 6800 | U5MODE ^(1,2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6810 | U5STA ^(1,2) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | FFFF |
| 6820 | U5TXREG ^(1,2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6830 | U5RXREG ^(1,2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6840 | U5BRG ^(1,2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.
- 2: This register is only available on 100-pin devices.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 19-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 5 **ABAUD**: Auto-Baud Enable bit
 1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55);
 cleared by hardware upon completion
 0 = Baud rate measurement disabled or completed
- bit 4 **RXINV**: Receive Polarity Inversion bit
 1 = UxRX Idle state is '0'
 0 = UxRX Idle state is '1'
- bit 3 **BRGH**: High Baud Rate Enable bit
 1 = High-Speed mode – 4x baud clock enabled
 0 = Standard Speed mode – 16x baud clock enabled
- bit 2-1 **PDSEL<1:0>**: Parity and Data Selection bits
 11 = 9-bit data, no parity
 10 = 8-bit data, odd parity
 01 = 8-bit data, even parity
 00 = 8-bit data, no parity
- bit 0 **STSEL**: Stop Selection bit
 1 = 2 Stop bits
 0 = 1 Stop bit

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 23-17: C1FIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('n' = 0 THROUGH 15)

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|--------------------------|-------------------------|---------------------------|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | TXNFULLIE | TXHALFIE | TXEMPTYIE |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | RXOVFLIE | RXFULLIE | RXHALFIE | RXNEMPTYIE |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | — | TXNFULLIF ⁽¹⁾ | TXHALFIF | TXEMPTYIF ⁽¹⁾ |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | RXOVFLIF | RXFULLIF ⁽¹⁾ | RXHALFIF ⁽¹⁾ | RXNEMPTYIF ⁽¹⁾ |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit

1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit

1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit

1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit

1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit

1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit

1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit

1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit⁽¹⁾

TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is not full
0 = FIFO is full

TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

Note 1: This bit is read-only and reflects the status of the FIFO.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

28.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. “Watchdog Timer and Power-up Timer”** (DS60001114), **Section 32. “Configuration”** (DS60001124) and **Section 33. “Programming and Diagnostics”** (DS60001129) in the *“PIC32 Family Reference Manual”*, which are available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible device configuration
- Watchdog Timer (WDT)
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)

28.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- CFGCON: Configuration Control Register

In addition, the DEVID register (Register 28-6) provides device and revision information.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

FIGURE 31-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

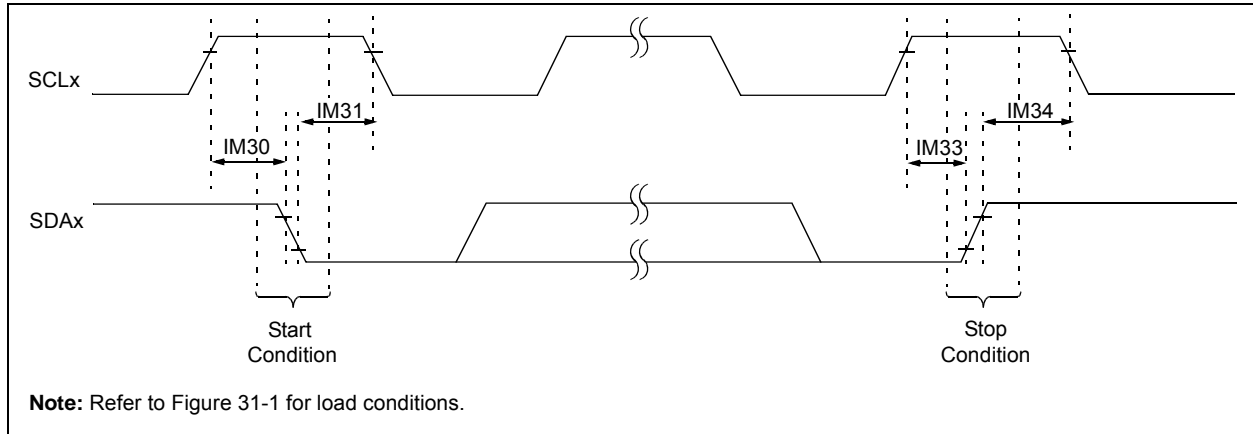
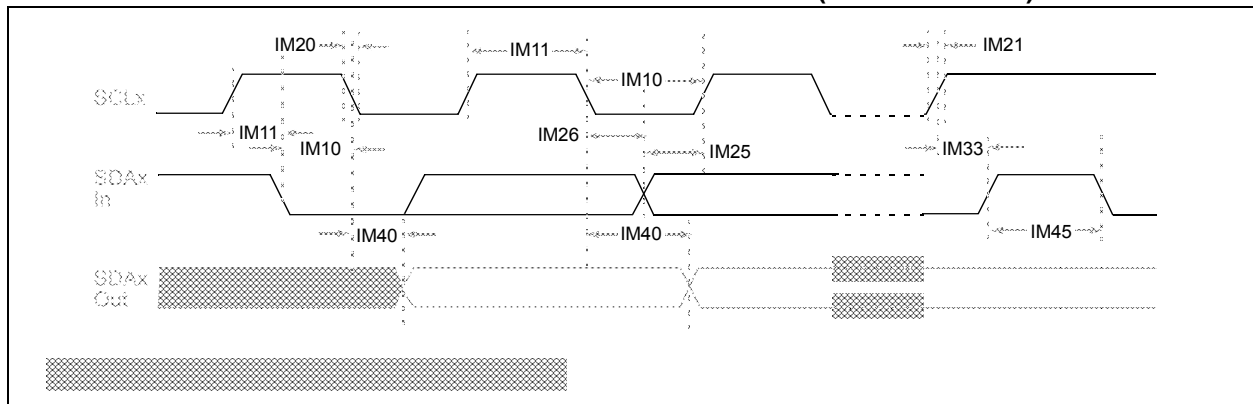


FIGURE 31-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

32.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX/5XX 64/100-pin AC characteristics and timing parameters.

TABLE 32-5: EXTERNAL CLOCK TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial | | | | |
|--------------------|--------|---------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|----------|------------|-------------------------------|
| Param. No. | Symbol | Characteristics | Min. | Typical | Max. | Units | Conditions |
| MOS10 | Fosc | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) | DC 4 | — — | 50 50 | MHz MHz | EC (Note 2) ECPLL (Note 1) |

- Note 1:** PLL input requirements: $4\text{ MHz} \leq F_{\text{PLLIN}} \leq 5\text{ MHz}$ (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.
- 2:** This parameter is characterized, but not tested in manufacturing.

TABLE 32-6: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial | | | | |
|--------------------|--------|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|------|-------|------------|
| Param. No. | Symbol | Characteristics | Min. | Typical | Max. | Units | Conditions |
| MSP10 | TscL | SCKx Output Low Time (Note 1,2) | Tsck/2 | — | — | ns | — |
| MSP11 | Tsch | SCKx Output High Time (Note 1,2) | Tsck/2 | — | — | ns | — |

- Note 1:** These parameters are characterized, but not tested in manufacturing.
- 2:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

TABLE 32-7: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial | | | | |
|--------------------|--------|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------|------------|
| Param. No. | Symbol | Characteristics ⁽¹⁾ | Min. | Typ. | Max. | Units | Conditions |
| MSP10 | TscL | SCKx Output Low Time (Note 1,2) | Tsck/2 | — | — | ns | — |
| MSP11 | Tsch | SCKx Output High Time (Note 1,2) | Tsck/2 | — | — | ns | — |

- Note 1:** These parameters are characterized, but not tested in manufacturing.
- 2:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 32-8: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp | | | | |
|--------------------|----------|----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------|------------|
| Param. No. | Symbol | Characteristics | Min. | Typ. | Max. | Units | Conditions |
| MSP70 | TscL | SCKx Input Low Time (Note 1,2) | $T_{SCK}/2$ | — | — | ns | — |
| MSP71 | TscH | SCKx Input High Time (Note 1,2) | $T_{SCK}/2$ | — | — | ns | — |
| MSP51 | TssH2doZ | SSx \uparrow to SDOx Output High-Impedance (Note 2) | 5 | — | 25 | ns | — |

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns.

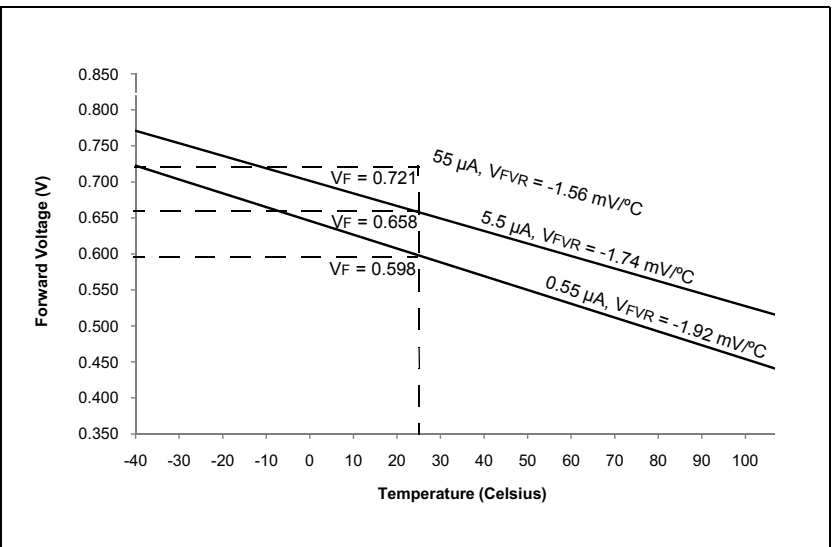
TABLE 32-9: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial | | | | |
|--------------------|--------|------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|------|-------|------------|
| Param. No. | Symbol | Characteristics | Min. | Typical | Max. | Units | Conditions |
| SP70 | TscL | SCKx Input Low Time (Note 1,2) | $T_{SCK}/2$ | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time (Note 1,2) | $T_{SCK}/2$ | — | — | ns | — |

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns.

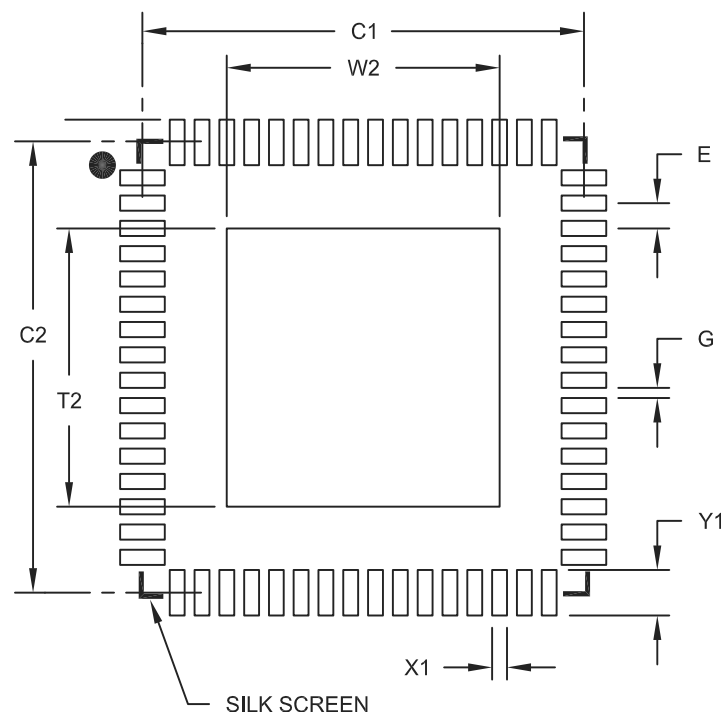
FIGURE 33-5: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE



PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 5.40x5.40mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|----------------------------|----|-------------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Optional Center Pad Width | W2 | | | 5.50 |
| Optional Center Pad Length | T2 | | | 5.50 |
| Contact Pad Spacing | C1 | | 8.90 | |
| Contact Pad Spacing | C2 | | 8.90 | |
| Contact Pad Width (X64) | X1 | | | 0.30 |
| Contact Pad Length (X64) | Y1 | | | 0.85 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2154A

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

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