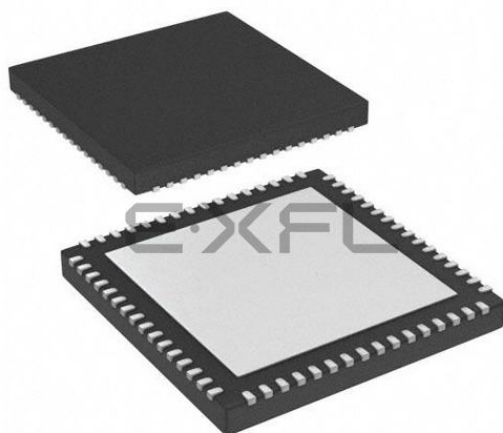




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f256h-50i-mr

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 1: PIC32MX1XX/2XX/5XX 64/100-PIN CONTROLLER FAMILY FEATURES

Device	Pins	Packages ⁽⁴⁾	Program Memory (KB) ⁽¹⁾	Data Memory (KB)	Remappable Peripherals					10-bit 1 Msps ADC (Channels)	Analog Comparators	USB On-The-Go (OTG)	CAN	CTMU	I ² C	PMP	RTCC	DMA Channels (Programmable/Dedicated)	I/O Pins	JTAG
					Remappable Pins	Timers/Capture/Compare ⁽²⁾	UART	SPI/I ² S	External Interrupts ⁽³⁾											
PIC32MX120F064H	64	QFN, TQFP	64+3	8	37	5/5/5	4	3	5	28	3	N	0	Y	2	Y	Y	4/0	53	Y
PIC32MX130F128H	64	QFN, TQFP	128+3	16	37	5/5/5	4	3	5	28	3	N	0	Y	2	Y	Y	4/0	53	Y
PIC32MX130F128L	100	TQFP	128+3	16	54	5/5/5	5	4	5	48	3	N	0	Y	2	Y	Y	4/0	85	Y
	100	TFBGA																		
PIC32MX230F128H	64	QFN, TQFP	128+3	16	37	5/5/5	4	3	5	28	3	Y	0	Y	2	Y	Y	4/2	49	Y
PIC32MX230F128L	100	TQFP	128+3	16	54	5/5/5	5	4	5	48	3	Y	0	Y	2	Y	Y	4/2	81	Y
	100	TFBGA																		
PIC32MX530F128H	64	QFN, TQFP	128+3	16	37	5/5/5	4	3	5	28	3	Y	1	Y	2	Y	Y	4/4	49	Y
PIC32MX530F128L	100	TQFP	128+3	16	54	5/5/5	5	4	5	48	3	Y	1	Y	2	Y	Y	4/4	81	Y
	100	TFBGA																		
PIC32MX150F256H	64	QFN, TQFP	256+3	32	37	5/5/5	4	3	5	28	3	N	0	Y	2	Y	Y	4/0	53	Y
PIC32MX150F256L	100	TQFP	256+3	32	54	5/5/5	5	4	5	48	3	N	0	Y	2	Y	Y	4/0	85	Y
	100	TFBGA																		
PIC32MX250F256H	64	QFN, TQFP	256+3	32	37	5/5/5	4	3	5	28	3	Y	0	Y	2	Y	Y	4/2	49	Y
PIC32MX250F256L	100	TQFP	256+3	32	54	5/5/5	5	4	5	48	3	Y	0	Y	2	Y	Y	4/2	81	Y
	100	TFBGA																		
PIC32MX550F256H	64	QFN, TQFP	256+3	32	37	5/5/5	4	3	5	28	3	Y	1	Y	2	Y	Y	4/4	49	Y
PIC32MX550F256L	100	TQFP	256+3	32	54	5/5/5	5	4	5	48	3	Y	1	Y	2	Y	Y	4/4	81	Y
	100	TFBGA																		
PIC32MX170F512H	64	QFN, TQFP	512+3	64	37	5/5/5	4	3	5	28	3	N	0	Y	2	Y	Y	4/0	53	Y
PIC32MX170F512L	100	TQFP	512+3	64	54	5/5/5	5	4	5	48	3	N	0	Y	2	Y	Y	4/0	85	Y
	100	TFBGA																		
PIC32MX270F512H	64	QFN, TQFP	512+3	64	37	5/5/5	4	3	5	28	3	Y	0	Y	2	Y	Y	4/2	49	Y
PIC32MX270F512L	100	TQFP	512+3	64	54	5/5/5	5	4	5	48	3	Y	0	Y	2	Y	Y	4/2	81	Y
	100	TFBGA																		
PIC32MX570F512H	64	QFN, TQFP	512+3	64	37	5/5/5	4	3	5	28	3	Y	1	Y	2	Y	Y	4/4	49	Y
PIC32MX570F512L	100	TQFP	512+3	64	54	5/5/5	5	4	5	48	3	Y	1	Y	2	Y	Y	4/4	81	Y
	100	TFBGA																		

- Note**
- 1: All devices feature 3 KB of Boot Flash memory.
 - 2: Four out of five timers are remappable.
 - 3: Four out of five external interrupts are remappable.
 - 4: Please contact your local Microchip Sales Office for information regarding the availability of devices in the 100-pin TFBGA package.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 3: PIN NAMES FOR 64-PIN USB DEVICES

64-PIN QFN ⁽⁴⁾ AND TQFP (TOP VIEW)			
PIC32MX230F128H PIC32MX530F128H PIC32MX250F256H PIC32MX550F256H PIC32MX270F512H PIC32MX570F512H		64	1
		QFN ⁽⁴⁾	TQFP ¹
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN22/RPE5/PMD5/RE5	33	USBID/RPF3/RF3
2	AN23/PMD6/RE6	34	VBUS
3	AN27/PMD7/RE7	35	VUSB3V3
4	AN16/C1IND/RPG6/SCK2/PMA5/RG6	36	D-
5	AN17/C1INC/RPG7/PMA4/RG7	37	D+
6	AN18/C2IND/RPG8/PMA3/RG8	38	VDD
7	MCLR	39	OSC1/CLKI/RC12
8	AN19/C2INC/RPG9/PMA2/RG9	40	OSC2/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	RPD8/RTCC/RD8
11	AN5/C1INA/RPB5/VBUSON/RB5	43	RPD9/SDA1/RD9
12	AN4/C1INB/RB4	44	RPD10/SCL1/PMA15/RD10
13	PGED3/AN3/C2INA/RPB3/RB3	45	RPD11/PMA14/RD11
14	PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2	46	RPD0/INT0/RD0
15	PGEC1/VREF-/AN1/RPB1/CTED12/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN6/RPB6/RB6	49	AN24/RPD1/RD1
18	PGED2/AN7/RPB7/CTED3/RB7	50	AN25/RPD2/SCK1/RD2
19	AVDD	51	AN26/C3IND/RPD3/RD3
20	AVSS	52	RPD4/PMWR/RD4
21	AN8/RPB8/CTED10/RB8	53	RPD5/PMRD/RD5
22	AN9/RPB9/CTED4/PMA7/RB9	54	C3INC/RD6
23	TMS/CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	55	C3INB/RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	VSS	57	VDD
26	VDD	58	C3INA/RPF0/RF0
27	TCK/AN12/PMA11/RB12	59	RPF1/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/RPB14/SCK3/CTED5/PMA1/RB14	61	PMD1/RE1
30	AN15/RPB15/OCFB/CTED6/PMA0/RB15	62	AN20/PMD2/RE2
31	RPF4/SDA2/PMA9/RF4	63	RPE3/CTPLS/PMD3/RE3
32	RPF5/SCL2/PMA8/RF5	64	AN21/PMD4/RE4

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
 - 2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 11.0 “I/O Ports”** for more information.
 - 3: Shaded pins are 5V tolerant.
 - 4: The metal plane at the bottom of the QFN device is not connected to any pins and is recommended to be connected to Vss externally.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 5: PIN NAMES FOR 100-PIN USB DEVICES

100-PIN TQFP (TOP VIEW)		100		1	
PIC32MX230F128L PIC32MX530F128L PIC32MX250F256L PIC32MX550F256L PIC32MX270F512L PIC32MX570F512L					
Pin #	Full Pin Name	Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN28/RG15	36	VSS		
2	VDD	37	VDD		
3	AN22/RPE5/PMD5/RE5	38	TCK/CTED2/RA1		
4	AN23/PMD6/RE6	39	AN34/RPF13/SCK3/RF13		
5	AN27/PMD7/RE7	40	AN35/RPF12/RF12		
6	AN29/RPC1/RC1	41	AN12/PMA11/RB12		
7	AN30/RPC2/RC2	42	AN13/PMA10/RB13		
8	AN31/RPC3/RC3	43	AN14/RPB14/CTED5/PMA1/RB14		
9	RPC4/CTED7/RC4	44	AN15/RPB15/OCFB/CTED6/PMA0/RB15		
10	AN16/C1IND/RPG6/SCK2/PMA5/RG6	45	VSS		
11	AN17/C1INC/RPG7/PMA4/RG7	46	VDD		
12	AN18/C2IND/RPG8/PMA3/RG8	47	AN36/RPD14/RD14		
13	MCLR	48	AN37/RPD15/SCK4/RD15		
14	AN19/C2INC/RPG9/PMA2/RG9	49	RPF4/PMA9/RF4		
15	VSS	50	RPF5/PMA8/RF5		
16	VDD	51	USBID/RPF3/RF3		
17	TMS/CTED1/RA0	52	AN38/RPF2/RF2		
18	AN32/RPE8/RE8	53	AN39/RPF8/RF8		
19	AN33/RPE9/RE9	54	VBUS		
20	AN5/C1INA/RPB5/VBUS0N/RB5	55	VUSB3V3		
21	AN4/C1INB/RB4	56	D-		
22	PGED3/AN3/C2INA/RPB3/RB3	57	D+		
23	PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2	58	SCL2/RA2		
24	PGEC1/AN1/RPB1/CTED12/RB1	59	SDA2/RA3		
25	PGED1/AN0/RPB0/RB0	60	TDI/CTED9/RA4		
26	PGEC2/AN6/RPB6/RB6	61	TDO/RA5		
27	PGED2/AN7/RPB7/CTED3/RB7	62	VDD		
28	VREF-/PMA7/RA9	63	OSC1/CLK1/RC12		
29	VREF+/PMA6/RA10	64	OSC2/CLK0/RC15		
30	AVDD	65	VSS		
31	AVSS	66	RPA14/SCL1/RA14		
32	AN8/RPB8/CTED10/RB8	67	RPA15/SDA1/RA15		
33	AN9/RPB9/CTED4/RB9	68	RPD8/RTCC/RD8		
34	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	69	RPD9/RD9		
35	AN11/PMA12/RB11	70	RPD10/SCK1/PMA15/RD10		

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
 - 2: Every I/O port pin (RAX-RGx) can be used as a change notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
 - 3: Shaded pins are 5V tolerant.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
Interrupt Controller	0xBF88	0x1000
Bus Matrix		0x2000
DMA		0x3000
USB		0x5000
PORTA-PORTG		0x6000
CAN1		0xB000
Watchdog Timer	0xBF80	0x0000
RTCC		0x0200
Timer1-Timer5		0x0600
IC1-IC5		0x2000
OC1-OC5		0x3000
I2C1-I2C2		0x5000
SPI1-SPI4		0x5800
UART1-UART5		0x6000
PMP		0x7000
ADC1		0x9000
DAC		0x9800
Comparator 1, 2, 3		0xA000
Oscillator		0xF000
Device and Revision ID		0xF200
Flash Controller		0xF400
PPS		0xFA00
Configuration	0xBFC0	0x0BF0

4.2 Special Function Register Maps

TABLE 4-2: BUS MATRIX REGISTER MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	BMXCON ⁽¹⁾	31:16	—	—	—	—	—	BMXCHEDMA	—	—	—	—	—	BMXERRIXI	BMXERRICD	BMXERRDMA	BMXERRDS	BMXERRIS	041F
		15:0	—	—	—	—	—	—	—	—	—	BMXWSDRM	—	—	—	BMXARB<2:0>			0047
2010	BMXDKPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDKPBA<15:0>																0000
2020	BMXDUDBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDUDBA<15:0>																0000
2030	BMXDUPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDUPBA<15:0>																0000
2040	BMXDRMSZ	31:16	BMXDRMSZ<31:0>																xxxx
		15:0	BMXDRMSZ<31:0>																xxxx
2050	BMXPUPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	BMXPUPBA<19:16>					0000
		15:0	BMXPUPBA<15:0>																0000
2060	BMXPFMSZ	31:16	BMXPFMSZ<31:0>																xxxx
		15:0	BMXPFMSZ<31:0>																xxxx
2070	BMXBOOTSZ	31:16	BMXBOOTSZ<31:0>																0000
		15:0	BMXBOOTSZ<31:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET, and INV Registers” for more information.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	BMXDRMSZ<31:24>							
23:16	R	R	R	R	R	R	R	R
	BMXDRMSZ<23:16>							
15:8	R	R	R	R	R	R	R	R
	BMXDRMSZ<15:8>							
7:0	R	R	R	R	R	R	R	R
	BMXDRMSZ<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **BMXDRMSZ<31:0>**: Data RAM Memory (DRM) Size bits

Static value that indicates the size of the Data RAM in bytes:

0x00002000 = Device has 8 KB RAM

0x00004000 = Device has 16 KB RAM

0x00008000 = Device has 32 KB RAM

0x00010000 = Device has 64 KB RAM

REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	BMXPUPBA<19:16>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
	BMXPUPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXPUPBA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-20 **Unimplemented**: Read as '0'

bit 19-11 **BMXPUPBA<19:11>**: Program Flash (PFM) User Program Base Address bits

bit 10-0 **BMXPUPBA<10:0>**: Read-Only bits

Value is always '0', which forces 2 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.

2: The value in this register must be less than or equal to BMXPFMSZ.

TABLE 9-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
3280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>																0000	
3290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>									0000
32A0	DCH3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000	
32B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>									00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FFF8	
32C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000	
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000	
32D0	DCH3SSA	31:16	CHSSA<31:0>																0000	
		15:0																	0000	
32E0	DCH3DSA	31:16	CHDSA<31:0>																0000	
		15:0																	0000	
32F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSSIZ<15:0>																0000	
3300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>																0000	
3310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>																0000	
3320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>																0000	
3330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>																0000	
3340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>																0000	
3350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>									0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET, and INV Registers” for more information.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

NOTES:

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 11-1: INPUT PIN SELECTION (CONTINUED)

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPN Pin Selection
INT1	INT1R	INT1R<3:0>	0000 = RPD1 0001 = RPG9 0010 = RPB14 0011 = RPD0 0100 = RPD8 0101 = RPB6 0110 = RPD5 0111 = RPB2 1000 = RPF3 ⁽⁴⁾ 1001 = RPF13 ⁽³⁾ 1010 = Reserved 1011 = RPF2 ⁽¹⁾ 1100 = RPC2 ⁽³⁾ 1101 = RPE8 ⁽³⁾ 1110 = Reserved 1111 = Reserved
T3CK	T3CKR	T3CKR<3:0>	
IC1	IC1R	IC1R<3:0>	
$\overline{\text{U3CTS}}$	U3CTSR	U3CTSR<3:0>	
U4RX	U4RXR	U4RXR<3:0>	
U5RX	U5RXR	U5RXR<3:0>	
$\overline{\text{SS2}}$	SS2R	SS2R<3:0>	
OCFA	OCFAR	OCFAR<3:0>	

- Note 1:** This selection is not available on 64-pin USB devices.
2: This selection is only available on 100-pin General Purpose devices.
3: This selection is not available on 64-pin devices.
4: This selection is not available when USBID functionality is used on USB devices.
5: This selection is not available on devices without a CAN module.
6: This selection is not available on USB devices.
7: This selection is not available when VBUSON functionality is used on USB devices.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 18-1: I2CxCON: I²C 'x' CONTROL REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
	ON ⁽¹⁾	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

Legend:	HC = Cleared in Hardware
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** I²C Enable bit⁽¹⁾

1 = Enables the I²C module and configures the SDA and SCL pins as serial port pins

0 = Disables the I²C module; all I²C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)

1 = Release SCLx clock

0 = Hold SCLx clock low (clock stretch)

If STREN = 1:

Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:

Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.

bit 11 **STRICT:** Strict I²C Reserved Address Rule Enable bit

1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.

0 = Strict I²C Reserved Address Rule not enabled

bit 10 **A10M:** 10-bit Slave Address bit

1 = I2CxADD is a 10-bit slave address

0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit

1 = Slew rate control disabled

0 = Slew rate control enabled

bit 8 **SMEN:** SMBus Input Levels bit

1 = Enable I/O pin thresholds compliant with SMBus specification

0 = Disable SMBus input thresholds

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

bit 5-2 **WAITM<3:0>**: Data Read/Write Strobe Wait States bits⁽¹⁾

1111 = Wait of 16 TPB

•
•
•

0001 = Wait of 2 TPB

0000 = Wait of 1 TPB (default)

bit 1-0 **WAITE<1:0>**: Data Hold After Read/Write Strobe Wait States bits⁽¹⁾

11 = Wait of 4 TPB

10 = Wait of 3 TPB

01 = Wait of 2 TPB

00 = Wait of 1 TPB (default)

For Read operations:

11 = Wait of 3 TPB

10 = Wait of 2 TPB

01 = Wait of 1 TPB

00 = Wait of 0 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

3: These pins are active when MODE16 = 1 (16-bit mode).

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 21-2: RTCLARM: RTC ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ALRMEN ^(1,2)	R/W-0 CHIME ⁽²⁾	R/W-0 PIV ⁽²⁾	R-0 ALRMSYNC ⁽³⁾	R/W-0	R/W-0	R/W-0	R/W-0
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ARPT<7:0> ⁽³⁾								

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit^(1,2)

1 = Alarm is enabled

0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit⁽²⁾

1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF

0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit⁽²⁾

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.

When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit⁽³⁾

1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read.

The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain

0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits⁽³⁾

0000 = Every half-second

0001 = Every second

0010 = Every 10 seconds

0011 = Every minute

0100 = Every 10 minutes

0101 = Every hour

0110 = Once a day

0111 = Once a week

1000 = Once a month

1001 = Once a year (except when configured for February 29, once every four years)

1010 = Reserved; do not use

1011 = Reserved; do not use

11xx = Reserved; do not use

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 23-2: C1CFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

bit 10-8 **PRSEG<2:0>**: Propagation Time Segment bits⁽⁴⁾

111 = Length is 8 x T_Q

•
•
•

000 = Length is 1 x T_Q

bit 7-6 **SJW<1:0>**: Synchronization Jump Width bits⁽³⁾

11 = Length is 4 x T_Q

10 = Length is 3 x T_Q

01 = Length is 2 x T_Q

00 = Length is 1 x T_Q

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits

111111 = T_Q = (2 x 64)/SYSCLK

111110 = T_Q = (2 x 63)/SYSCLK

•
•
•

000001 = T_Q = (2 x 2)/SYSCLK

000000 = T_Q = (2 x 1)/SYSCLK

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.

2: 3 Time bit sampling is not allowed for BRP < 2.

3: SJW ≤ SEG2PH.

4: The Time Quanta per bit must be greater than 7 (that is, T_{QBIT} > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = 100).

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 23-15: C1FIFOBA: CAN MESSAGE BUFFER BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	C1FIFOBA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	C1FIFOBA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	C1FIFOBA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0 ⁽¹⁾	R-0 ⁽¹⁾
	C1FIFOBA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **C1FIFOBA<31:0>**: CAN FIFO Base Address bits

These bits define the base address of all message buffers. Individual message buffers are located based on the size of the previous message buffers. This address is a physical address. Bits <1:0> are read-only and read as '0', forcing the messages to be 32-bit word-aligned in device RAM.

Note 1: This bit is unimplemented and will always read '0', which forces word-alignment of messages.

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = 100).

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 23-17: C1FIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXNEMPTYIE
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	TXNFULLIF ⁽¹⁾	TXHALFIF	TXEMPTYIF ⁽¹⁾
7:0	U-0	U-0	U-0	U-0	R/W-0	R-0	R-0	R-0
	—	—	—	—	RXOVFLIF	RXFULLIF ⁽¹⁾	RXHALFIF ⁽¹⁾	RXNEMPTYIF ⁽¹⁾

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit

1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit

1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit

1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit

1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit

1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit

1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit

1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit⁽¹⁾

TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is not full
0 = FIFO is full

TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

Note 1: This bit is read-only and reflects the status of the FIFO.

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REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	CTMUSIDL	TGEN ⁽⁴⁾	EDGEN	EDGSEQEN	IDISSEN ⁽²⁾	CTTRIG
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ITRIM<5:0>						IRNG<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **EDG1MOD:** Edge 1 Edge Sampling Select bit

1 = Input is edge-sensitive

0 = Input is level-sensitive

bit 30 **EDG1POL:** Edge 1 Polarity Select bit

1 = Edge 1 programmed for a positive edge response

0 = Edge 1 programmed for a negative edge response

bit 29-26 **EDG1SEL<3:0>:** Edge 1 Source Select bits

1111 = IC4 Capture Event is selected

1110 = C2OUT pin is selected

1101 = C1OUT pin is selected

1100 = IC3 Capture Event is selected

1011 = IC2 Capture Event is selected

1010 = IC1 Capture Event is selected

1001 = CTED8 pin is selected

1000 = CTED7 pin is selected

0111 = CTED6 pin is selected

0110 = CTED5 pin is selected

0101 = CTED4 pin is selected

0100 = CTED3 pin is selected

0011 = CTED1 pin is selected

0010 = CTED2 pin is selected

0001 = OC1 Compare Event is selected

0000 = Timer1 Event is selected

bit 25 **EDG2STAT:** Edge 2 Status bit

Indicates the status of Edge 2 and can be written to control edge source

1 = Edge 2 has occurred

0 = Edge 2 has not occurred

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 31-41) in **Section 31.0 "40 MHz Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

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NOTES:

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 31-12: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
Program Flash Memory⁽³⁾							
D130	EP	Cell Endurance	20,000	—	—	E/W	—
D131	VPR	VDD for Read	2.3	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
	TWW	Word Write Cycle Time	—	411	—	FRC Cycles	See Note 4
D136	TRW	Row Write Cycle Time	—	6675	—	FRC Cycles	See Note 2,4
D137	TPE	Page Erase Cycle Time	—	20011	—	FRC Cycles	See Note 4
	TCE	Chip Erase Cycle Time	—	80180	—	FRC Cycles	See Note 4

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

3: Refer to the “PIC32 Flash Programming Specification” (DS60001145) for operating conditions during programming and erase cycles.

4: This parameter depends on FRC accuracy (See Table 31-19) and FRC tuning values (See Register 8-2).

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TABLE 32-3: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial	
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions
Idle Current (I_{IDLE}): Core Off, Clock on Base Current (Note 1)				
MDC34a	9.5	24	mA	50 MHz

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{\text{MCLR}} = V_{DD}$
- RTCC and JTAG are disabled

2: Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 32-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial	
Param. No.	Typical ⁽²⁾	Max.	Units	Conditions
Power-Down Current (I_{PD}) (Note 1)				
MDC40k	50	150	μA	-40°C
MDC40n	250	650	μA	+85°C
Module Differential Current				
MDC41e	15	55	μA	3.6V
MDC42e	34	55	μA	3.6V
MDC43d	1100	1800	μA	3.6V

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{\text{MCLR}} = V_{DD}$
- RTCC and JTAG are disabled

2: Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

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