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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	256КВ (256К × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f256h-50i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to Vss through a 1k to 10k resistor and configuring the pin as an input.

TABLE 4-1: SFR MEMORY MAP

Derinheral	Virtual Address			
Peripheral	Base	Offset Start		
Interrupt Controller		0x1000		
Bus Matrix		0x2000		
DMA	0.0000	0x3000		
USB	UXBE88	0x5000		
PORTA-PORTG		0x6000		
CAN1		0xB000		
Watchdog Timer		0x0000		
RTCC		0x0200		
Timer1-Timer5		0x0600		
IC1-IC5		0x2000		
OC1-OC5		0x3000		
I2C1-I2C2		0x5000		
SPI1-SPI4		0x5800		
UART1-UART5		0x6000		
PMP	UXDFOU	0x7000		
ADC1		0x9000		
DAC		0x9800		
Comparator 1, 2, 3		0xA000		
Oscillator		0xF000		
Device and Revision ID		0xF200		
Flash Controller		0xF400		
PPS		0xFA00		
Configuration	0xBFC0	0x0BF0		

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31:24				NVMDA	TA<31:24>				
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:10	NVMDATA<23:16>								
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
10.0	NVMDATA<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
				NVMD	ATA<7:0>				

REGISTER 6-4: NVMDATA: FLASH PROGRAM DATA REGISTER

I edend.

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMDATA<31:0>: Flash Programming Data bits

Note: The bits in this register are only reset by a Power-on Reset (POR).

NVMSRCADDR: SOURCE DATA ADDRESS REGISTER **REGISTER 6-5:**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31:24		NVMSRCADDR<31:24>								
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23:10	NVMSRCADDR<23:16>									
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	NVMSRCADDR<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				NVMSRC	ADDR<7:0>					

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-0 NVMSRCADDR<31:0>: Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24	—	—	—	—	—	—	—	—	
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	_	—	—	—	
45.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
15:8	CHSPTR<15:8>								
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
				CHSPTF	R<7:0>				

REGISTER 9-14: DCHxSPTR: DMA CHANNEL 'x' SOURCE POINTER REGISTER

Legend:

0			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSPTR<15:0>: Channel Source Pointer bits

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 9-15: DCHxDPTR: DMA CHANNEL 'x' DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24		—	—	—	—	—	—	_	
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10		—	—	—	—	—	—	_	
15.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
10.0	CHDPTR<15:8>								
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
7:0				CHDPTF	R<7:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16	Unimplemented: Read as '0'
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bit 15-0 CHDPTR<15:0>: Channel Destination Pointer bits

1111111111111111 = Points to byte 65,535 of the destination

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—	-	—	—	
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	CHCSIZ<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7.0				CHCSIZ	<u>/</u> <7:0>				

REGISTER 9-16: DCHxCSIZ: DMA CHANNEL 'x' CELL-SIZE REGISTER

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHCSIZ<15:0>: Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event

REGISTER 9-17: DCHxCPTR: DMA CHANNEL 'x' CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31.24	—	—	—	—	_	_		—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:10	—	—	—	—	—	—	_	—			
45.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
15:8	CHCPTR<15:8>										
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
1.0		CHCPTR<7:0>									

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

TABLE 11-18: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

ss										В	its								
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
ED00	PDC2P	31:16	_	_	_	_	—	_	_	—	—	—	_	—	_	_		_	0000
FB00	RPG2R	15:0		—	—	_	_	—	—	_	_	_	_	_		RPC2	<3:0>		0000
EDOC	DDC2D	31:16		—	—	_	_	—	_	_	_	_	_	_	_	_			0000
FBOC	RECOR	15:0		—	—	—	_	—	—	_	_	_	—	_		RPC3	<3:0>		0000
FROO	PPC/P	31:16		—		—	—	—	—	—	—	—	—	—	—	—	_	—	0000
1 890	KF 04K	15:0	-	—	—	—	_	—	—	_	_	_	—	_		RPC4	<3:0>		0000
EBB4	PPC13P	31:16		—		—	—	—	—	—	—	—	—	—	—	—	_	—	0000
1004	IN CISIN	15:0	_	—	—	—		—	—				—			RPC1	3<3:0>		0000
FBB8	RPC14R	31:16	_	—	—	—		—	—				—		—	—	—	—	0000
1 000		15:0	—	—	—	—	—	—	—	—	—	—	—	—		RPC14	4<3:0>		0000
FBC0	RPD0R	31:16	_		—	—	_			_	_	_	—		—	—	—	—	0000
		15:0	_		—	—	_			_	_	_	—			RPD0	<3:0>		0000
FBC4	RPD1R	31:16		—		—	—	—		—	—	—	—	—			—	—	0000
		15:0	_			—	—			—	—	—	—	—		RPD1	<3:0>		0000
FBC8	RPD2R	31:16	_		—	—	—				—		—			—	—	—	0000
		15:0	_		—	—	—			—	—	—	—	—		RPD2	<3:0>		0000
FBCC	RPD3R	31:16			—	—	—			—	—	—	—	—		—	—	—	0000
	_	15:0	_		—	—	—				—		—			RPD3	<3:0>		0000
FBD0	RPD4R	31:16			—	—	—			—	—	—	—	—	—	—	—	—	0000
		15:0	—		-	—	—			_	—	—	—	—		RPD4	<3:0>		0000
FBD4	RPD5R	31:16	—		-	—	—			_	—	—	—	—	—	—	—	—	0000
		15:0	_			_	_			_	_	_	_	_		RPD5	<3:0>		0000
FBE0	RPD8R	31:16	_			_							_				_		0000
		15:0	_			_							_			RPD8	<3:0>		0000
FBE4	RPD9R	31:16				_											-		0000
		15:0	_			_	_			_	_	_	_	_		RPD9	<3:0>		0000
FBE8	RPD10R	31:16	_							_		_					-	_	0000
		15:0	_							_		_				RPD10)<3:0>		0000
FBEC	RPD11R	31:16	_			_	_			_	_	_	_	_		-	—	—	0000
		15:0	_							_		_				RPD1	<3:0>		0000
FBF0	RPD12R	31:10	_		_	_	—		_	—	_	—	_	—	_		—	_	0000
		15:0	—	_	-	—	—	_	_	—	—	—	—	—		RPD12	2<3:0>		0000
FBF8	RPD14R	31:16	—		_	—	—		_	—	—	—	—	—	—			—	0000
		15:0	—	—		—	—	—	—	_	_	—	—	_		RPD14	+<3:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available if the associated RPx function is not present on the device. Refer to the pin table for the specific device to determine availability.

REGISTER 15-1: ICXCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)('x' = 1 THROUGH 5)

- bit 2-0 ICM<2:0>: Input Capture Mode Select bits
 - 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
 - 110 = Simple Capture Event mode every edge, specified edge first and every edge thereafter
 - 101 = Prescaled Capture Event mode every sixteenth rising edge
 - 100 = Prescaled Capture Event mode every fourth rising edge
 - 011 = Simple Capture Event mode every rising edge
 - 010 = Simple Capture Event mode every falling edge
 - 001 = Edge Detect mode every edge (rising and falling)
 - 000 = Input Capture module is disabled
- **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
 - 1 = Frame synchronization pulse coincides with the first bit clock
 - 0 = Frame synchronization pulse precedes the first bit clock
- bit 16 **ENHBUF:** Enhanced Buffer Enable bit⁽²⁾
 - 1 = Enhanced Buffer mode is enabled
 - 0 = Enhanced Buffer mode is disabled
- bit 15 **ON:** SPI Peripheral On bit⁽¹⁾
 - 1 = SPI Peripheral is enabled
 - 0 = SPI Peripheral is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 SIDL: Stop in Idle Mode bit
 - 1 = Discontinue operation when CPU enters in Idle mode
 - 0 = Continue operation in Idle mode
- bit 12 **DISSDO:** Disable SDOx pin bit
 - 1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
 - 0 = SDOx pin is controlled by the module
- bit 11-10 MODE<32,16>: 32/16-Bit Communication Select bits

When AUDEN = 1:

- MODE32 MODE16 Communication
 - 11 24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
 - 10 32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
 - 01 16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame
 - 00 16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame

When AUDEN = 0:

MODE32 MODE16 Communication

- 1x **32-bit**
- 01 **16-bit**
- 00 **8-bit**
- bit 9 SMP: SPI Data Input Sample Phase bit

Master mode (MSTEN = 1):

- 1 = Input data sampled at end of data output time
- 0 = Input data sampled at middle of data output time
- Slave mode (MSTEN = 0):
- SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.
- bit 8 CKE: SPI Clock Edge Select bit⁽³⁾
 - 1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)
 0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)
 - SSEN: Slave Select Enable (Slave mode) bit
 - 1 = SSx pin used for Slave mode
 - $0 = \overline{SSx}$ pin not used for Slave mode, pin controlled by port function.
- bit 6 **CKP:** Clock Polarity Select bit⁽⁴⁾

bit 7

- 1 = Idle state for clock is a high level; active state is a low level
- 0 = Idle state for clock is a low level; active state is a high level
- bit 5 MSTEN: Master Mode Enable bit
 - 1 = Master mode
 - 0 = Slave mode
- **Note 1:** When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - **2:** This bit can only be written when the ON bit = 0.
 - **3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
 - 4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 4 DISSDI: Disable SDI bit
 - 1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
 - 0 = SDI pin is controlled by the SPI module
- bit 3-2 STXISEL<1:0>: SPI Transmit Buffer Empty Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
 - 10 = Interrupt is generated when the buffer is empty by one-half or more
 - 01 = Interrupt is generated when the buffer is completely empty
 - 00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete
- bit 1-0 SRXISEL<1:0>: SPI Receive Buffer Full Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is full
 - 10 = Interrupt is generated when the buffer is full by one-half or more
 - 01 = Interrupt is generated when the buffer is not empty
 - 00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)
- **Note 1:** When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - **2:** This bit can only be written when the ON bit = 0.
 - **3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
 - 4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

19.1 Control Registers

TABLE 19-1: UART1 THROUGH UART5 REGISTER MAP

ress		e								Bi	its								s
Virtual Add (BF80_#	Registe Name	Bit Rang	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
<u></u>		31:16	—	_	_	_	—	—	—	_	_	_	—	_	_	_	_	_	0000
6000	UTWODE	15:0	ON	—	SIDL	IREN	RTSMD	—	UEN	<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSE	L<1:0>	STSEL	0000
6010	111574(1)	31:16	—	—	_	—	—	—	—	ADM_EN				ADDF	R<7:0>				0000
0010	UISIA	15:0	UTXISI	EL<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXIS	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	FFFF
6020		31:16	_	—	_				—	—	—	—	—	—	—	—	—	—	0000
0020	UTIXILE	15:0		—	_				_	TX8				Transmit	t Register				0000
6030	U1RXREG	31:16	—	—	—	—	—	—	—	—	_	—	—		—	—			0000
	01104120	15:0	—	—	—	—	—	—	—	RX8				Receive	Register				0000
6040	U1BRG ⁽¹⁾	31:16	_	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0		-		-	-		Bau	d Rate Gen	erator Pres	caler							0000
6200	U2MODE ⁽¹⁾	31:16	—	—			—	—	—	_	—	—	—	—	—	—		—	0000
		15:0	ON	_	SIDL	IREN	RTSMD	—	UEN	<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSE	L<1:0>	STSEL	0000
6210	U2STA ⁽¹⁾	31:16	—	—	—	—	—	—		ADM_EN			r	ADDF	R<7:0>	r	1	1	0000
		15:0	UTXISI	EL<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXIS	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	FFFI
6220	U2TXREG	31:16	_	—		—	—	—	_	—	—	—	—		—	—			0000
		15:0	—	—	_	—		—	_	TX8				Transmit	t Register				0000
6230	U2RXREG	31:16	_						_	_	—	—	—			—	—	—	0000
		15:0	_						_	RX8				Receive	Register				0000
6240	U2BRG ⁽¹⁾	31:16			_		—	_				. —			—	_			0000
		15:0			1				Bau	d Rate Gen	erator Pres	caler							0000
6400	U3MODE ⁽¹⁾	31:16	_		-	-	-	—	—		—	—		—	—		<u> </u>	-	0000
		15.0	ON	_	SIDL	IREN	RTSMD	—	UEN	<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSE	L<1:0>	STSEL	0000
6410	U3STA ⁽¹⁾	31:16	—		—	—	—	—	—	ADM_EN				ADDF	₹<7:0>		0500		0000
		15:0	UTXISI	=L<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXIS	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	FFFF
6420	U3TXREG	31:16										_				_			0000
		15:0	_		-			_	_	TX8				Transmit	t Register				0000
6430	U3RXREG	31:16	_		-			_	_	—	_	—	—			—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8				Receive	Register				0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

2: This register is only available on 100-pin devices.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 23-17: C1FIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
01.04	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
31:24	—	—	—	_	—	TXNFULLIE	TXHALFIE	TXEMPTYIE
00.40	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	—	—	—	_	RXOVFLIE	RXFULLIE	RXHALFIE	RXNEMPTYIE
45.0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
15:8	—	—	—	_	—	TXNFULLIF ⁽¹⁾	TXHALFIF	TXEMPTYIF ⁽¹⁾
7.0	U-0	U-0	U-0	U-0	R/W-0	R-0	R-0	R-0
7:0	_	_	_	_	RXOVFLIF	RXFULLIF ⁽¹⁾	RXHALFIF ⁽¹⁾	RXNEMPTYIF ⁽¹⁾

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 Unimplemented: Read as '0'

bit 26	TXNFULLIE: Transmit FIFO Not Full Interrupt Enable bit 1 = Interrupt enabled for FIFO not full 0 = Interrupt disabled for FIFO not full
bit 25	TXHALFIE: Transmit FIFO Half Full Interrupt Enable bit 1 = Interrupt enabled for FIFO half full 0 = Interrupt disabled for FIFO half full
bit 24	TXEMPTYIE: Transmit FIFO Empty Interrupt Enable bit 1 = Interrupt enabled for FIFO empty 0 = Interrupt disabled for FIFO empty
bit 23-20	Unimplemented: Read as '0'
bit 19	RXOVFLIE: Overflow Interrupt Enable bit
	1 = Interrupt enabled for overflow event0 = Interrupt disabled for overflow event
bit 18	RXFULLIE: Full Interrupt Enable bit 1 = Interrupt enabled for FIFO full 0 = Interrupt disabled for FIFO full
bit 17	RXHALFIE: FIFO Half Full Interrupt Enable bit 1 = Interrupt enabled for FIFO half full 0 = Interrupt disabled for FIFO half full
bit 16	RXNEMPTYIE: Empty Interrupt Enable bit
	1 = Interrupt enabled for FIFO not empty0 = Interrupt disabled for FIFO not empty
bit 15-11	Unimplemented: Read as '0'
bit 10	TXNFULLIF: Transmit FIFO Not Full Interrupt Flag bit ⁽¹⁾ TXEN = 1: (FIFO configured as a transmit buffer) 1 = FIFO is not full 0 = FIFO is full
	<u>TXEN = 0:</u> (FIFO configured as a receive buffer) Unused, reads '0'
Note 1:	This bit is read-only and reflects the status of the FIFO.

28.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 9. "Watchdog Timer and Power-up Timer" (DS60001114), Section 32. "Configuration" (DS60001124) and Section 33. "Programming and Diagnostics" (DS60001129) in the "PIC32 Family Reference Manual", which are available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible device configuration
- Watchdog Timer (WDT)
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming[™] (ICSP[™])

28.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- CFGCON: Configuration Control Register

In addition, the DEVID register (Register 28-6) provides device and revision information.

TABLE 31-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHA	ARACTER	ISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Conditions	
Operati	ng Voltag	e						
DC10	Vdd	Supply Voltage (Note 2)	2.3		3.6	V	—	
DC12	Vdr	RAM Data Retention Voltage (Note 1)	1.75	-		V	—	
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	1.75	_	2.1	V	_	
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.00005	—	0.115	V/μs	_	

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for BOR values.

АС СНА	RACTERIS	STICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Charact	eristics	Min.	Max.	Units	Conditions	
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	_	μS	PBCLK must operate at a minimum of 800 kHz	
			400 kHz mode	1.3	_	μS	PBCLK must operate at a minimum of 3.2 MHz	
			1 MHz mode (Note 1)	0.5	_	μS	_	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μS	PBCLK must operate at a minimum of 800 kHz	
			400 kHz mode	0.6	—	μS	PBCLK must operate at a minimum of 3.2 MHz	
			1 MHz mode (Note 1)	0.5	_	μS		
IS20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be from	
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode (Note 1)	—	100	ns		
IS21	TR:SCL	SDAx and SCLx	100 kHz mode	—	1000	ns	CB is specified to be from	
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode (Note 1)	—	300	ns		
IS25	TSU:DAT	Data Input	100 kHz mode	250	—	ns	—	
		Setup Time	400 kHz mode	100	—	ns		
			1 MHz mode (Note 1)	100	_	ns		
IS26	THD:DAT	Data Input	100 kHz mode	0	—	ns	—	
		Hold Time	400 kHz mode	0	0.9	μs		
			1 MHz mode (Note 1)	0	0.3	μS		
IS30	TSU:STA	Start Condition	100 kHz mode	4700	—	ns	Only relevant for Repeated	
		Setup Time	400 kHz mode	600	—	ns	Start condition	
			1 MHz mode (Note 1)	250	_	ns		
IS31	THD:STA	Start Condition	100 kHz mode	4000		ns	After this period, the first	
		Hold Time	400 kHz mode	600	_	ns	clock pulse is generated	
			1 MHz mode (Note 1)	250	—	ns		
IS33	Tsu:sto	Stop Condition	100 kHz mode	4000	—	ns	_	
		Setup Time	400 kHz mode	600	—	ns]	
			1 MHz mode (Note 1)	600		ns		

TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

АС СНА	RACTERIS	STICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param. No.	Param. No. Symbol Characteristics				Max.	Units	Conditions		
IS34	THD:STO	Stop Condition	100 kHz mode	4000	_	ns	_		
		Hold Time	400 kHz mode	600	—	ns			
			1 MHz mode (Note 1)	250		ns			
IS40	TAA:SCL	Output Valid from	100 kHz mode	0	3500	ns	—		
		Clock	400 kHz mode	0	1000	ns			
			1 MHz mode (Note 1)	0	350	ns			
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus		
			400 kHz mode	1.3	—	μs	must be free before a new		
			1 MHz mode (Note 1)	0.5	_	μS	transmission can start		
IS50	Св	Bus Capacitive Lo	ading	—	400	pF	—		

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

32.1 DC Characteristics

TABLE 32-1: OPERATING MIPS VS. VOLTAGE

	Voo Bango	Tomp Bango	Max. Frequency
Characteristic	(in Volts) ⁽¹⁾	(in °C)	PIC32MX1XX/2XX/5XX 64/100-pin Family
MDC5	VBOR-3.6V	-40°C to +85°C	50 MHz

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for BOR values.

TABLE 32-2: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARA	CTERISTICS	5	Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial						
Parameter No.	Typical ⁽³⁾	Max.	Units	Conditions					
Operating (Current (IDD)	(Note 1, 2)							
MDC24	25	40	mA 50 MHz						

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD
- CPU executing while(1) statement from Flash
- **3:** RTCC and JTAG are disabled
- **4:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

32.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX/5XX 64/100-pin AC characteristics and timing parameters.

TABLE 32-5:	EXTERNAL CLOCK TIMING REQUIREMENTS
TABLE 32-5:	EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Op (unless othe Operating ter	perating Co erwise state mperature	onditions: 2.3 ed) -40°C ≤ TA ≤	V to 3.6\ +85°C fo	/ or Industrial	
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
MOS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4		50 50	MHz MHz	EC (Note 2) ECPLL (Note 1)

Note 1: PLL input requirements: $4 \text{ MHz} \le \text{FPLLIN} \le 5 \text{ MHz}$ (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.

2: This parameter is characterized, but not tested in manufacturing.

TABLE 32-6: SPIX MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
Param. No.	Symbol	Characteristics	Min. Typical Max. Units Conditions				Conditions
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	_	—	ns	_
MSP11	TscH	SCKx Output High Time (Note 1,2)	Тѕск/2		—	ns	_

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

TABLE 32-7:	SPIX MODULE MASTER MODE	(CKE = 1)	TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min. Typ. Max. Units Conditions				Conditions
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	—		ns	_
MSP11	TscH	SCKx Output High Time (Note 1,2)	Тѕск/2	—		ns	_

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

100-Lead Plastic Thin Quad Flatpack (PT)-12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		1	MILLIMETER	S
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing C			13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads C		0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B

APPENDIX A: REVISION HISTORY

Revision A (July 2014)

This is the initial released version of the document.

Revision B (September 2014)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-1.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
1.0 "Device Overview"	Added the USBOEN pin to the Pinout I/O Descriptions (see Table 1-1).
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Updated the Primary Oscillator loading capacitor calculations (see 2.8.1 "Crystal Oscillator Design Consideration ").
	Added 2.11 "Considerations When Interfacing to Remotely Powered Circuits"
10.0 "USB On-The-Go (OTG)"	Updated the UOEMON bit definitions (see Register 10-20).
31.0 "40 MHz Electrical Characteristics"	Updated DC Characteristics I/O Pin Input Specification parameters DI30 and DI31 (see Table 31-8).

Revision C (November 2014)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-2.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE A-2: MAJOR SECTION UPDATES

Section Name	Update Description
20.0 "Parallel Master Port (PMP)"	Added the RDSTART bit to the Parallel Port Control Register (see Table 20-1 and Register 20-1).
31.0 "40 MHz Electrical	Updated the IDD Operating Current DC Characteristics (see Table 31-5).
Characteristics"	Updated the IIDLE Idle Current DC Characteristics (see Table 31-6).
	Updated the IPD Power Down Current DC Characteristics (see Table 31-7).
	Updated the Internal FRC Accuracy (see Table 31-19).
32.0 "50 MHz Electrical	Updated the IDD Operating Current DC Characteristics (see Table 32-2).
Characteristics"	Updated the IIDLE Idle Current DC Characteristics (see Table 32-3).
	Updated the IPD Power Down Current DC Characteristics (see Table 32-4).

Revision D (April 2016)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-2.

Section Name	Update Description
1.0 "Device Overview"	Removed the USBOEN pin and all trace-related pins from the Pinout I/O Descriptions (see Table 1-1).
2.0 "Guidelines for Getting Started	Section 2.7 "Trace" was removed.
with 32-bit MCUs"	Section 2.10 "Sosc Design Recommendation" was removed.
3.0 "CPU"	References to the Shadow Register Set (SRS), which is not supported by PIC32MX1XX/2XX/5XX 64/100-pin Family devices, were removed from 3.1 "Features" , 3.2.1 "Execution Unit ", and Coprocessor 0 Registers (Table 3.2)
4.0 "Memory Organization"	The SFR Memory Map was added (see Table 4-1).
5.0 "Interrupt Controller"	The Single Vector Shadow Register Set (SSO) bit (INTCON<16>) was removed (see Register 5-1).
10.0 "USB On-The-Go (OTG)"	The UOEMON bit (U1CNFG1<6>) was removed (see Register 10-20).
23.0 "Controller Area Network	The CAN features (number of messages and FIFOs) were updated.
(CAN)"	The PIC32 CAN Block Diagram was updated (see Figure 23-1).
	The following registers were updated:
	C1FSTAT (see Register 23-6)
	C1RXOVF (see Register 23-7)
	C1RXFn (see Register 23-14)
	C1FIFOCONn (see Register 23-16)
	C1FIFOINTn (see Register 23-17)
	C1FIFOUAn (see Register 23-18)
	C1FIFOCIn (see Register 23-19)
	The C1FLTCON4 through C1FLTCON7 registers were removed.
28.0 "Special Features"	The virtual addresses for the Device Configuration Word registers were updated (see Table 28-1).
31.0 "40 MHz Electrical Characteristics"	The EJTAG Timing Characteristics diagram was updated (see Figure 31-23).

TABLE A-3: MAJOR SECTION UPDATES