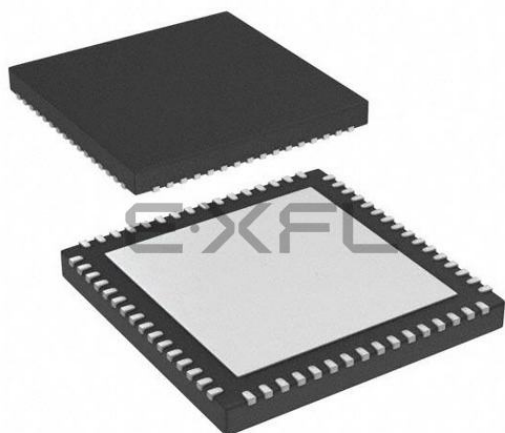




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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f256h-v-mr

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 1: PIC32MX1XX/2XX/5XX 64/100-PIN CONTROLLER FAMILY FEATURES

Device	Pins	Packages ⁽⁴⁾	Program Memory (KB) ⁽¹⁾	Data Memory (KB)	Remappable Peripherals					10-bit 1 Msps ADC (Channels)	Analog Comparators	USB On-The-Go (OTG)	CAN	CTMU	I ² C	PMP	RTCC	DMA Channels (Programmable/Dedicated)	I/O Pins	JTAG
					Remappable Pins	Timers/Capture/Compare ⁽²⁾	UART	SPI/I ² S	External Interrupts ⁽³⁾											
PIC32MX120F064H	64	QFN, TQFP	64+3	8	37	5/5/5	4	3	5	28	3	N	0	Y	2	Y	Y	4/0	53	Y
PIC32MX130F128H	64	QFN, TQFP	128+3	16	37	5/5/5	4	3	5	28	3	N	0	Y	2	Y	Y	4/0	53	Y
PIC32MX130F128L	100	TQFP	128+3	16	54	5/5/5	5	4	5	48	3	N	0	Y	2	Y	Y	4/0	85	Y
	100	TFBGA																		
PIC32MX230F128H	64	QFN, TQFP	128+3	16	37	5/5/5	4	3	5	28	3	Y	0	Y	2	Y	Y	4/2	49	Y
PIC32MX230F128L	100	TQFP	128+3	16	54	5/5/5	5	4	5	48	3	Y	0	Y	2	Y	Y	4/2	81	Y
	100	TFBGA																		
PIC32MX530F128H	64	QFN, TQFP	128+3	16	37	5/5/5	4	3	5	28	3	Y	1	Y	2	Y	Y	4/4	49	Y
PIC32MX530F128L	100	TQFP	128+3	16	54	5/5/5	5	4	5	48	3	Y	1	Y	2	Y	Y	4/4	81	Y
	100	TFBGA																		
PIC32MX150F256H	64	QFN, TQFP	256+3	32	37	5/5/5	4	3	5	28	3	N	0	Y	2	Y	Y	4/0	53	Y
PIC32MX150F256L	100	TQFP	256+3	32	54	5/5/5	5	4	5	48	3	N	0	Y	2	Y	Y	4/0	85	Y
	100	TFBGA																		
PIC32MX250F256H	64	QFN, TQFP	256+3	32	37	5/5/5	4	3	5	28	3	Y	0	Y	2	Y	Y	4/2	49	Y
PIC32MX250F256L	100	TQFP	256+3	32	54	5/5/5	5	4	5	48	3	Y	0	Y	2	Y	Y	4/2	81	Y
	100	TFBGA																		
PIC32MX550F256H	64	QFN, TQFP	256+3	32	37	5/5/5	4	3	5	28	3	Y	1	Y	2	Y	Y	4/4	49	Y
PIC32MX550F256L	100	TQFP	256+3	32	54	5/5/5	5	4	5	48	3	Y	1	Y	2	Y	Y	4/4	81	Y
	100	TFBGA																		
PIC32MX170F512H	64	QFN, TQFP	512+3	64	37	5/5/5	4	3	5	28	3	N	0	Y	2	Y	Y	4/0	53	Y
PIC32MX170F512L	100	TQFP	512+3	64	54	5/5/5	5	4	5	48	3	N	0	Y	2	Y	Y	4/0	85	Y
	100	TFBGA																		
PIC32MX270F512H	64	QFN, TQFP	512+3	64	37	5/5/5	4	3	5	28	3	Y	0	Y	2	Y	Y	4/2	49	Y
PIC32MX270F512L	100	TQFP	512+3	64	54	5/5/5	5	4	5	48	3	Y	0	Y	2	Y	Y	4/2	81	Y
	100	TFBGA																		
PIC32MX570F512H	64	QFN, TQFP	512+3	64	37	5/5/5	4	3	5	28	3	Y	1	Y	2	Y	Y	4/4	49	Y
PIC32MX570F512L	100	TQFP	512+3	64	54	5/5/5	5	4	5	48	3	Y	1	Y	2	Y	Y	4/4	81	Y
	100	TFBGA																		

- Note**
- 1: All devices feature 3 KB of Boot Flash memory.
 - 2: Four out of five timers are remappable.
 - 3: Four out of five external interrupts are remappable.
 - 4: Please contact your local Microchip Sales Office for information regarding the availability of devices in the 100-pin TFBGA package.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP			
AN0	16	25	I	Analog	Analog input channels.
AN1	15	24	I	Analog	
AN2	14	23	I	Analog	
AN3	13	22	I	Analog	
AN4	12	21	I	Analog	
AN5	11	20	I	Analog	
AN6	17	26	I	Analog	
AN7	18	27	I	Analog	
AN8	21	32	I	Analog	
AN9	22	33	I	Analog	
AN10	23	34	I	Analog	
AN11	24	35	I	Analog	
AN12	27	41	I	Analog	
AN13	28	42	I	Analog	
AN14	29	43	I	Analog	
AN15	30	44	I	Analog	
AN16	4	10	I	Analog	
AN17	5	11	I	Analog	
AN18	6	12	I	Analog	
AN19	8	14	I	Analog	
AN20	62	98	I	Analog	
AN21	64	100	I	Analog	
AN22	1	3	I	Analog	
AN23	2	4	I	Analog	
AN24	49	76	I	Analog	
AN25	50	77	I	Analog	
AN26	51	78	I	Analog	
AN27	3	5	I	Analog	
AN28	—	1	I	Analog	
AN29	—	6	I	Analog	
AN30	—	7	I	Analog	
AN31	—	8	I	Analog	
AN32	—	18	I	Analog	
AN33	—	19	I	Analog	
AN34	—	39	I	Analog	
AN35	—	40	I	Analog	

Legend: CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

- Note 1:** This pin is only available on devices without a USB module.
2: This pin is only available on devices with a USB module.
3: This pin is not available on 64-pin devices with a USB module.
4: This pin is only available on 100-pin devices without a USB module.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 5-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION

Interrupt Source ⁽¹⁾	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
			Flag	Enable	Priority	Sub-priority	
Highest Natural Order Priority							
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
INT0 – External Interrupt	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
IC1E – Input Capture 1 Error	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
IC1 – Input Capture 1	6	5	IFS0<6>	IEC0<6>	IPC1<12:10>	IPC1<9:8>	Yes
OC1 – Output Compare 1	7	6	IFS0<7>	IEC0<7>	IPC1<20:18>	IPC1<17:16>	No
INT1 – External Interrupt 1	8	7	IFS0<8>	IEC0<8>	IPC1<28:26>	IPC1<25:24>	No
T2 – Timer2	9	8	IFS0<9>	IEC0<9>	IPC2<4:2>	IPC2<1:0>	No
IC2E – Input Capture 2	10	9	IFS0<10>	IEC0<10>	IPC2<12:10>	IPC2<9:8>	Yes
IC2 – Input Capture 2	11	9	IFS0<11>	IEC0<11>	IPC2<12:10>	IPC2<9:8>	Yes
OC2 – Output Compare 2	12	10	IFS0<12>	IEC0<12>	IPC2<20:18>	IPC2<17:16>	No
INT2 – External Interrupt 2	13	11	IFS0<13>	IEC0<13>	IPC2<28:26>	IPC2<25:24>	No
T3 – Timer3	14	12	IFS0<14>	IEC0<14>	IPC3<4:2>	IPC3<1:0>	No
IC3E – Input Capture 3	15	13	IFS0<15>	IEC0<15>	IPC3<12:10>	IPC3<9:8>	Yes
IC3 – Input Capture 3	16	13	IFS0<16>	IEC0<16>	IPC3<12:10>	IPC3<9:8>	Yes
OC3 – Output Compare 3	17	14	IFS0<17>	IEC0<17>	IPC3<20:18>	IPC3<17:16>	No
INT3 – External Interrupt 3	18	15	IFS0<18>	IEC0<18>	IPC3<28:26>	IPC3<25:24>	No
T4 – Timer4	19	16	IFS0<19>	IEC0<19>	IPC4<4:2>	IPC4<1:0>	No
IC4E – Input Capture 4 Error	20	17	IFS0<20>	IEC0<20>	IPC4<12:10>	IPC4<9:8>	Yes
IC4 – Input Capture 4	21	17	IFS0<21>	IEC0<21>	IPC4<12:10>	IPC4<9:8>	Yes
OC4 – Output Compare 4	22	18	IFS0<22>	IEC0<22>	IPC4<20:18>	IPC4<17:16>	No
INT4 – External Interrupt 4	23	19	IFS0<23>	IEC0<23>	IPC4<28:26>	IPC4<25:24>	No
T5 – Timer5	24	20	IFS0<24>	IEC0<24>	IPC5<4:2>	IPC5<1:0>	No
IC5E – Input Capture 5 Error	25	21	IFS0<25>	IEC0<25>	IPC5<12:10>	IPC5<9:8>	Yes
IC5 – Input Capture 5	26	21	IFS0<26>	IEC0<26>	IPC5<12:10>	IPC5<9:8>	Yes
OC5 – Output Compare 5	27	22	IFS0<27>	IEC0<27>	IPC5<20:18>	IPC5<17:16>	No
AD1 – ADC1 Convert done	28	23	IFS0<28>	IEC0<28>	IPC5<28:26>	IPC5<25:24>	Yes
FSCM – Fail-Safe Clock Monitor	29	24	IFS0<29>	IEC0<29>	IPC6<4:2>	IPC6<1:0>	No
RTCC – Real-Time Clock and Calendar	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>	No
FCE – Flash Control Event	31	26	IFS0<31>	IEC0<31>	IPC6<20:18>	IPC6<17:16>	No
CMP1 – Comparator Interrupt	32	27	IFS1<0>	IEC1<0>	IPC6<28:26>	IPC6<25:24>	No
CMP2 – Comparator Interrupt	33	28	IFS1<1>	IEC1<1>	IPC7<4:2>	IPC7<1:0>	No
USB – USB Interrupts	34	29	IFS1<2>	IEC1<2>	IPC7<12:10>	IPC7<9:8>	Yes
SPI1E – SPI1 Fault	35	30	IFS1<3>	IEC1<3>	IPC7<20:18>	IPC7<17:16>	Yes
SPI1RX – SPI1 Receive Done	36	30	IFS1<4>	IEC1<4>	IPC7<20:18>	IPC7<17:16>	Yes
SPI1TX – SPI1 Transfer Done	37	30	IFS1<5>	IEC1<5>	IPC7<20:18>	IPC7<17:16>	Yes
U1E – UART1 Fault	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>	Yes
U1RX – UART1 Receive Done	39	31	IFS1<7>	IEC1<7>	IPC7<28:26>	IPC7<25:24>	Yes
U1TX – UART1 Transfer Done	40	31	IFS1<8>	IEC1<8>	IPC7<28:26>	IPC7<25:24>	Yes
I2C1B – I2C1 Bus Collision Event	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>	Yes
I2C1S – I2C1 Slave Event	42	32	IFS1<10>	IEC1<10>	IPC8<4:2>	IPC8<1:0>	Yes
I2C1M – I2C1 Master Event	43	32	IFS1<11>	IEC1<11>	IPC8<4:2>	IPC8<1:0>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX1XX/2XX/5XX 64/100-pin Controller Family Features”** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

7.1 Control Registers

TABLE 7-1: RESET SFR SUMMARY

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F600	RCON	31:16	—	—	HVDR	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CMR	VREGS	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	xxxx ⁽¹⁾
F610	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000

Legend: — = unimplemented, read as '0'. Address offset values are shown in hexadecimal.

Note 1: The Reset value is dependent on the DEVCFGx Configuration bits and the type of reset.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 8-4: REFOTRIM: REFERENCE OSCILLATOR TRIM REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ROTRIM<8:1>							
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ROTRIM<0>	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

y = Value set from Configuration bits on POR
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-23 **ROTRIM<8:0>**: Reference Oscillator Trim bits

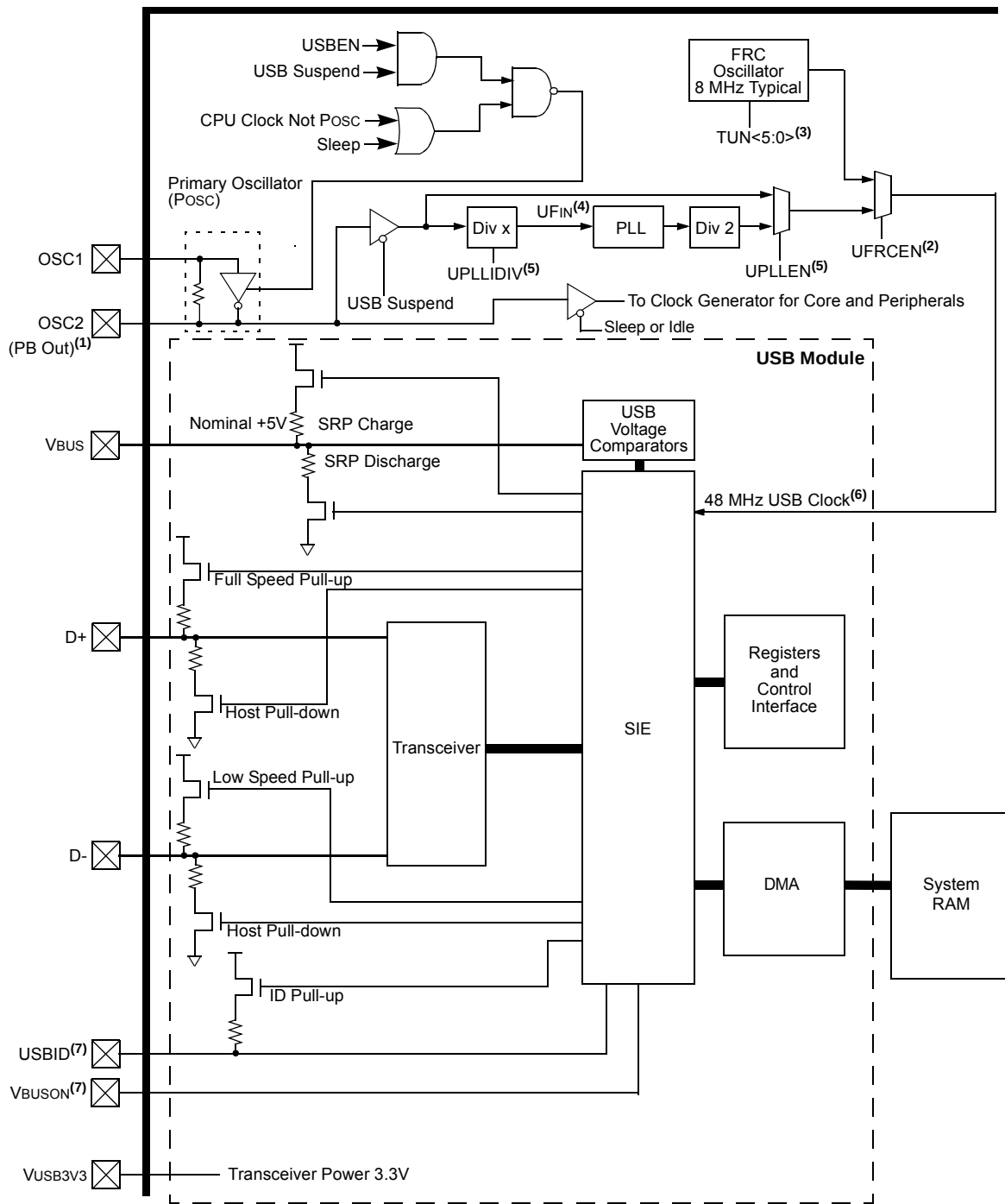
11111111 = 511/512 divisor added to RODIV value
11111110 = 510/512 divisor added to RODIV value
.
.
.
10000000 = 256/512 divisor added to RODIV value
.
.
.
00000010 = 2/512 divisor added to RODIV value
00000001 = 1/512 divisor added to RODIV value
00000000 = 0/512 divisor added to RODIV value

bit 22-0 **Unimplemented**: Read as '0'

Note: While the ON bit (REFOCON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

FIGURE 10-1: PIC32MX1XX/2XX/5XX USB INTERFACE DIAGRAM



- Note 1:** PB clock is only available on this pin for select EC modes.
- Note 2:** This bit field is contained in the OSCCON register.
- Note 3:** This bit field is contained in the OSCTRM register.
- Note 4:** USB PLL UFIN requirements: 4 MHz.
- Note 5:** This bit field is contained in the DEVCFG2 register.
- Note 6:** A 48 MHz clock is required for proper USB operation.
- Note 7:** Pins can be used as GPIO when the USB module is disabled or if the USB is enabled but DEVCFG3<31:30> = '0b00.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 10-4: U1OTGCON: USB OTG CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **DPPULUP:** D+ Pull-Up Enable bit

1 = D+ data line pull-up resistor is enabled

0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit

1 = D- data line pull-up resistor is enabled

0 = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit

1 = D+ data line pull-down resistor is enabled

0 = D+ data line pull-down resistor is disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit

1 = D- data line pull-down resistor is enabled

0 = D- data line pull-down resistor is disabled

bit 3 **VBUSON:** VBUS Power-on bit

1 = VBUS line is powered

0 = VBUS line is not powered

bit 2 **OTGEN:** OTG Functionality Enable bit

1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control

0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 **VBUSCHG:** VBUS Charge Enable bit

1 = VBUS line is charged through a pull-up resistor

0 = VBUS line is not charged through a resistor

bit 0 **VBUSDIS:** VBUS Discharge Enable bit

1 = VBUS line is discharged through a pull-down resistor

0 = VBUS line is not discharged through a resistor

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

11.1 Parallel I/O (PIO) Ports

All port pins have ten registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin, regardless of the output function including PPS remapped output functions to act as an open-drain output. The only exception is the I²C pins that are open drain by default.

The open-drain feature allows the presence of outputs higher than VDD (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

See the “**Device Pin Tables**” section for the available pins and their functionality.

11.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default. The ANSELx register bit, when cleared, disables the corresponding digital input buffer pin(s).

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module. The TRISx bits only control the corresponding digital output buffer pin(s).

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level; i.e., when ANSELx = 1; TRISx = x).

Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be an NOP.

11.1.4 INPUT CHANGE NOTIFICATION

The input Change Notification (CN) function of the I/O ports allows the PIC32MX1XX/2XX/5XX 64/100-pin devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Five control registers are associated with the CN functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit.

11.1.5 INTERNALLY SELECTABLE PULL-UPS AND PULL-DOWNS

Each I/O pin also has a weak pull-up and every I/O pin has a weak pull-down connected to it, which are independent of any other I/O pin functionality (i.e., PPS, Open Drain, or CN). The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note: Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output. They should also be disabled on 5V tolerant pins when the pin voltage can exceed VDD.

An additional control register (CNCONx) is shown in Register 11-3.

11.2 CLR, SET, and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 11-2: OUTPUT PIN SELECTION (CONTINUED)

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD9	RPD9R	RPD9R<3:0>	0000 = No Connect
RPG6	RPG6R	RPG6R<3:0>	0001 = U3RTS
RPB8	RPB8R	RPB8R<3:0>	0010 = U4TX
RPB15	RPB15R	RPB15R<3:0>	0011 = REFCLKO
RPD4	RPD4R	RPD4R<3:0>	0100 = U5TX ⁽³⁾
RPB0	RPB0R	RPB0R<3:0>	0101 = Reserved
RPE3	RPE3R	RPE3R<3:0>	0110 = Reserved
RPB7	RPB7R	RPB7R<3:0>	0111 = $\overline{SS1}$
RPB2	RPB2R	RPB2R<3:0>	1000 = SDO1
RPF12 ⁽³⁾	RPF12R	RPF12R<3:0>	1001 = Reserved
RPD12 ⁽³⁾	RPD12R	RPD12R<3:0>	1010 = Reserved
RPF8 ⁽³⁾	RPF8R	RPF8R<3:0>	1011 = OC5
RPC3 ⁽³⁾	RPC3R	RPC3R<3:0>	1100 = Reserved
RPE9 ⁽³⁾	RPE9R	RPE9R<3:0>	1101 = C1OUT
			1110 = $\overline{SS3}$
			1111 = $\overline{SS4}$ ⁽³⁾
RPD1	RPD1R	RPD1R<3:0>	0000 = No Connect
RPG9	RPG9R	RPG9R<3:0>	0001 = $\overline{U2RTS}$
RPB14	RPB14R	RPB14R<3:0>	0010 = Reserved
RPD0	RPD0R	RPD0R<3:0>	0011 = $\overline{U1RTS}$
RPD8	RPD8R	RPD8R<3:0>	0100 = U5TX ⁽³⁾
RPB6	RPB6R	RPB6R<3:0>	0101 = Reserved
RPD5	RPD5R	RPD5R<3:0>	0110 = $\overline{SS2}$
RPF3 ⁽¹⁾	RPF3R	RPF3R<3:0>	0111 = Reserved
RPF6 ⁽²⁾	RPF6R	RPF6R<3:0>	1000 = SDO1
RPF13 ⁽³⁾	RPF13R	RPF13R<3:0>	1001 = Reserved
RPC2 ⁽³⁾	RPC2R	RPC2R<3:0>	1010 = Reserved
RPE8 ⁽³⁾	RPE8R	RPE8R<3:0>	1011 = OC2
RPF2 ⁽¹⁾	RPF2R	RPF2R<3:0>	1100 = OC1
			1101 = Reserved
			1110 = Reserved
			1111 = Reserved

- Note 1:** This selection is not available on 64-pin USB devices.
- 2:** This selection is only available on 100-pin General Purpose devices.
- 3:** This selection is not available on 64-pin devices.
- 4:** This selection is not available when USBID functionality is used on USB devices.
- 5:** This selection is not available on devices without a CAN module.
- 6:** This selection is not available on USB devices.
- 7:** This selection is not available when VBUSON functionality is used on USB devices.

TABLE 11-4: PORTB REGISTER MAP

Virtual Address (BF88_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6100	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSELB15	ANSELB14	ANSELB13	ANSELB12	ANSELB11	ANSELB10	ANSELB9	ANSELB8	ANSELB7	ANSELB6	ANSELB5	ANSELB4	ANSELB3	ANSELB2	ANSELB1	ANSELB0	FFFF
6110	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
6120	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
6130	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
6140	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
6150	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
6160	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
6170	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6180	CNENB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
6190	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATB15	CN STATB14	CN STATB13	CN STATB12	CN STATB11	CN STATB10	CN STATB9	CN STATB8	CN STATB7	CN STATB6	CN STATB5	CN STATB4	CN STATB3	CN STATB2	CN STATB1	CN STATB0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET, and INV Registers” for more information.

15.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. “Input Capture”** (DS60001122) of the “*PIC32 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com/PIC32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- Simple capture event modes:
 - Capture timer value on every falling edge of input at ICx pin
 - Capture timer value on every rising edge of input at ICx pin
 - Capture timer value on every edge (rising and falling)
 - Capture timer value on every edge (rising and falling), specified edge first.

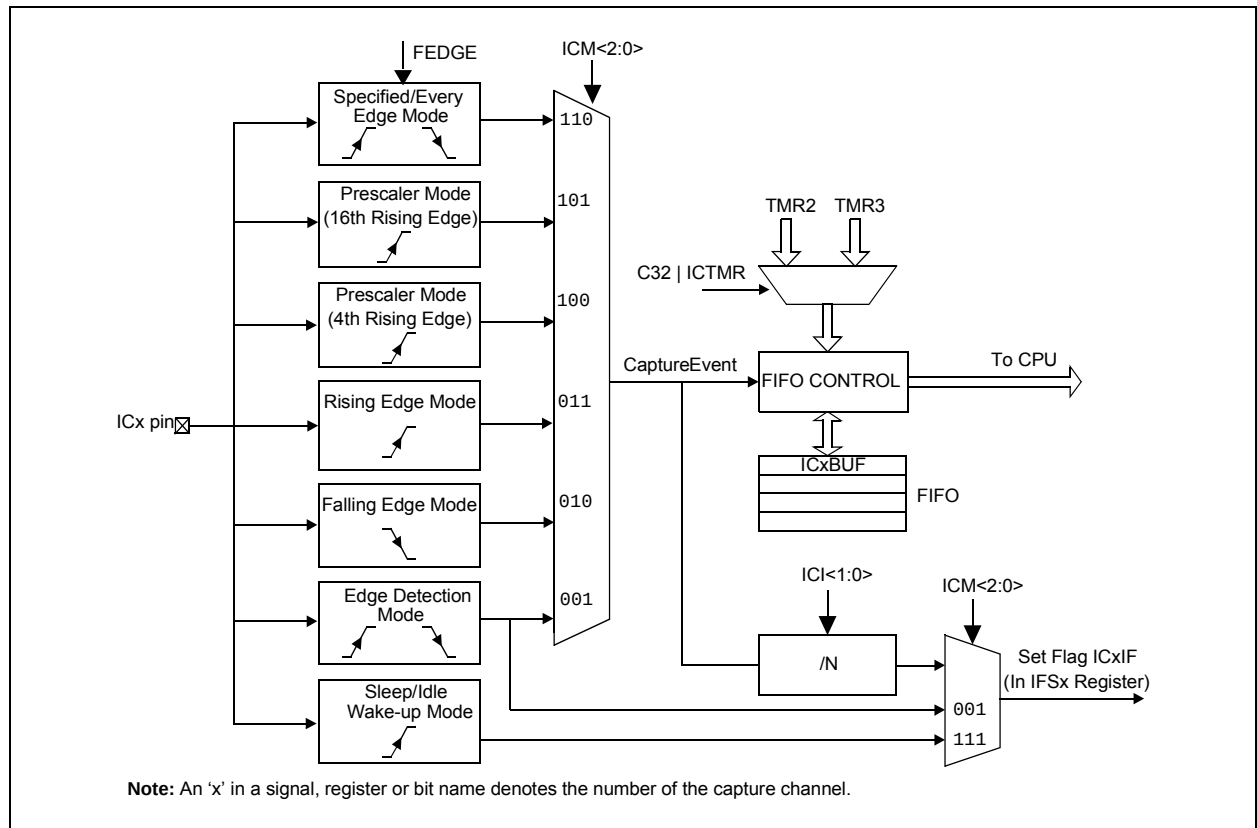
- Prescaler capture event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

The other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values
Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM



18.1 Control Registers

TABLE 18-1: I2C1 AND I2C2 REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	I2C1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	BFFF
5010	I2C1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
5020	I2C1ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Register										0000
5030	I2C1MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Mask Register										0000
5040	I2C1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5050	I2C1TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	Transmit Register									
5060	I2C1RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	Receive Register									
5100	I2C2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	BFFF
5110	I2C2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
5120	I2C2ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Register										0000
5130	I2C2MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Mask Register										0000
5140	I2C2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5150	I2C2TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	Transmit Register									
5160	I2C2RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	Receive Register									

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

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REGISTER 19-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 5 **ABAUD**: Auto-Baud Enable bit
 1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55);
 cleared by hardware upon completion
 0 = Baud rate measurement disabled or completed
- bit 4 **RXINV**: Receive Polarity Inversion bit
 1 = UxRX Idle state is '0'
 0 = UxRX Idle state is '1'
- bit 3 **BRGH**: High Baud Rate Enable bit
 1 = High-Speed mode – 4x baud clock enabled
 0 = Standard Speed mode – 16x baud clock enabled
- bit 2-1 **PDSEL<1:0>**: Parity and Data Selection bits
 11 = 9-bit data, no parity
 10 = 8-bit data, odd parity
 01 = 8-bit data, even parity
 00 = 8-bit data, no parity
- bit 0 **STSEL**: Stop Selection bit
 1 = 2 Stop bits
 0 = 1 Stop bit

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSClk cycle immediately following the instruction that clears the module's ON bit.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 23-12: C1FLTCON2: CAN FILTER CONTROL REGISTER 2 (CONTINUED)

- bit 20-16 **FSEL10<4:0>**: FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0
- bit 15 **FLTEN9**: Filter 9 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 14-13 **MSEL9<1:0>**: Filter 9 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 12-8 **FSEL9<4:0>**: FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0
- bit 7 **FLTEN8**: Filter 8 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 6-5 **MSEL8<1:0>**: Filter 8 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 4-0 **FSEL8<4:0>**: FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

26.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

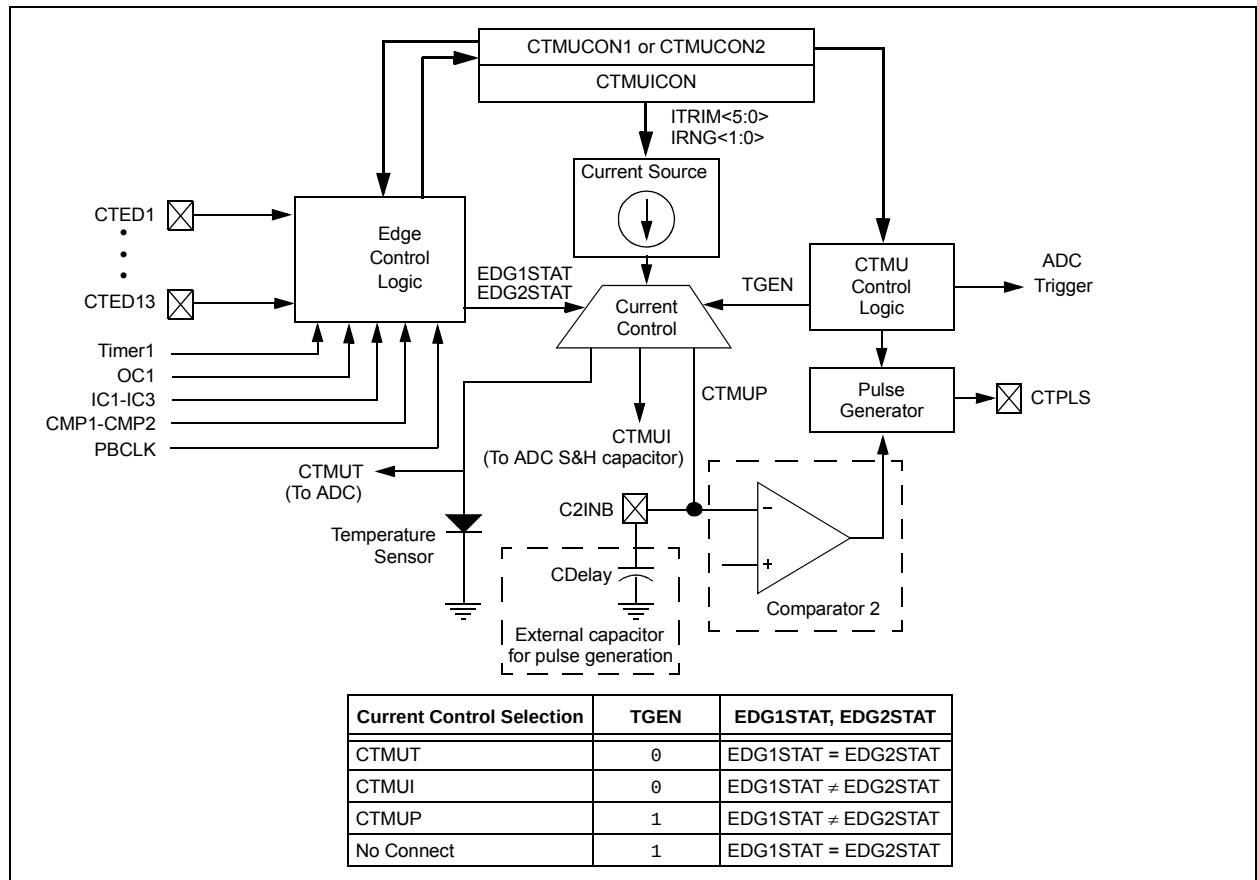
The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.

The CTMU module includes the following key features:

- Up to 13 channels available for capacitive or time measurement input
- On-chip precision current source
- 16-edge input trigger sources
- Selection of edge or level-sensitive inputs
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- Integrated temperature sensing diode
- Control of current source during auto-sampling
- Four current source ranges
- Time measurement resolution of one nanosecond

A block diagram of the CTMU is shown in Figure 26-1.

FIGURE 26-1: CTMU BLOCK DIAGRAM



PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

FIGURE 31-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

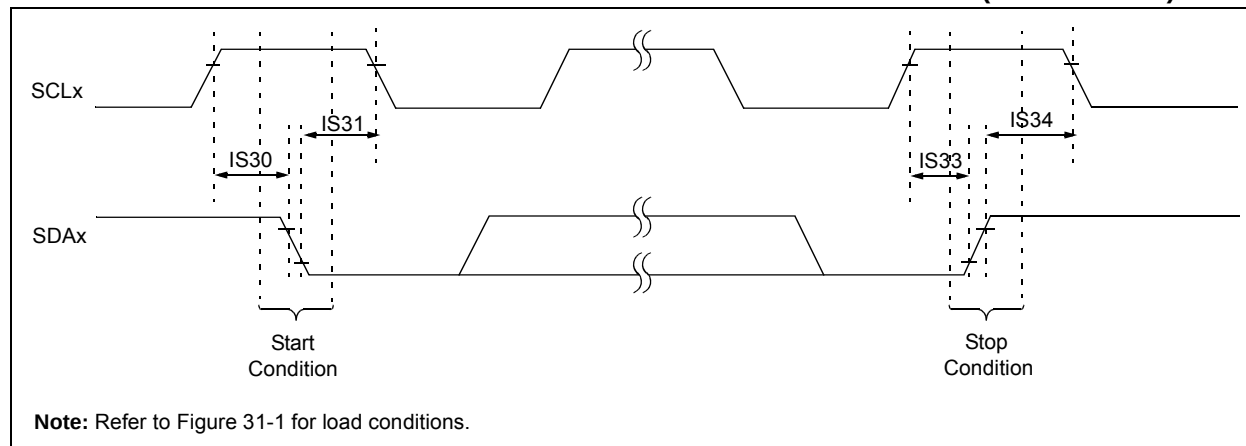
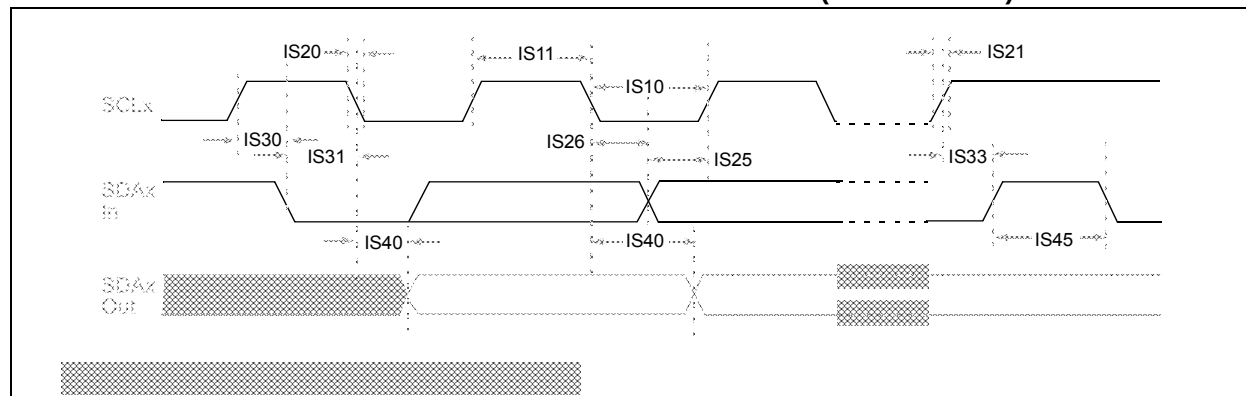
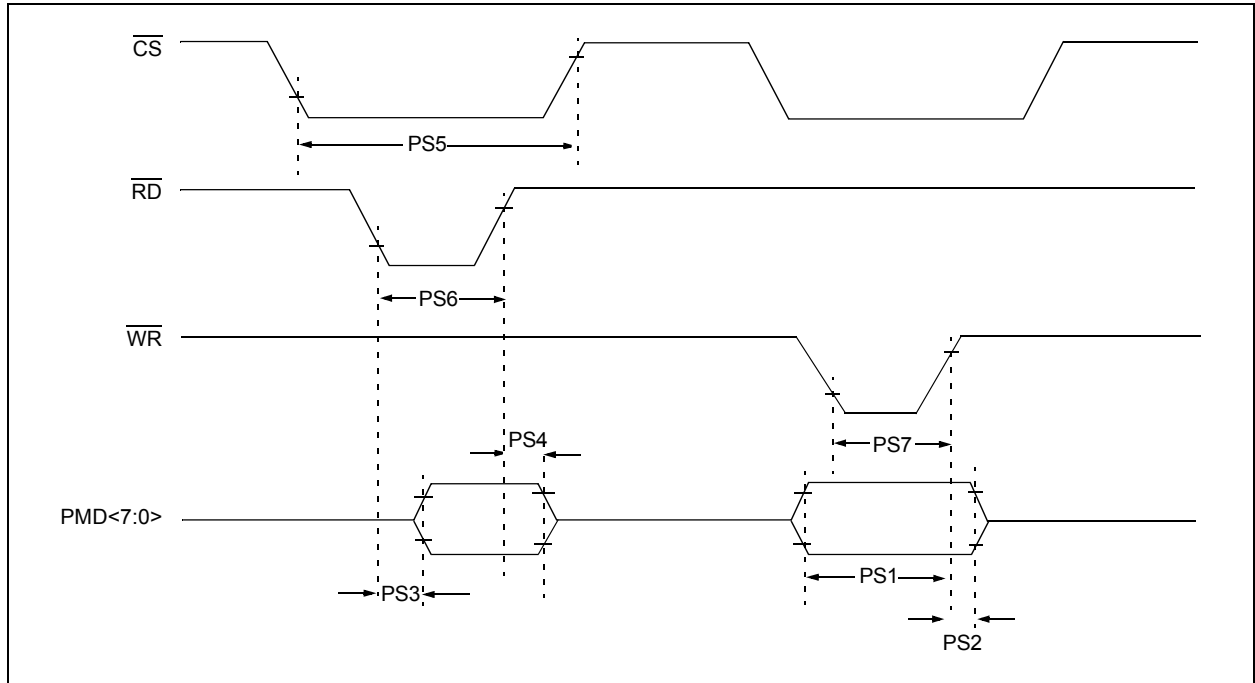


FIGURE 31-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

FIGURE 31-20: PARALLEL SLAVE PORT TIMING



PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 31-41: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
CTMU CURRENT SOURCE							
CTMUI1	IOUT1	Base Range ⁽¹⁾	—	0.55	—	μA	CTMUCON<9:8> = 01
CTMUI2	IOUT2	10x Range ⁽¹⁾	—	5.5	—	μA	CTMUCON<9:8> = 10
CTMUI3	IOUT3	100x Range ⁽¹⁾	—	55	—	μA	CTMUCON<9:8> = 11
CTMUI4	IOUT4	1000x Range ⁽¹⁾	—	550	—	μA	CTMUCON<9:8> = 00
CTMUUFV1	VF	Temperature Diode Forward Voltage ^(1,2)	—	0.598	—	V	T _A = +25°C, CTMUCON<9:8> = 01
			—	0.658	—	V	T _A = +25°C, CTMUCON<9:8> = 10
			—	0.721	—	V	T _A = +25°C, CTMUCON<9:8> = 11
CTMUUFV2	VFVR	Temperature Diode Rate of Change ^(1,2)	—	-1.92	—	mV/°C	CTMUCON<9:8> = 01
			—	-1.74	—	mV/°C	CTMUCON<9:8> = 10
			—	-1.56	—	mV/°C	CTMUCON<9:8> = 11

Note 1: Nominal value at center point of current trim range (CTMUCON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksp/s
- All PMD bits are cleared (PMDx = 0)
- Executing a while(1) statement
- Device operating from the FRC with no PLL

3: The CTMU module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

32.0 50 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX/5XX 64/100-pin Family electrical characteristics for devices operating at 50 MHz.

The specifications for 50 MHz are identical to those shown in **Section 31.0 “40 MHz Electrical Characteristics”**, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter “M”, which denotes 50 MHz operation. For example, parameter DC29a in **Section 31.0 “40 MHz Electrical Characteristics”**, is the up to 40 MHz operation equivalent for MDC29a.

Absolute maximum ratings for the PIC32MX1XX/2XX/5XX 64/100-pin Family 50 MHz devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias	-40°C to +85°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS (Note 3)	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.3V (Note 3)	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V (Note 3)	-0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3	-0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of VSS pin(s)	300 mA
Maximum current into VDD pin(s) (Note 2)	300 mA
Maximum output current sunk by any I/O pin	15 mA
Maximum output current sourced by any I/O pin	15 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports (Note 2)	200 mA

Note 1: Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

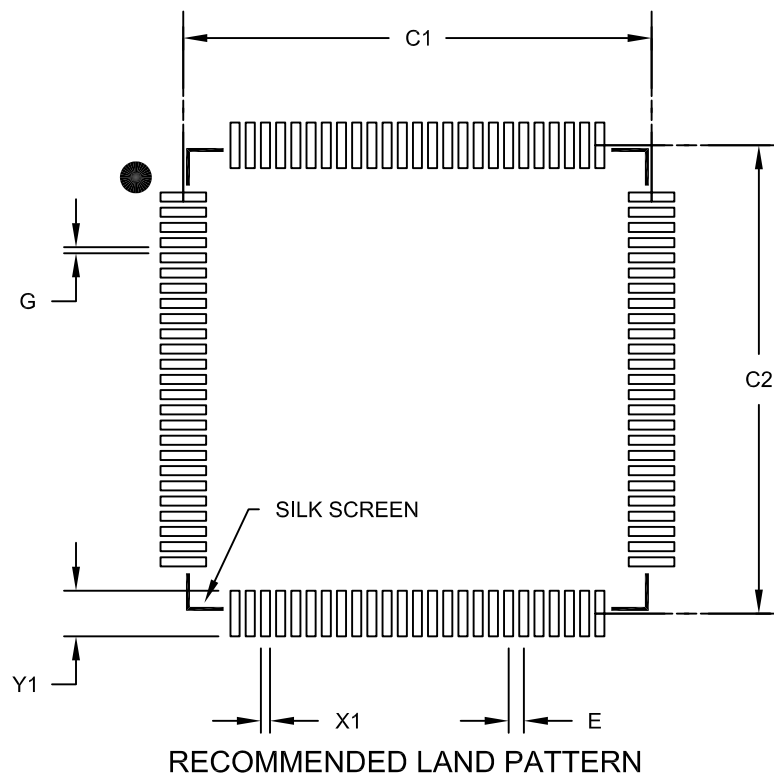
2: Maximum allowable current is a function of device maximum power dissipation (see Table 32-2).

3: See the “**Device Pin Tables**” section for the 5V tolerant pins.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X100)	X1			0.30
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B