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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f256ht-v-mr

TABLE 4: PIN NAMES FOR 100-PIN GENERAL PURPOSE DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MX130F128L
PIC32MX150F256L
PIC32MX170F512L

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN28/RG15	36	Vss
2	VDD	37	VDD
3	AN22/RPE5/PMD5/RE5	38	TCK/CTED2/RA1
4	AN23/PMD6/RE6	39	AN34/RPF13/SCK3/RF13
5	AN27/PMD7/RE7	40	AN35/RPF12/RF12
6	AN29/RPC1/RC1	41	AN12/PMA11/RB12
7	AN30/RPC2/RC2	42	AN13/PMA10/RB13
8	AN31/RPC3/RC3	43	AN14/RPB14/CTED5/PMA1/RB14
9	RPC4/CTED7/RC4	44	AN15/RPB15/OCFB/CTED6/PMA0/RB15
10	AN16/C1IND/RPG6/SCK2/PMA5/RG6	45	Vss
11	AN17/C1INC/RPG7/PMA4/RG7	46	VDD
12	AN18/C2IND/RPG8/PMA3/RG8	47	AN36/RPD14/RD14
13	MCLR	48	AN37/RPD15/SCK4/RD15
14	AN19/C2INC/RPG9/PMA2/RG9	49	RPF4/PMA9/RF4
15	Vss	50	RPF5/PMA8/RF5
16	VDD	51	RPF3/RF3
17	TMS/CTED1/RA0	52	AN38/RPF2/RF2
18	AN32/RPE8/RE8	53	AN39/RPF8/RF8
19	AN33/RPE9/RE9	54	RPF7/RF7
20	AN5/C1INA/RPB5/RB5	55	RPF6/SCK1/INT0/RF6
21	AN4/C1INB/RB4	56	SDA1/RG3
22	PGED3/AN3/C2INA/RPB3/RB3	57	SCL1/RG2
23	PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2	58	SCL2/RA2
24	PGEC1/AN1/RPB1/CTED12/RB1	59	SDA2/RA3
25	PGED1/AN0/RPB0/RB0	60	TDI/CTED9/RA4
26	PGEC2/AN6/RPB6/RB6	61	TDO/RA5
27	PGED2/AN7/RPB7/CTED3/RB7	62	VDD
28	VREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	Vss
31	AVss	66	RPA14/RA14
32	AN8/RPB8/CTED10/RB8	67	RPA15/RA15
33	AN9/RPB9/CTED4/RB9	68	RPD8/RTCC/RD8
34	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	69	RPD9/RD9
35	AN11/PMA12/RB11	70	RPD10/PMA15/RD10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 1-1:   PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP			
RF0	58	87	I/O	ST	PORTF is a bidirectional I/O port
RF1	59	88	I/O	ST	
RF2	34[3]	52	I/O	ST	
RF3	33	51	I/O	ST	
RF4	31	49	I/O	ST	
RF5	32	50	I/O	ST	
RF6	35[1]	55[1]	I/O	ST	
RF7	—	54[4]	I/O	ST	
RF8	—	53	I/O	ST	
RF12	—	40	I/O	ST	
RF13	—	39	I/O	ST	
RG0	—	90	I/O	ST	PORTG is a bidirectional I/O port
RG1	—	89	I/O	ST	
RG2	37[1]	57[1]	I/O	ST	
RG3	36[1]	56[1]	I/O	ST	
RG6	4	10	I/O	ST	
RG7	5	11	I/O	ST	
RG8	6	12	I/O	ST	
RG9	8	14	I/O	ST	
RG12	—	96	I/O	ST	
RG13	—	97	I/O	ST	
RG14	—	95	I/O	ST	
RG15	—	1	I/O	ST	
T1CK	48	74	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	I	ST	Timer5 External Clock Input
$\overline{U1CTS}$	PPS	PPS	I	ST	UART1 Clear to Send
$\overline{U1RTS}$	PPS	PPS	O	—	UART1 Ready to Send
U1RX	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	O	—	UART1 Transmit
$\overline{U2CTS}$	PPS	PPS	I	ST	UART2 Clear to Send
$\overline{U2RTS}$	PPS	PPS	O	—	UART2 Ready to Send
U2RX	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	O	—	UART2 Transmit

Legend: CMOS = CMOS compatible input or output   Analog = Analog input   I = Input   O = Output
ST = Schmitt Trigger input with CMOS levels   TTL = TTL input buffer   P = Power

Note 1: This pin is only available on devices without a USB module.
   2: This pin is only available on devices with a USB module.
   3: This pin is not available on 64-pin devices with a USB module.
   4: This pin is only available on 100-pin devices without a USB module.

The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (`MFHI`) and Move-From-LO (`MFLO`) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32® architecture also defines a multiply instruction, `MUL`, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit `MFLO` instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (`MADD`) and Multiply-Subtract (`MSUB`), are used to perform the multiply-accumulate and multiply-subtract operations. The `MADD` instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the `MSUB` instruction multiplies two operands and then subtracts the product from the HI and LO registers. The `MADD` and `MSUB` operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e®, is also available by accessing the CP0 registers, listed in Table 3-2.

TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core.
7	HWREna	Enables access via the `RDHWR` instruction to selected hardware registers.
8	BadVAddr[1]	Reports the address for the most recent address-related exception.
9	Count[1]	Processor cycle count.
10	Reserved	Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core.
11	Compare[1]	Timer interrupt control.
12	Status[1]	Processor status and control.
12	IntCtl[1]	Interrupt system status and control.
13	Cause[1]	Cause of last general exception.
14	EPC[1]	Program counter at last exception.
15	PRId	Processor identification and revision.
15	EBASE	Exception vector base register.
16	Config	Configuration register.
16	Config1	Configuration register 1.
16	Config2	Configuration register 2.
16	Config3	Configuration register 3.
17-22	Reserved	Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core.
23	Debug[2]	Debug control and exception status.
24	DEPC[2]	Program counter at last debug exception.
25-29	Reserved	Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core.
30	ErrorEPC[1]	Program counter at last error.
31	DESAVE[2]	Debug handler scratchpad register.

Note 1: Registers used in exception processing.

2: Registers used during debug.

6.0 FLASH PROGRAM MEMORY

Note:	This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual".*

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the "*PIC32 Flash Programming Specification*" (DS60001145), which can be downloaded from the Microchip web site.

Note:	On PIC32MX1XX/2XX/5XX 64/100-pin devices, the Flash page size is 1 KB and the row size is 128 bytes (256 IW and 32 IW, respectively).

FIGURE 8-1: **PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY CLOCK DIAGRAM**

Notes: 1. A series resistor, R_S, may be required for AT strip cut crystals or eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, R_P, with a value of 1 MΩ.
   2. The internal feedback resistor, R_F, is typically in the range of 2 MΩ to 10 MΩ.
   3. Refer to **Section 6. "Oscillator Configuration"** (DS60001112) in the "*PIC32 Family Reference Manual*" for determining the best oscillator components.
   4. PBCLK out is available on the OSC2 pin in certain clock modes.
   5. USB PLL is available on PIC32MX2XX/5XX devices only.

TABLE 10-1: USB REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

18.0 INTER-INTEGRATED CIRCUIT (I^{2}C)

> **Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit (I^{2}C)"** (DS60001116) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The I^{2}C module provides complete hardware support for both Slave and Multi-Master modes of the I^{2}C serial communication standard. Figure 18-1 illustrates the I^{2}C module block diagram.

Each I^{2}C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I^{2}C module offers the following key features:

- I^{2}C interface supporting both master and slave operation
- I^{2}C Slave mode supports 7-bit and 10-bit addressing
- I^{2}C Master mode supports 7-bit and 10-bit addressing
- I^{2}C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I^{2}C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I^{2}C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking

FIGURE 18-1: **I²C BLOCK DIAGRAM**
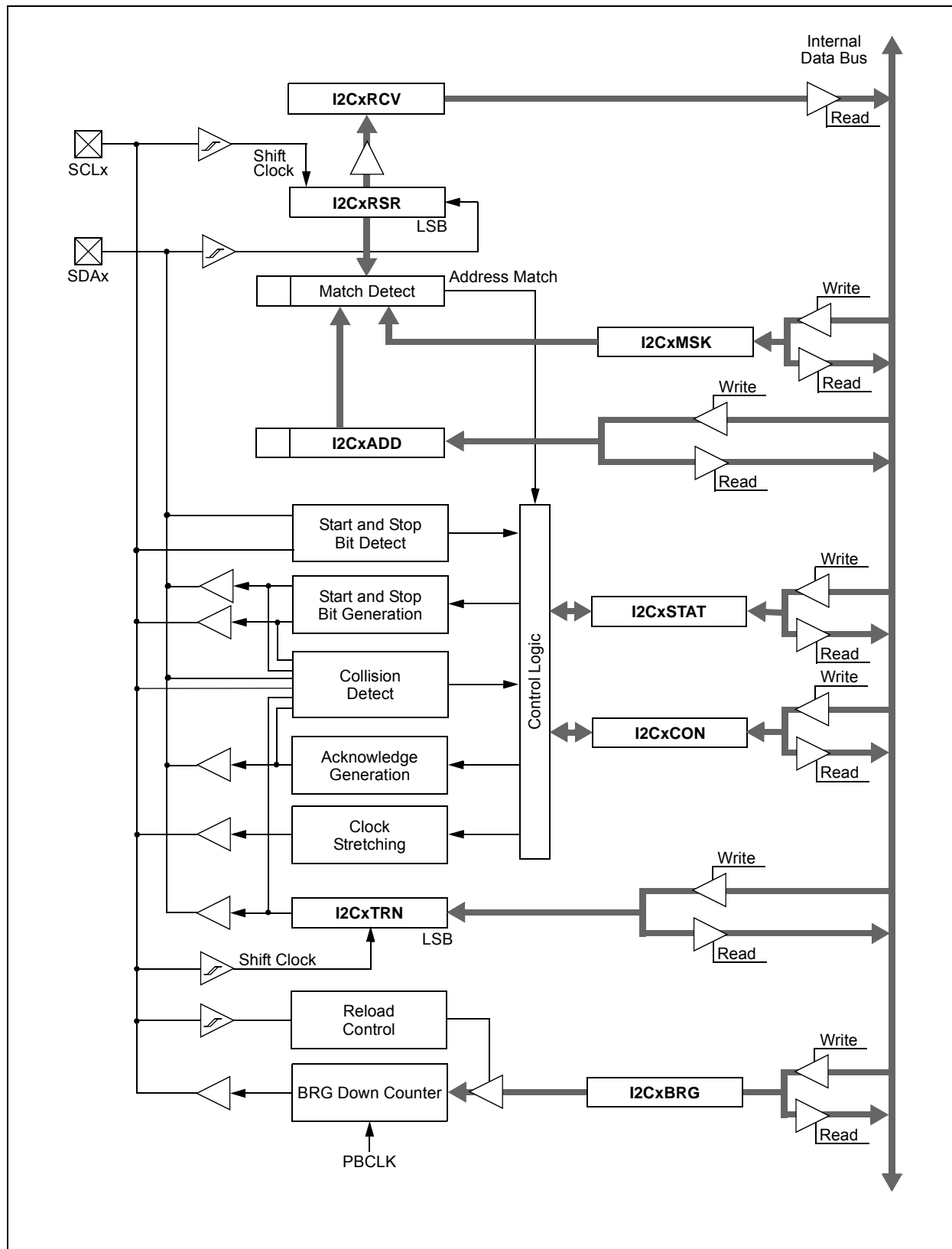
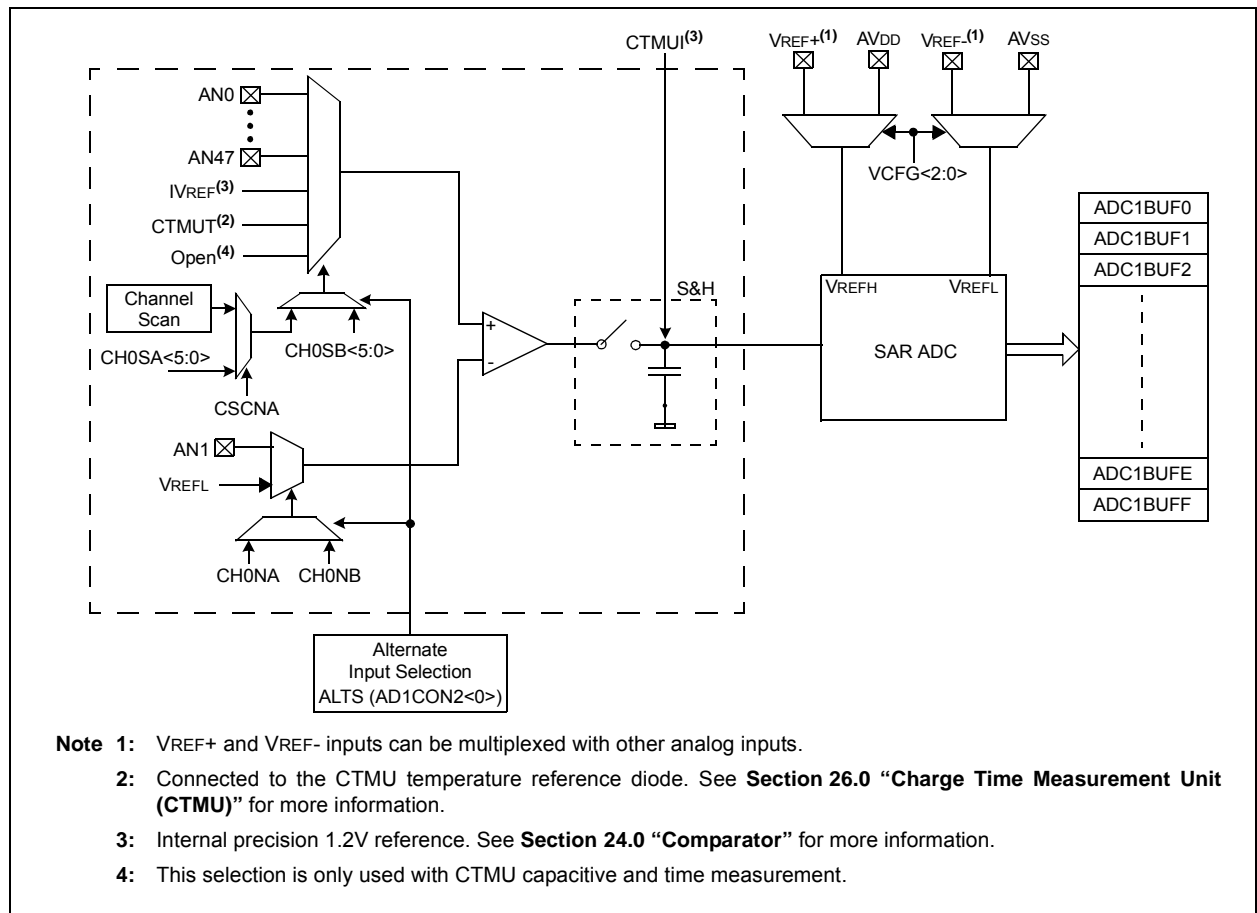## 22.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed
- Up to 48 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- Operation during CPU Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 22-1. The 10-bit ADC has up to 28 analog input pins, designated AN0-AN27. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

FIGURE 22-1: ADC1 MODULE BLOCK DIAGRAM

Note 1: VREF+ and VREF- inputs can be multiplexed with other analog inputs.

2: Connected to the CTMU temperature reference diode. See **Section 26.0 "Charge Time Measurement Unit (CTMU)"** for more information.

3: Internal precision 1.2V reference. See **Section 24.0 "Comparator"** for more information.

4: This selection is only used with CTMU capacitive and time measurement.

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	ON[1]	—	SIDL	—	—	FORM<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
	SSRC<2:0>			CLRASAM	—	ASAM	SAMP[2]	DONE[3]

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16   **Unimplemented:** Read as '0'

bit 15   **ON:** ADC Operating Mode bit[1]

     1 = ADC module is operating
     0 = ADC module is not operating

bit 14   **Unimplemented:** Read as '0'

bit 13   **SIDL:** Stop in Idle Mode bit

     1 = Discontinue module operation when device enters Idle mode
     0 = Continue module operation in Idle mode

bit 12-11   **Unimplemented:** Read as '0'

bit 10-8   **FORM<2:0>:** Data Output Format bits

     011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
     010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
     001 = Signed Integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sssd dddd dddd)
     000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
     111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000 0000)
     110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000 0000)
     101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
     100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5   **SSRC<2:0>:** Conversion Trigger Source Select bits

     111 = Internal counter ends sampling and starts conversion (auto convert)
     110 = Reserved
     101 = Reserved
     100 = Reserved
     011 = CTMU ends sampling and starts conversion
     010 = Timer 3 period match ends sampling and starts conversion
     001 = Active transition on INT0 pin ends sampling and starts conversion
     000 = Clearing SAMP bit ends sampling and starts conversion

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

     2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ 0, this bit is automatically cleared by hardware to end sampling and start conversion.

     3: This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

23.0 CONTROLLER AREA NETWORK (CAN)

> **Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 34. "Controller Area Network (CAN)"** (DS60001154) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Controller Area Network (CAN) module supports the following key features:

- Standards Compliance:
  - Full CAN 2.0B compliance
  - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
  - 16 message FIFOs
  - Each FIFO can have up to 16 messages for a total of 256 messages
  - FIFO can be a transmit message FIFO or a receive message FIFO
  - User-defined priority levels for message FIFOs used for transmission
  - 16 acceptance filters for message filtering
  - Four acceptance filter mask registers for message filtering
  - Automatic response to remote transmit request
  - DeviceNet™ addressing support
- Additional Features:
  - Loopback, Listen All Messages, and Listen Only modes for self-test, system diagnostics and bus monitoring
  - Low-power operating modes
  - CAN module is a bus master on the PIC32 system bus
  - Use of DMA is not required
  - Dedicated time-stamp timer
  - Dedicated DMA channels
  - Data-only Message Reception mode

Figure 23-1 illustrates the general structure of the CAN module.

FIGURE 23-1: PIC32 CAN MODULE BLOCK DIAGRAM
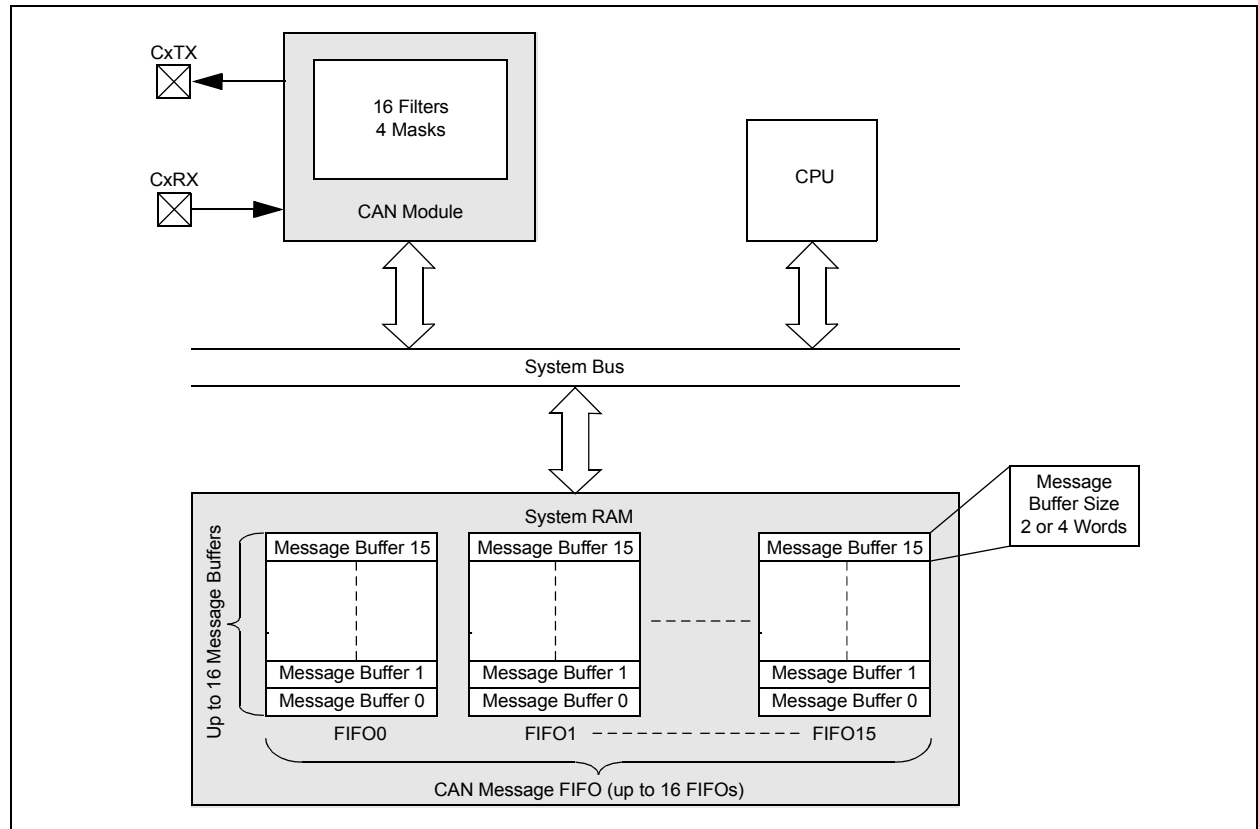
REGISTER 23-12: C1FLTCON2: CAN FILTER CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN11	MSEL11<1:0>		FSEL11<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN10	MSEL10<1:0>		FSEL10<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN9	MSEL9<1:0>		FSEL9<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN8	MSEL8<1:0>		FSEL8<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN11:** Filter 11 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL11<1:0>:** Filter 11 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL11<4:0>:** FIFO Selection bits

11111 = Reserved
•
•
•
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
•
•
•
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN10:** Filter 10 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL10<1:0>:** Filter 10 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

Note:	The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 24-2: CMSTAT: COMPARATOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	C3OUT	C2OUT	C1OUT

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-14   **Unimplemented:** Read as '0'

bit 13   **SIDL:** Stop in IDLE Control bit

1 = All Comparator modules are disabled in IDLE mode
0 = All Comparator modules continue to operate in the IDLE mode

bit 12-3   **Unimplemented:** Read as '0'

bit 2   **C3OUT:** Comparator Output bit

1 = Output of Comparator 3 is a '1'
0 = Output of Comparator 3 is a '0'

bit 1   **C2OUT:** Comparator Output bit

1 = Output of Comparator 2 is a '1'
0 = Output of Comparator 2 is a '0'

bit 0   **C1OUT:** Comparator Output bit

1 = Output of Comparator 1 is a '1'
0 = Output of Comparator 1 is a '0'

NOTES:

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28.0   SPECIAL FEATURES

Note:	This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog Timer and Power-up Timer"** (DS60001114), **Section 32. "Configuration"** (DS60001124) and **Section 33. "Programming and Diagnostics"** (DS60001129) in the *"PIC32 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

• Flexible device configuration
• Watchdog Timer (WDT)
• Joint Test Action Group (JTAG) interface
• In-Circuit Serial Programming™ (ICSP™)

28.1   Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

• DEVCFG0: Device Configuration Word 0
• DEVCFG1: Device Configuration Word 1
• DEVCFG2: Device Configuration Word 2
• DEVCFG3: Device Configuration Word 3
• CFGCON: Configuration Control Register

In addition, the DEVID register (Register 28-6) provides device and revision information.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 31-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40°C \leq T_A \leq +85°C$ for Industrial $-40°C \leq T_A \leq +105°C$ for V-temp				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO10	V_{OL}	**Output Low Voltage** I/O Pins: 4x Sink Driver Pins - All I/O output pins not defined as 8x Sink Driver pins	—	—	0.4	V	$I_{OL} \leq 9$ mA, V_{DD} = 3.3V
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - RB14, RC15, RD2, RD10, RD15, RF6, RF13, RG6	—	—	0.4	V	$I_{OL} \leq 15$ mA, V_{DD} = 3.3V
DO20	V_{OH}	**Output High Voltage** I/O Pins: 4x Source Driver Pins - All I/O output pins not defined as 8x Source Driver pins	2.4	—	—	V	$I_{OH} \geq -10$ mA, V_{DD} = 3.3V
		Output High Voltage I/O Pins: 8x Source Driver Pins - RB14, RC15, RD2, RD10, RD15, RF6, RF13, RG6	2.4	—	—	V	$I_{OH} \geq -15$ mA, V_{DD} = 3.3V
DO20A	V_{OH1}	**Output High Voltage** I/O Pins: 4x Source Driver Pins - All I/O output pins not defined as 8x Sink Driver pins	1.5[1]	—	—	V	$I_{OH} \geq -14$ mA, V_{DD} = 3.3V
			2.0[1]	—	—		$I_{OH} \geq -12$ mA, V_{DD} = 3.3V
			3.0[1]	—	—		$I_{OH} \geq -7$ mA, V_{DD} = 3.3V
		Output High Voltage I/O Pins: 8x Source Driver Pins - RB14, RC15, RD2, RD10, RD15, RF6, RF13, RG6	1.5[1]	—	—	V	$I_{OH} \geq -22$ mA, V_{DD} = 3.3V
			2.0[1]	—	—		$I_{OH} \geq -18$ mA, V_{DD} = 3.3V
			3.0[1]	—	—		$I_{OH} \geq -10$ mA, V_{DD} = 3.3V

Note 1: Parameters are characterized, but not tested.

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FIGURE 31-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS

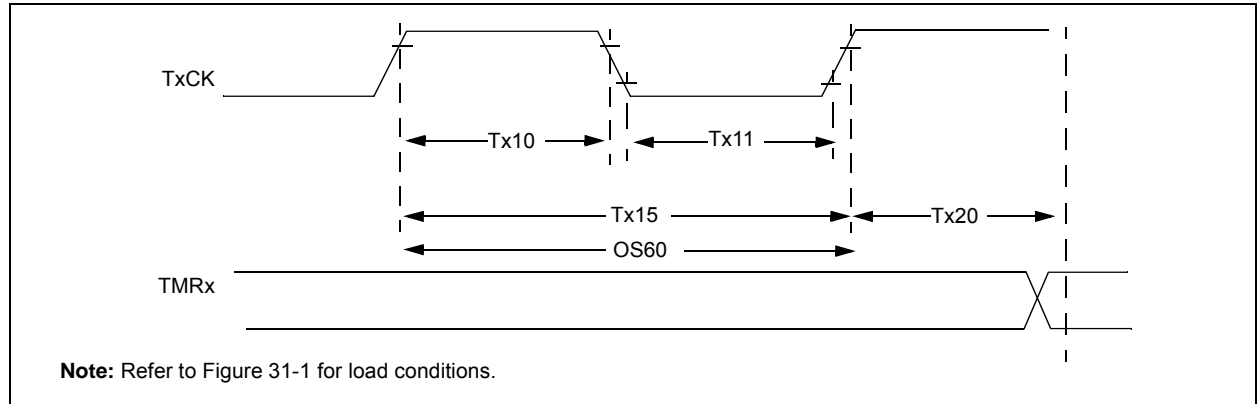Note: Refer to Figure 31-1 for load conditions.

TABLE 31-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS[1]				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics[2]		Min.	Typical	Max.	Units	Conditions
TA10	T$_{T x H}$	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 T$_{PB}$)/N] + 25 ns	—	—	ns	Must also meet parameter TA15
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	T$_{T x L}$	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 T$_{PB}$)/N] + 25 ns	—	—	ns	Must also meet parameter TA15
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	T$_{T x P}$	TxCK Input Period	Synchronous, with prescaler	[(Greater of 25 ns or 2 T$_{PB}$)/N] + 30 ns	—	—	ns	V$_{DD}$ > 2.7V
				[(Greater of 25 ns or 2 T$_{PB}$)/N] + 50 ns	—	—	ns	V$_{DD}$ < 2.7V
			Asynchronous, with prescaler	20	—	—	ns	V$_{DD}$ > 2.7V (Note 3)
				50	—	—	ns	V$_{DD}$ < 2.7V (Note 3)
OS60	F$_{T1}$	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting the TCS (T1CON<1>) bit)		32	—	100	kHz	—
TA20	T$_{CKEXTMRL}$	Delay from External TxCK Clock Edge to Timer Increment		—		1	T$_{PB}$	—

Note 1: Timer1 is a Type A timer.
   2: This parameter is characterized, but not tested in manufacturing.
   3: N = Prescale Value (1, 8, 64, 256).

FIGURE 31-8: **OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS**

OCx
(Output Compare
or PWM mode)

OC11 → |← → OC10 →| |←

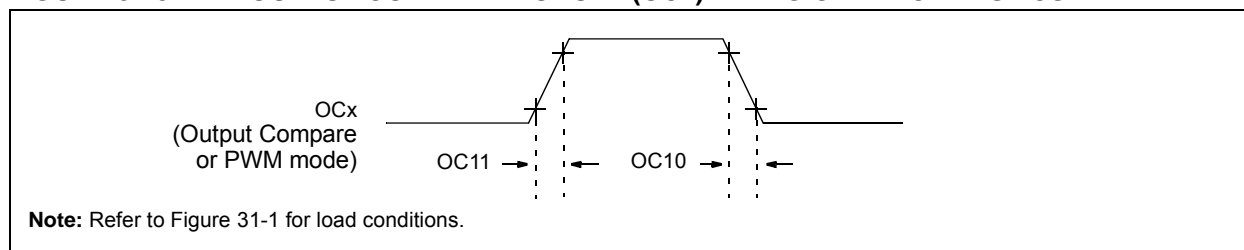**Note:** Refer to Figure 31-1 for load conditions.

TABLE 31-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics[1]	Min.	Typical[2]	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.
2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

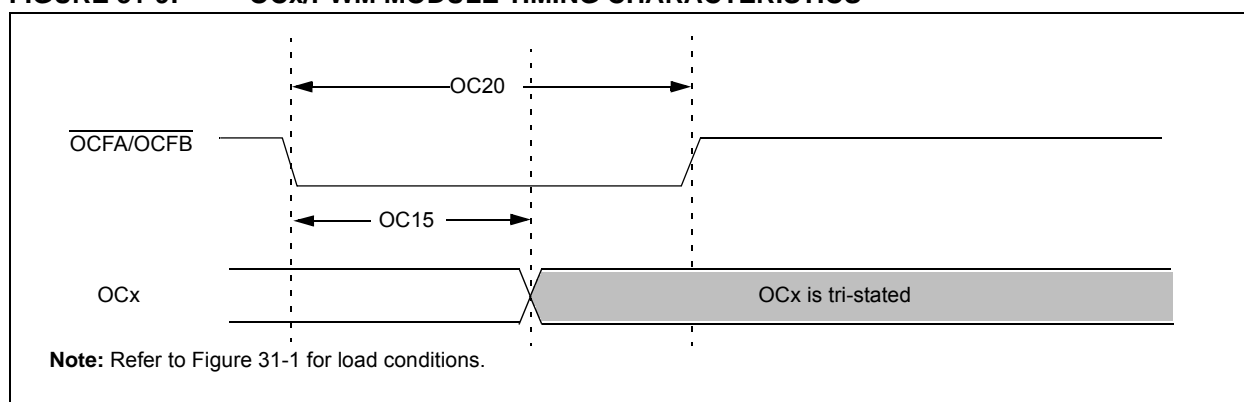**FIGURE 31-9:** **OCx/PWM MODULE TIMING CHARACTERISTICS**

OCFA/OCFB

OC20

OC15

OCx

OCx is tri-stated

Note: Refer to Figure 31-1 for load conditions.

TABLE 31-27: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param No.	Symbol	Characteristics[1]	Min	Typical[2]	Max	Units	Conditions
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.
2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 31-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

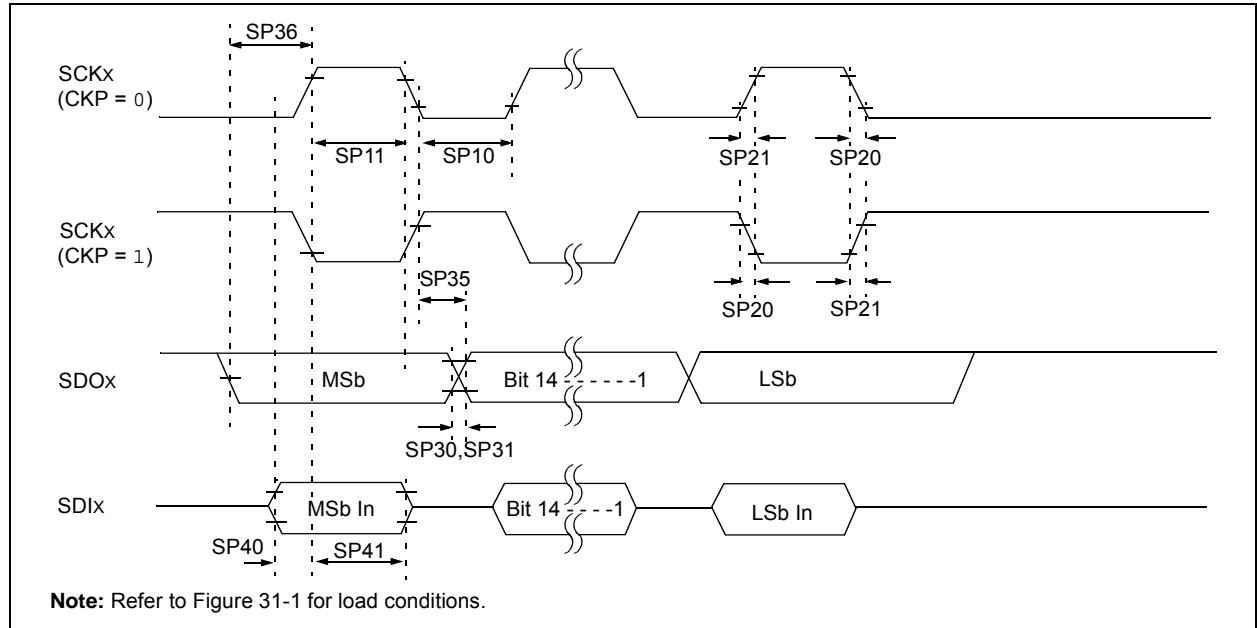**Note:** Refer to Figure 31-1 for load conditions.

TABLE 31-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time **(Note 3)**	Tsck/2	—	—	ns	—
SP11	TscH	SCKx Output High Time **(Note 3)**	Tsck/2	—	—	ns	—
SP20	TscF	SCKx Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP30	TDOF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2DOV, TscL2DOV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP36	TDOV2SC, TDOV2scL	SDOx Data Output Setup to First SCKx Edge	15	—	—	ns	—
SP40	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	15	—	—	ns	VDD > 2.7V
			20	—	—	ns	VDD < 2.7V
SP41	TscH2DIL, TscL2DIL	Hold Time of SDIx Data Input to SCKx Edge	15	—	—	ns	VDD > 2.7V
			20	—	—	ns	VDD < 2.7V

Note 1: These parameters are characterized, but not tested in manufacturing.

   2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

   3: The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.

   4: Assumes 50 pF load on all SPIx pins.

NOTES: