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Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f256ht-v-pt

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NOTES:

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

	Pin N	umber			
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	Pin Type	Buffer Type	Description
MCLR	7	13	I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVdd	19	30	Р	Р	Positive supply for analog modules. This pin must be connected at all times.
AVss	20	31	Р	Р	Ground reference for analog modules
Vdd	10, 26, 38, 57	2, 16, 37, 46, 62, 86	Р	_	Positive supply for peripheral logic and I/O pins
VCAP	56	85	Р	_	Capacitor for Internal Voltage Regulator
Vss	9, 25, 41	15, 36, 45, 65, 75	Р	_	Ground reference for logic and I/O pins
VREF+	16	29	Р	Analog	Analog Voltage Reference (High) Input
VREF-	15	28	Р	Analog	Analog Voltage Reference (Low) Input
Legend:	CMOS = CM	10S compati	ble inpu	it or output	Analog = Analog input I = Input O = Output

Legend: CMOS = CMOS compatible input or output Analog = Analog input I = Input ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

Control Registers 10.1

TABLE 10-1: USB REGISTER MAP

ess											Bit	s							
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5040		31:16	_	_	_	_	_	_	_	_	_		_	_	-	_	_	_	0000
5040	UIUIGIR	15:0	—	_	—	—	—	—	_	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
5050		31:16	_	—	—	—	_	_	—	_	—	-	_	—		_	_	—	0000
3030	UIUIUIL	15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
5060		31:16	—	—	—	—	—	—	—	—	-		_	-		—	—	-	0000
5000	010100IAI**	15:0	—				—	—		—	ID		LSTATE	_	SESVD	SESEND	—	VBUSVD	0000
5070		31:16	—				—	—		—	—	_	—	_		—	—	—	0000
0070	UIUIUUUU	15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0000		15:0	—	—	—	—	—	—	—	—	UACTPND ⁽⁴⁾	—	—	USLPGRD	USBBUSY		USUSPEND	USBPWR	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
5200	U1IR ⁽²⁾	15.0	_	_	_	_	_	_	_	_	STALLIE	ATTACHIE	RESUMEIE	IDI FIF	TRNIF	SOFIE	UERRIE	URSTIF	0000
		10.0									OINEEII		RECOMEN			00111	OLIVIA	DETACHIF	0000
		31:16	—				—	—		—	—	—	—	—	—	—	—	_	0000
5210	U1IE	15:0	_	_	_	_	_	_	_	_	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000
																		DETACHIE	0000
	(2)	31:16	—				—	—		—		—	—	—	_		—		0000
5220	U1EIR ⁽²⁾	15:0	_	_	_	_	_	_	_	_	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	0000
											5.02.	5117121	5.1.5.12.	5.02.	5111021	0110102	EOFEF		0000
		31:16	—				_			—	—	—	—	—	_	—	—	—	0000
5230	U1EIE	15:0	_	_	_	_	_	_	_	_	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE	0000
														-			EOFEE		0000
5240	U1STAT ⁽³⁾	31:16	_				_	_		_		—	—	—	_	—	_	_	0000
		15:0	—				_	—		—		ENDF	PT<3:0>		DIR	PPBI	_	_	0000
		31:16	_				_	_		_		_	—		_	_	_	—	0000
5250	U1CON	15:0	_	_	_	_	_	_	_	_	JSTATE	SE0	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN	0000
													TOKBUSY					SOFEN	0000
5260	U1ADDR	31:16	—				_	—		—				—	—				0000
		15:0	—							0000									
5270	U1BDTP1	31:16	_				_	_		_	_	—			—	—	—	_	0000
	l	15:0		—			—		—				BC	TPTRL<15:9>	•			—	0000
Leger	nd: x = unkr	10wn v	alue on R	leset; — =	: unimpler	nented, re	ead as '0'.	Reset va	lues are s	shown in h	nexadecimal.								

Legend:

With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information. Note 1:

2: This register does not have associated SET and INV registers.

This register does not have associated CLR, SET and INV registers. 3:

4: Reset value for this bit is undefined.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24	—	—	—	—				—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	-		-	—	
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15.0	—	—	—	—	-		-	—	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7.0				BDTPTR	H<23:16>				

REGISTER 10-18: U1BDTP2: USB BDT PAGE 2 REGISTER

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 **BDTPTRH<23:16>:** BDT Base Address bits This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
	—	—	—	—	—	—	—	—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:10	—	—	—	—	—	—	—	—			
15:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
15:8	—	—	—	—	—	—	—	—			
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7.0				BDTPTR	U<31:24>						

REGISTER 10-19: U1BDTP3: USB BDT PAGE 3 REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 BDTPTRU<31:24>: BDT Base Address bits

This 8-bit value provides address bits 31 through 24 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

REGISTER 18-2: I2CxSTAT: I²C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	-	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	-	—	—
45.0	R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
15:8	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
7.0	R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
7:0	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF

Legend:	HS = Set in hardware	HSC = Hardware set/clear	red
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit

bit 31-16 Unimplemented: Read as '0'

bit 15 ACKSTAT: Acknowledge Status bit

(when operating as I²C master, applicable to master transmit operation)

- 1 = Acknowledge was not received from slave
- 0 = Acknowledge was received from slave

Hardware set or clear at end of slave Acknowledge.

- bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
 - 1 = Master transmit is in progress (8 bits + ACK)
 - 0 = Master transmit is not in progress

Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

- bit 13-11 Unimplemented: Read as '0'
- bit 10 BCL: Master Bus Collision Detect bit

1 = A bus collision has been detected during a master operation

0 = No collision

Hardware set at detection of bus collision. This condition can only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module.

- bit 9 GCSTAT: General Call Status bit
 - 1 = General call address was received
 - 0 = General call address was not received

Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 ADD10: 10-bit Address Status bit

1 = 10-bit address was matched

0 = 10-bit address was not matched

Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 IWCOL: Write Collision Detect bit

1 = An attempt to write the I2CxTRN register failed because the I²C module is busy 0 = No collision

- Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).
- bit 6 **I2COV:** Receive Overflow Flag bit

1 = A byte was received while the I2CxRCV register is still holding the previous byte0 = No overflow

Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

- bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
 - 1 = Indicates that the last byte received was data
 - 0 = Indicates that the last byte received was device address

Hardware clear at device address match. Hardware set by reception of slave byte.

REGISTER 21-1: RTCCON: RTC CONTROL REGISTER (CONTINUED)

- bit 3 RTCWREN: RTC Value Registers Write Enable bit⁽⁴⁾
 - 1 = RTC Value registers can be written to by the user
 - 0 = RTC Value registers are locked out from being written to by the user
- bit 2 RTCSYNC: RTCC Value Registers Read Synchronization bit
 - 1 = RTC Value registers can change while reading, due to a rollover ripple that results in an invalid data read If the register is read twice and results in the same data, the data can be assumed to be valid
 - 0 = RTC Value registers can be read without concern about a rollover ripple
- bit 1 HALFSEC: Half-Second Status bit⁽⁵⁾
 - 1 = Second half period of a second
 - 0 = First half period of a second
- bit 0 RTCOE: RTCC Output Enable bit
 - 1 = RTCC clock output enabled clock presented onto an I/O
 - 0 = RTCC clock output disabled
- **Note 1:** The ON bit is only writable when RTCWREN = 1.
 - 2: When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 3: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
 - 4: The RTCWREN bit can be set only when the write sequence is enabled.
 - 5: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

'0' = Bit is cleared

x = Bit is unknown

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
31:24		HR10	<3:0>		HR01<3:0>				
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
23:10		MIN10	<3:0>		MIN01<3:0>				
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
15:8		SEC10	<3:0>		SEC01<3:0>				
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
7:0	—	—	—	—	_	_	_	—	
Legend:									
R = Read	lable bit		W = Writable	e bit	U = Unimple	emented bit, re	ead as '0'		

REGISTER 21-5: ALRMTIME: ALARM TIME VALUE REGISTER

bit 31-28 HR10<3:0>: Binary Coded Decimal value of hours bits, 10s place digits; contains a value from 0 to 2
bit 27-24 HR01<3:0>: Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9
bit 23-20 MIN10<3:0>: Binary Coded Decimal value of minutes bits, 10s place digits; contains a value from 0 to 5
bit 19-16 MIN01<3:0>: Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9
bit 15-12 SEC10<3:0>: Binary Coded Decimal value of seconds bits, 10s place digits; contains a value from 0 to 5
bit 11-8 SEC01<3:0>: Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9
bit 7-0 Unimplemented: Read as '0'

'1' = Bit is set

-n = Value at POR

REGISTE	EGISTER 22-2: AD1CON2: ADC CONTROL REGISTER 2									
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1			
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
	—	—	—	—	—	—	—			
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—	—	—			
15.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0			
10.0		VCFG<2:0>		OFFCAL	—	CSCNA	—			
7.0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7.0	BUFS	_		SMP	I<3:0>		BUFM			

F

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re-	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-13 VCFG<2:0>: Voltage Reference Configuration bits

	VREFH	VREFL
000	AVDD	AVss
001	External VREF+ pin	AVss
010	AVDD	External VREF- pin
011	External VREF+ pin	External VREF- pin
1xx	AVDD	AVss

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

- 1 = Enable Offset Calibration mode
 - Positive and negative inputs of the sample and hold amplifier are connected to VREFL
- 0 = Disable Offset Calibration mode

The inputs to the sample and hold amplifier are controlled by AD1CHS or AD1CSSL

bit 11 Unimplemented: Read as '0'

- bit 10 CSCNA: Input Scan Select bit
 - 1 = Scan inputs
 - 0 = Do not scan inputs

bit 9-8 Unimplemented: Read as '0'

- bit 7 BUFS: Buffer Fill Status bit
 - Only valid when BUFM = 1.
 - 1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7
 - 0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 Unimplemented: Read as '0'

bit 5-2 SMPI<3:0>: Sample/Convert Sequences Per Interrupt Selection bits

- 1111 = Interrupts at the completion of conversion for each 16^{th} sample/convert sequence 1110 = Interrupts at the completion of conversion for each 15^{th} sample/convert sequence
- 0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence 0000 = Interrupts at the completion of conversion for each sample/convert sequence
- bit 1 BUFM: ADC Result Buffer Mode Select bit
 - 1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8
 - 0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0
- bit 0 ALTS: Alternate Input Sample Mode Select bit
 - 1 = Uses Sample A input multiplexer settings for first sample, then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples
 - 0 = Always use Sample A input multiplexer settings

Bit 24/16/8/0 U-0

U-0

U-0

R/W-0 ALTS

23.0 CONTROLLER AREA NETWORK (CAN)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 34. "Controller Area Network (CAN)" (DS60001154) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The Controller Area Network (CAN) module supports the following key features:

- · Standards Compliance:
 - Full CAN 2.0B compliance
 - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
 - 16 message FIFOs
 - Each FIFO can have up to 16 messages for a total of 256 messages

- FIFO can be a transmit message FIFO or a receive message FIFO
- User-defined priority levels for message FIFOs used for transmission
- 16 acceptance filters for message filtering
- Four acceptance filter mask registers for message filtering
- Automatic response to remote transmit request
- DeviceNet[™] addressing support
- Additional Features:
 - Loopback, Listen All Messages, and Listen Only modes for self-test, system diagnostics and bus monitoring
 - Low-power operating modes
 - CAN module is a bus master on the PIC32 system bus
 - Use of DMA is not required
 - Dedicated time-stamp timer
 - Dedicated DMA channels
- Data-only Message Reception mode

Figure 23-1 illustrates the general structure of the CAN module.

FIGURE 23-1: PIC32 CAN MODULE BLOCK DIAGRAM



REGISTER 23-2: C1CFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

- bit 10-8 **PRSEG<2:0>:** Propagation Time Segment bits⁽⁴⁾ 111 = Length is $8 \times TQ$ $000 = \text{Length is } 1 \times TQ$ SJW<1:0>: Synchronization Jump Width bits⁽³⁾ bit 7-6 11 = Length is $4 \times TQ$ $10 = \text{Length is } 3 \times TQ$ 01 = Length is 2 x TQ $00 = \text{Length is } 1 \times TQ$ bit 5-0 BRP<5:0>: Baud Rate Prescaler bits 111111 = Tq = (2 x 64)/SYSCLK 111110 = TQ = (2 x 63)/SYSCLK • 000001 = TQ = (2 x 2)/SYSCLK $000000 = TQ = (2 \times 1)/SYSCLK$ Note 1: SEG2PH \leq SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically. 2: 3 Time bit sampling is not allowed for BRP < 2.
 - **3:** SJW \leq SEG2PH.
 - **4:** The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = 100).

31.1 DC Characteristics

TABLE 31-1: OPERATING MIPS VS. VOLTAGE

	Voo Bango	Tomp Bango	Max. Frequency
Characteristic	(in Volts) ⁽¹⁾	(in °C)	PIC32MX1XX/2XX/5XX 64/100-pin Family
DC5	VBOR-3.6V	-40°C to +105°C	40 MHz

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for BOR values.

TABLE 31-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
V-temp Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+105	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – S IOH)	PD		PINT + PI/C)	W
I/O Pin Power Dissipation: I/O = S (({VDD – VOH} x IOH) + S (VOL x IOL))					
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJ	A	W

TABLE 31-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 64-pin QFN	θJA	28	_	°C/W	1
Package Thermal Resistance, 64-pin TQFP, 10 mm x 10 mm	θJA	55	—	°C/W	1
Package Thermal Resistance, 100-pin TQFP, 12 mm x 12 mm	θJA	52	—	°C/W	1
Package Thermal Resistance, 100-pin TQFP, 14 mm x 14 mm	θJA	50		°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

DC CHA	RACTERIS	TICS	Standar Operatir	$\begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	m. Typical ⁽²⁾ Max. Units Conditions									
Power-D	Down Curre	ent (IPD) (No	otes 1, 5)							
DC40k	33	78	μA	-40°C						
DC40I	49	78	μA	+25°C	Raso Rower Down Current					
DC40n	281	450	μA	+85°C	Dase Fower-Down Current					
DC40m	559	895	μA	+105°C						
Module	Differential	Current								
DC41e	10	25	μA	3.6V	Watchdog Timer Current: AIWDT (Note 3)					
DC42e	29	50	μA	3.6V RTCC + Timer1 w/32 kHz Crystal: △IRTCC (Note 3)						
DC43d	1000	1300	μA	3.6V ADC: ΔΙΑDC (Notes 3,4)						

TABLE 31-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

Note 1: The test conditions for IPD current measurements are as follows:

Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)

OSC2/CLKO is configured as an I/O input pin

- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD
- RTCC and JTAG are disabled
- 2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- **3:** The ∆ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5: IPD electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

	DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)						
DOOIL			Operatin	ig tempe	erature	$\label{eq:constraint} \begin{array}{l} -40^\circ C \leq TA \leq +85^\circ C \text{ for Industrial} \\ -40^\circ C \leq TA \leq +105^\circ C \text{ for V-temp} \end{array}$			
Param.	Symbol	Characteristic	Min.	Min. Typ. Max.			Conditions		
DO10	Vol	Output Low Voltage I/O Pins: 4x Sink Driver Pins - All I/O output pins not defined as 8x Sink Driver pins	_	_	0.4	v	IOL \leq 9 mA, VDD = 3.3V		
DO10	VOL	Output Low Voltage I/O Pins: 8x Sink Driver Pins - RB14, RC15, RD2, RD10, RD15, RF6, RF13, RG6	_	_	0.4	v	$\text{IOL} \leq 15 \text{ mA}, \text{ VDD} = 3.3 \text{V}$		
DO20		Output High Voltage I/O Pins: 4x Source Driver Pins - All I/O output pins not defined as 8x Source Driver pins	2.4	_	_	v	Ioh ≥ -10 mA, Vdd = 3.3V		
	VOIT	Output High Voltage I/O Pins: 8x Source Driver Pins - RB14, RC15, RD2, RD10, RD15, RF6, RF13, RG6	2.4	_	_	v	Іон ≥ -15 mA, Vdd = 3.3V		
		Output High Voltage	1.5 ⁽¹⁾	_			IOH \ge -14 mA, VDD = 3.3V		
		4x Source Driver Pins - All I/O	2.0 ⁽¹⁾	_	—	V	IOH \ge -12 mA, VDD = 3.3V		
D0204	Vout	Sink Driver pins	3.0 ⁽¹⁾	_	—		Ioh \geq -7 mA, Vdd = 3.3V		
DOZUA	VOHI	Output High Voltage	1.5 ⁽¹⁾	_	_		$\text{IOH} \geq \text{-22 mA, VDD} = 3.3\text{V}$		
		8x Source Driver Pins - RB14,	2.0 ⁽¹⁾	_	_	V	$\text{IOH} \geq \text{-18 mA, VDD} = 3.3\text{V}$		
		RC15, RD2, RD10, RD15, RF6, RF13, RG6	3.0 ⁽¹⁾	_	_		IOH \geq -10 mA, VDD = 3.3V		

TABLE 31-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

Note 1: Parameters are characterized, but not tested.

31.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX/5XX 64/100-pin AC characteristics and timing parameters.

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



TABLE 31-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics	Min. Typical ⁽¹⁾ Max. Units Conditions							
DO50	Cosco	OSC2 pin	_	_	15	pF	In XT and HS modes when an external crystal is used to drive OSC1			
DO50a	Csosc	SOSCI/SOSCO pins	_	33		pF	Epson P/N: MC-306 32.7680K- A0:ROHS			
DO56	Сю	All I/O pins and OSC2	_	— — 50 pF EC mode						
DO58	Св	SCLx, SDAx	— — 400 pF In I ² C mode							

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 31-2: EXTERNAL CLOCK TIMING



AC CHARA	CTERISTIC	S ⁽²⁾	Standard (unless of Operating	Operating therwise st temperature	Conditions (see Note 3): 2.5V to 3.6V ated) e $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp
ADC Speed	TAD Min.	Sampling Time Min.	Rs Max.	Vdd	ADC Channels Configuration
1 Msps to 400 ksps ⁽¹⁾	65 ns	132 ns	500Ω	3.0V to 3.6V	ANX CHX ADC
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	ANX ADC ANX OF VREF-

TABLE 31-35: 10-BIT CONVERSION RATE PARAMETERS

Note 1: External VREF- and VREF+ pins must be used for correct operation.

2: These parameters are characterized, but not tested in manufacturing.

3: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 31-39: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\label{eq:constraint} \begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min. Typ. Max. Units Conditions					
PM11	Twr	PMWR Pulse Width		1 Трв	_	_	_	
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 Трв	_	_	_	
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 Трв	—	_	_	

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 31-40: OTG ELECTRICAL SPECIFICATIONS

АС СНА	RACTERI	STICS	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$						
Param. No.	Symbol	Characteristics ⁽¹⁾	Min. Typ. Max. Units Conditions						
USB313	VUSB3V3	USB Voltage	3.0	_	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation		
USB315	VILUSB	Input Low Voltage for USB Buffer	_	—	0.8	V	—		
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	_	V	—		
USB318	VDIFS	Differential Input Sensitivity	—	_	0.2	V	The difference between D+ and D- must exceed this value while VCM is met		
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—		
USB320	Zout	Driver Output Impedance	28.0	—	44.0	Ω	—		
USB321	Vol	Voltage Output Low	0.0	—	0.3	V	1.425 kΩ load connected to VUSB3V3		
USB322	Vон	Voltage Output High	2.8	_	3.6	V	1.425 k Ω load connected to ground		

Note	1:	These parameters are characterized, but not tested in manufacturing.
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TABLE 31-41: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 3):2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +105^\circ C \mbox{ for V-temp} \end{array}$					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions	
CTMU CUR	RENT SOUR	CE						
CTMUI1	IOUT1	Base Range ⁽¹⁾	_	0.55		μA	CTMUCON<9:8> = 01	
CTMUI2	IOUT2	10x Range ⁽¹⁾	—	5.5	_	μA	CTMUCON<9:8> = 10	
CTMUI3	Ιουτ3	100x Range ⁽¹⁾	_	55		μA	CTMUCON<9:8> = 11	
CTMUI4	IOUT4	1000x Range ⁽¹⁾	—	550	_	μA	CTMUCON<9:8> = 00	
CTMUFV1	VF	Temperature Diode Forward Voltage ^(1,2)	_	0.598	_	V	TA = +25°C, CTMUCON<9:8> = 01	
			_	0.658	_	V	TA = +25°C, CTMUCON<9:8> = 10	
			_	0.721	_	V	TA = +25°C, CTMUCON<9:8> = 11	
CTMUFV2	VFVR	Temperature Diode Rate of	—	-1.92	_	mV/ºC	CTMUCON<9:8> = 01	
		Change ^(1,2)	—	-1.74	—	mV/ºC	CTMUCON<9:8> = 10	
			_	-1.56		mV/ºC	CTMUCON<9:8> = 11	

Note 1: Nominal value at center point of current trim range (CTMUCON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksps
- All PMD bits are cleared (PMDx = 0)
- Executing a while(1) statement
- Device operating from the FRC with no PLL
- **3:** The CTMU module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.



100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Chamfers at corners are optional; size may vary.
- 3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 0.40 mm Contact Length and 5.40x5.40mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimensior	MIN	NOM	MAX		
Contact Pitch	E	0.50 BSC			
Optional Center Pad Width	W2	5.50			
Optional Center Pad Length	T2			5.50	
Contact Pad Spacing	C1		8.90		
Contact Pad Spacing	C2		8.90		
Contact Pad Width (X64)	X1			0.30	
Contact Pad Length (X64)	Y1			0.85	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2154A