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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	81
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f256l-v-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

6.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 5. "Flash Program Memory" (DS60001121) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32). PIC32MX1XX/2XX/5XX 64/100-pin devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming[™] (ICSP[™])

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual"*.

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the *"PIC32 Flash Programming Specification"* (DS60001145), which can be downloaded from the Microchip web site.

Note: On PIC32MX1XX/2XX/5XX 64/100-pin devices, the Flash page size is 1 KB and the row size is 128 bytes (256 IW and 32 IW, respectively).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	-	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:10	—	—	—	—	—	-	—	—	
45.0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	
15:8	ON ⁽¹⁾	—	—	SUSPEND	DMABUSY ⁽¹⁾		—	—	
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	_	_	_	_		_	_	_	

REGISTER 9-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Legend:

0			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ON: DMA On bit⁽¹⁾
 - 1 = DMA module is enabled
 - 0 = DMA module is disabled
- bit 14-13 **Unimplemented:** Read as '0'
- bit 12 **SUSPEND:** DMA Suspend bit
 - 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
 - 0 = DMA operates normally

bit 11 DMABUSY: DMA Module Busy bit⁽¹⁾

- 1 = DMA module is active
- 0 = DMA module is disabled and not actively transferring data
- bit 10-0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
51.24	—	—	—	—	_	_		—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	—	—	_	_	-	—		
15.9	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
15.0	—	—	_	—				_		
7:0	R-0	U-0	R-0	U-0	R-0	R-0	U-0	R-0		
	ID	—	LSTATE	—	SESVD	SESEND		VBUSVD		

REGISTER 10-3: U1OTGSTAT: USB OTG STATUS REGISTER

Legend:

3			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7 ID: ID Pin State Indicator bit
 - 1 = No cable is attached or a Type-B cable has been plugged into the USB receptacle
 - 0 = A Type-A cable has been plugged into the USB receptacle
- bit 6 Unimplemented: Read as '0'
- bit 5 LSTATE: Line State Stable Indicator bit
 - 1 = USB line state (U1CON<SE0> and U1CON<JSTATE>) has been stable for the previous 1 ms
 - 0 = USB line state (U1CON<SE0> and U1CON<JSTATE>) has not been stable for the previous 1 ms

bit 4 Unimplemented: Read as '0'

- bit 3 SESVD: Session Valid Indicator bit
 - 1 = VBUS voltage is above Session Valid on the A or B device
 - 0 = VBUS voltage is below Session Valid on the A or B device
- bit 2 **SESEND:** B-Device Session End Indicator bit
 - 1 = VBUS voltage is below Session Valid on the B device
 - 0 = VBUS voltage is above Session Valid on the B device

bit 1 Unimplemented: Read as '0'

- bit 0 VBUSVD: A-Device VBUS Valid Indicator bit
 - 1 = VBUS voltage is above Session Valid on the A device
 - 0 = VBUS voltage is below Session Valid on the A device

REGISTER 10-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—		—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—		—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	_	—		_	—	_	_	—
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	STALLIE	STALLIE ATTACHIE RI			TRNIE	SOFIE		URSTIE ⁽²⁾
			RESUMEIE	IDLEIE			UERRIE'	DETACHIE ⁽³⁾
1	1	1				1		

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7	STALLIE: STALL Handshake Interrupt Enable bit
	1 = STALL interrupt enabled
	0 = STALL interrupt disabled

bit 6 **ATTACHIE:** ATTACH Interrupt Enable bit 1 = ATTACH interrupt enabled

0 = ATTACH interrupt disabled

bit 5 **RESUMEIE:** RESUME Interrupt Enable bit

- 1 = RESUME interrupt enabled
- 0 = RESUME interrupt disabled
- bit 4 IDLEIE: Idle Detect Interrupt Enable bit
 - 1 = Idle interrupt enabled
 - 0 = Idle interrupt disabled
- bit 3 TRNIE: Token Processing Complete Interrupt Enable bit
 - 1 = TRNIF interrupt enabled
 - 0 = TRNIF interrupt disabled
- bit 2 SOFIE: SOF Token Interrupt Enable bit
 - 1 = SOFIF interrupt enabled
 - 0 = SOFIF interrupt disabled
- bit 1 UERRIE: USB Error Interrupt Enable bit⁽¹⁾
 - 1 = USB Error interrupt enabled
 - 0 = USB Error interrupt disabled
- bit 0 **URSTIE:** USB Reset Interrupt Enable bit⁽²⁾
 - 1 = URSTIF interrupt enabled
 - 0 = URSTIF interrupt disabled
 - DETACHIE: USB Detach Interrupt Enable bit⁽³⁾
 - 1 = DATTCHIF interrupt enabled
 - 0 = DATTCHIF interrupt disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.

- 2: Device mode.
- 3: Host mode.

Peripheral Pin	[pin name]R SFR	[<i>pin name</i>]R bits	[<i>pin name</i>]R Value to RPn Pin Selection
INT1	INT1R	INT1R<3:0>	0000 = RPD1 0001 = RPG9
ТЗСК	T3CKR	T3CKR<3:0>	0010 = RPB14 0011 = RPD0
IC1	IC1R	IC1R<3:0>	0100 = RPD8 0101 = RPB6
U3CTS	U3CTSR	U3CTSR<3:0>	0110 = RPD5 0111 = RPB2
U4RX	U4RXR	U4RXR<3:0>	1000 = RPF3 ⁽⁴⁾ 1001 = RPF13 ⁽³⁾
U5RX	U5RXR	U5RXR<3:0>	1010 = Reserved 1011 = RPF2 ⁽¹⁾
SS2	SS2R	SS2R<3:0>	1100 = RPC2 ⁽³⁾ 1101 = RPE8 ⁽³⁾
OCFA	OCFAR	OCFAR<3:0>	1110 = Reserved 1111 = Reserved

TABLE 11-1:INPUT PIN SELECTION (CONTINUED)

Note 1: This selection is not available on 64-pin USB devices.

- 2: This selection is only available on 100-pin General Purpose devices.
- 3: This selection is not available on 64-pin devices.
- 4: This selection is not available when USBID functionality is used on USB devices.
- 5: This selection is not available on devices without a CAN module.
- 6: This selection is not available on USB devices.
- 7: This selection is not available when VBUSON functionality is used on USB devices.

TABLE 11-12: PORTF REGISTER MAP FOR PIC32MX230F128L, PIC32MX530F128L, PIC32MX250F256L, PIC32MX550F256L, PIC32MX270F512L, AND PIC32MX570F512L DEVICES ONLY

ess				Bits															
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6500	ANSELE	31:16	—	—	—	—	—	_	_	—	—	—	—	—	—	—	_	—	0000
0000	, aloceli	15:0	—	—	ANSELE13	ANSELE12	—	_	_	ANSELE8	—	—	—	—	—	ANSELE2	ANSELE1	ANSELE0	3107
6510	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0010	11401	15:0	_	—	TRISF13	TRISF12	—	—	—	TRISF8	—	—	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	313F
6520	PORTE	31:16	_	—	—	—	_	_	_	—	_	—	—		—	—	_	—	0000
0020	1 Oltin	15:0	—	—	RF13	RF12	—	_	_	RF8	—	—	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6530	LATE	31:16	—	—	—	—	—	_	_	—	—	—	—	—	—	—	—	—	0000
0000	2,00	15:0	—	—	LATF13	LATF12	—	_	_	LATF8	—	—	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6540	ODCE	31:16	_	—	—	—		_		—	_	—	—		—	—			0000
0040	0001	15:0	_	—	ODCF13	ODCF12		_		ODCF8	_	—	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000
6550	CNPUE	31:16	_	—	—	—		_		—	_	—	—		—	—			0000
0000		15:0	_	—	CNPUF13	CNPUF12		_		CNPUF8	_	—	CNPUF5	CNPUF4	CNPDF3	CNPUF2	CNPUF1	CNPUF0	0000
6560	CNPDE	31:16	_	—	—	—		_		—	_	—	—		—	—			0000
0000		15:0	_	—	CNPDF13	CNPDF12		_		CNPDF8	_	—	CNPDF5	CNPFF4	CNPDF3	CNPDF2	CNPDF1	CNPDF0	0000
6570	CNCONE	31:16	_	—	—	—		_		—	_	—	—		—	—			0000
0070	onoon	15:0	ON	—	SIDL	—		_		—	_	—	—		—	—			0000
6580	CNENE	31:16	—	—	—	—	—	—	-	—	—	—	—	_	—	—	—	_	0000
0000	CINEINI	15:0	—	—	CNIEF13	CNIEF12	_	_	_	CNIEF8	_	—	CNIEF5	CNIEF4	CNIEF3	CNIEF2	CNIEF1	CNIEF0	0000
		31:16	_	_	-	_	_	_	_	_	_	_	_	_	—	-	_	_	0000
6590	CNSTATF	15:0	_	_	CN STATF13	CN STATF12	_	_	_	CN STATF8	_	_	CN STATF5	CN STATF4	CN STATF3	CN STATF2	CN STATF1	CN STATF0	0000

Legend: x = Unknown value on Reset; - = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—	_	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:10	—	—	_	—	—	—	—	—		
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0		
15:8	ON	_	SIDL	_	_		_	—		
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	_	_		—	_	_	_	—		

REGISTER 11-3: CNCONX: CHANGE NOTICE CONTROL FOR PORTX REGISTER (X = A – G)

Legend:

5			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Change Notice (CN) Control ON bit
 - 1 = CN is enabled
 - 0 = CN is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Control bit
 - 1 = CPU Idle Mode halts CN operation
 - 0 = CPU Idle does not affect CN operation
- bit 12-0 Unimplemented: Read as '0'

REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

- bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit
 - $\frac{\text{When TCS} = 1:}{1 = \text{External clock input is synchronized}}$ 0 = External clock input is not synchronized $\frac{\text{When TCS} = 0:}{\text{This bit is ignored.}}$
- bit 1 **TCS:** Timer Clock Source Select bit 1 = External clock from TxCKI pin 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER (CONTINUED)

bit 3 SPITBE: SPI Transmit Buffer Empty Status bit 1 = Transmit buffer, SPIxTXB is empty 0 = Transmit buffer, SPIxTXB is not empty Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR. Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB. bit 2 Unimplemented: Read as '0' bit 1 SPITBF: SPI Transmit Buffer Full Status bit 1 = Transmit not yet started, SPITXB is full 0 = Transmit buffer is not full Standard Buffer Mode: Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB. Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR. Enhanced Buffer Mode: Set when CWPTR + 1 = SRPTR; cleared otherwise bit 0 SPIRBF: SPI Receive Buffer Full Status bit 1 = Receive buffer, SPIxRXB is full

0 = Receive buffer, SPIxRXB is not full

Standard Buffer Mode:

Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.

Enhanced Buffer Mode:

Set when SWPTR + 1 = CRPTR; cleared otherwise

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0 U-0		U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	_	_	_	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	_	_	—	_	_
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	IREN	RTSMD	_	UEN	<1:0>
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL	<1:0>	STSEL

REGISTER 19-1: UxMODE: UARTx MODE REGISTER

Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** UARTx Enable bit⁽¹⁾
 - 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits
 - UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal

bit 14 Unimplemented: Read as '0'

bit 13 SIDL: Stop in Idle Mode bit

- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation in Idle mode
- bit 12 IREN: IrDA Encoder and Decoder Enable bit
 - 1 = IrDA is enabled
 - 0 = IrDA is disabled
- bit 11 **RTSMD:** Mode Selection for UxRTS Pin bit
 - 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
 - $0 = \overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 Unimplemented: Read as '0'

bit 9-8 UEN<1:0>: UARTx Enable bits

- 11 = UxTX, UxRX and UxBCLK pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
- 00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/UxBCLK pins are controlled by corresponding bits in the PORTx register
- bit 7 WAKE: Enable Wake-up on Start bit Detect During Sleep Mode bit
 - 1 = Wake-up enabled
 - 0 = Wake-up disabled
- bit 6 LPBACK: UARTx Loopback Mode Select bit
 - 1 = Loopback mode is enabled
 - 0 = Loopback mode is disabled
- **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

19.2 Timing Diagrams

Figure 19-2 and Figure 19-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 19-2: UART RECEPTION



FIGURE 19-3: TRANSMISSION (8-BIT OR 9-BIT DATA)



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
45.0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	BUSY	IRQM	<1:0>	INCM	<1:0>	MODE16	MODE	=<1:0>
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	WAITB	<1:0>(1)		WAITM	<3:0>(1)		WAITE	<1:0>(1)

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER

Legend:

•			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **BUSY:** Busy bit (Master mode only)
 - 1 = Port is busy
 - 0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits

- 11 = Reserved, do not use
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Slave mode only)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No Interrupt generated
- bit 12-11 INCM<1:0>: Increment Mode bits
 - 11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)
 - 10 = Decrement ADDR<15:0> by 1 every read/write cycle⁽²⁾
 - 01 = Increment ADDR<15:0> by 1 every read/write cycle⁽²⁾
 - 00 = No increment or decrement of address
- bit 10 **MODE16:** 8/16-bit Mode bit
 - 1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer
 - 0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer
- bit 9-8 MODE<1:0>: Parallel Port Mode Select bits
 - 11 = Master mode 1 (PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, PMD<7:0> and PMD<8:15>⁽³⁾)
 - 10 = Master mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, PMD<7:0> and PMD<8:15>⁽³⁾)
 - 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>)
 - 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS and PMD<7:0>)

bit 7-6 WAITB<1:0>: Data Setup to Read/Write Strobe Wait States bits⁽¹⁾

- 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
- 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
- 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
- 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)
- **Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.
 - 2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.
 - 3: These pins are active when MODE16 = 1 (16-bit mode).

REGISTER 21-1: RTCCON: RTC CONTROL REGISTER (CONTINUED)

- bit 3 RTCWREN: RTC Value Registers Write Enable bit⁽⁴⁾
 - 1 = RTC Value registers can be written to by the user
 - 0 = RTC Value registers are locked out from being written to by the user
- bit 2 RTCSYNC: RTCC Value Registers Read Synchronization bit
 - 1 = RTC Value registers can change while reading, due to a rollover ripple that results in an invalid data read If the register is read twice and results in the same data, the data can be assumed to be valid
 - 0 = RTC Value registers can be read without concern about a rollover ripple
- bit 1 HALFSEC: Half-Second Status bit⁽⁵⁾
 - 1 = Second half period of a second
 - 0 = First half period of a second
- bit 0 RTCOE: RTCC Output Enable bit
 - 1 = RTCC clock output enabled clock presented onto an I/O
 - 0 = RTCC clock output disabled
- **Note 1:** The ON bit is only writable when RTCWREN = 1.
 - 2: When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 3: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
 - 4: The RTCWREN bit can be set only when the write sequence is enabled.
 - 5: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

			• • • • • • •							
Bit Range	Bit Bit E 31/23/15/7 30/22/14/6 29/2		Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
31:24		HR10	<3:0>			HR01	<3:0>			
00.40	R/W-x R/W-x R/W-x R/W-x				R/W-x	R/W-x	R/W-x	R/W-x		
23:16		MIN10	<3:0>			MIN01	<3:0>			
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
15:8		SEC10)<3:0>			SEC0 ²	1<3:0>			
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
7:0	—	_	—	—	—	_	—	—		
Legend:										
R = Read	able bit		W = Writable	e bit	U = Unimple	emented bit, re	ead as '0'			

REGISTER 21-3: RTCTIME: RTC TIME VALUE REGISTER

 -n = Value at POR
 '1' = Bit is set
 '0' = Bit is cleared
 x = Bit is unknown

 bit 31-28
 HR10<3:0>: Binary-Coded Decimal Value of Hours bits, 10s place digits; contains a value from 0 to 2

bit 31-28 HR(10<3:0>: Binary-Coded Decimal Value of Hours bits, 10s place digits, contains a value from 0 to 2
bit 27-24 HR01<3:0>: Binary-Coded Decimal Value of Hours bits, 1s place digit; contains a value from 0 to 9
bit 23-20 MIN10<3:0>: Binary-Coded Decimal Value of Minutes bits, 10s place digits; contains a value from 0 to 5
bit 19-16 MIN01<3:0>: Binary-Coded Decimal Value of Minutes bits, 1s place digit; contains a value from 0 to 9
bit 15-12 SEC10<3:0>: Binary-Coded Decimal Value of Seconds bits, 10s place digits; contains a value from 0 to 5
bit 11-8 SEC01<3:0>: Binary-Coded Decimal Value of Seconds bits, 1s place digit; contains a value from 0 to 9
bit 17-0 Unimplemented: Read as '0'

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

'0' = Bit is cleared

x = Bit is unknown

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
31:24		HR10	<3:0>			HR01	<3:0>		
00.40	R/W-x R/W-x R/W-x			R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
23:10		MIN10	<3:0>			Bit 26/18/10/2 R/W-x HR01 R/W-x MIN01 R/W-x SEC01 U-0 — emented bit, real	<3:0>		
45.0	R/W-x R/W-x		R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
15:8		SEC10	<3:0>			SEC0 ²	1<3:0>		
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
7:0	—	_	—	—	_	_	_	—	
Legend:									
R = Read	lable bit		W = Writable	e bit	U = Unimple	emented bit, re	ead as '0'		

REGISTER 21-5: ALRMTIME: ALARM TIME VALUE REGISTER

bit 31-28 HR10<3:0>: Binary Coded Decimal value of hours bits, 10s place digits; contains a value from 0 to 2
bit 27-24 HR01<3:0>: Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9
bit 23-20 MIN10<3:0>: Binary Coded Decimal value of minutes bits, 10s place digits; contains a value from 0 to 5
bit 19-16 MIN01<3:0>: Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9
bit 15-12 SEC10<3:0>: Binary Coded Decimal value of seconds bits, 10s place digits; contains a value from 0 to 5
bit 11-8 SEC01<3:0>: Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9
bit 7-0 Unimplemented: Read as '0'

'1' = Bit is set

-n = Value at POR

23.1 **Control Registers**

TABLE 23-1: CAN1 REGISTER SUMMARY

ess										Bit	s								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
D 000	01001	31:16		_	_	_	ABAT		REQOP<2:0	>	(OPMOD<2:0	>	CANCAP	_	_	_	_	0480
B000	CICON	15:0	ON	—	SIDLE	—	CANBUSY	_	—	_	_	—	_		D	NCNT<4:0>			0000
P010	CICEC	31:16	_	_	_	—		_	—		_	WAKFIL	_	_	_	SI	EG2PH<2:0	>	0000
BUIU	CICEG	15:0	SEG2PHTS	SAM	S	EG1PH<2:0	>		PRSEG<2:0	>	SJW	<1:0>			BRP<	5:0>			0000
B020	CUNT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	-	-	—	—	_	—	MODIE	CTMRIE	RBIE	TBIE	0000
D020	CIINI	15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF			_	—				MODIF	CTMRIF	RBIF	TBIF	0000
B030	C1VEC	31:16				—	_		—	_	—		_	—	_	_	_	—	0000
8000	011/20	15:0	—	—	—			FILHIT<4:0	>		—		-	1	CODE<6:0>		1		0040
B040	C1TREC	31:16	—	—	—	—	—	_	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
Bollo	office	15:0				TERRC	NT<7:0>		•					RERRCN	VT<7:0>				0000
B050	C1ESTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	_	—	0000
8000	01101/1	15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000
B060	C1RXOVE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8000	01101011	15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
B070	C1TMR	31:16								CANTS<	:15:0>								0000
20.0		15:0							CA	NTSPRE<15	:0>				-		1	l	0000
B080	C1RXM0	31:16						SID<10:0>							MIDE	—	EID<1	7:16>	xxxx
8000	Onotino	15:0								EID<1	5:0>						-		XXXX
BUOU	C1RXM1	31:16						SID<10:0>							MIDE	_	EID<1	7:16>	xxxx
D000	Onotim	15:0								EID<1	5:0>								xxxx
POAD	C1PVM2	31:16						SID<10:0>							MIDE	—	EID<1	7:16>	xxxx
BUAU	CTRAIMZ	15:0								EID<1	5:0>								xxxx
DUDU	C1PVM2	31:16						SID<10:0>							MIDE	_	EID<1	7:16>	xxxx
DUDU	CTRAINS	15:0								EID<1	5:0>								xxxx
DOCO		31:16	FLTEN3	MSEL	.3<1:0>			FSEL3<4:0	>		FLTEN2	MSEL	2<1:0>		F	SEL2<4:0>			0000
DUCU	CIFLICONU	15:0	FLTEN1	MSEL	.1<1:0>			FSEL1<4:0	>		FLTEN0	MSEL	0<1:0>		F	SEL0<4:0>			0000
PODO		31:16	FLTEN7	MSEL	.7<1:0>			FSEL7<4:0	>		FLTEN6	MSEL	6<1:0>		F	SEL6<4:0>			0000
PODO	CIFLICONI	15:0	FLTEN5	MSEL	.5<1:0>	> FSEL5<4:0> FLTEN4 MSEL4<1:0> FSEL4<4:0>								0000					
DOLO		31:16	6 FLTEN11 MSEL11<1:0> FSEL11<4:0> FLTEN10 MSEL10<1:0> FSEL10<4:0>								0000								
DUEU	C IFLI CON2	15:0) FLTEN9 MSEL9<1:0> FSEL9<4:0> FLTEN8 MSEL8<1:0> FSEL8<4:0>							0000									
DUEU		31:16	FLTEN15	MSEL ²	15<1:0>			FSEL15<4:0)>		FLTEN14	MSEL1	4<1:0>		F	SEL14<4:0>			0000
DUFU	GIFLICONS	15:0	FLTEN13	MSEL	13<1:0>			FSEL13<4:0)>		FLTEN12	MSEL1	2<1:0>		F	SEL12<4:0>			0000
D140	C1RXFn	31:16						SID<10:0>							EXID	—	EID<1	7:16>	xxxx
D140	U (n = 0-15) 15:0> EID<15:0>										XXXX								

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

x = unknown value on Reset; ---- = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information. Note 1:

REGISTER	23-10: C1FLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)
bit 20-16	FSEL2<4:0>: FIFO Selection bits
	11111 = Reserved
	•
	10000 = Reserved
	01111 = Message matching filter is stored in FIFO buffer 15
	•
	•
hit 15	ELTEN4: Filter 4 Enchle bit
DIUID	FLIENT: Filler I Effable bit
	0 = Filter is disabled
bit 14-13	MSEL1<1:0>: Filter 1 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
bit 12 8	ESEL 1 - Acceptance Mask 0 selected
DIL 12-0	11111 = Reserved
	•
	•
	10000 = Reserved
	01111 = Message matching filter is stored in FIFO buffer 15
	•
	•
	00000 = Message matching filter is stored in FIFO buffer 0
bit 7	FLTEN0: Filter 0 Enable bit
	1 = Filter is enabled
bit 6-5	MSEL 0-1:0>: Filter 0 Mack Select hits
bit 0-0	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 4-0	FSEL0<4:0>: FIFO Selection bits
	11111 = Reserved
	•
	•
	01111 = Message matching filter is stored in FIFO buffer 15
	•
	00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

29.0 INSTRUCTION SET

The PIC32MX1XX/2XX/5XX 64/100-pin family instruction set complies with the MIPS32[®] Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- · Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note: Refer to *"MIPS32[®] Architecture for Programmers Volume II: The MIPS32[®] Instruction Set"* at www.imgtec.com for more information.







АС СНА	ARACTER	ISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions			
Clock P	arameter	5								
AD50	TAD	ADC Clock Period ⁽²⁾	65	_	—	ns	See Table 31-35			
Conversion Rate										
AD55	TCONV	Conversion Time	_	12 TAD	—	_	—			
AD56 FCNV		Throughput Rate	—	—	1000	ksps	AVDD = 3.0V to 3.6V			
		(Sampling Speed)	—	—	400	ksps	AVDD = 2.5V to 3.6V			
AD57	TSAMP	Sample Time	1 Tad	—	—	—	TSAMP must be \geq 132 ns			
Timing	Paramete	rs								
AD60	TPCS	Conversion Start from Sample Trigger ⁽³⁾		1.0 Tad	—	_	Auto-Convert Trigger (SSRC<2:0> = 111) not selected			
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 Tad	—	1.5 Tad	_	_			
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1) ⁽³⁾	_	0.5 TAD	—		_			
AD63	TDPU	Time to Stabilize Analog Stage from ADC Off to ADC On ⁽³⁾		—	2	μS	—			

TABLE 31-36: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: Characterized by design but not tested.

4: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.