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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	81
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx250f256lt-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.2 Architecture Overview

The MIPS32[®] M4K[®] processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e[®] Support
- · Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32[®] M4K[®] processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation.

The execution unit includes:

- · 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- · Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32[®] M4K[®] processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1:MIPS32[®] M4K[®] PROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/
DIVIDE UNIT LATENCIES AND REPEAT RATES

Op code	Operand Size (mul rt) (div rs)	Latency	Repeat Rate							
MULT/MULTU, MADD/MADDU,	16 bits	1	1							
MSUB/MSUBU	32 bits	2	2							
MUL	16 bits	2	1							
	32 bits	3	2							
DIV/DIVU	8 bits	12	11							
	16 bits	19	18							
	24 bits	26	25							
	32 bits	33	32							

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	_	—	_	_	_	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:16	—	—	—	-	—	—	_	—	
45.0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	
15:8	CHBUSY	_	_	_	_	_	_	CHCHNS ⁽¹⁾	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0	
7:0	CHEN ⁽²⁾	CHAED	CHCHN	CHAEN	—	CHEDET	CHPF	RI<1:0>	

REGISTER 9-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER

Legend:

0				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-16 Unimplemented: Read as '0'

- bit 15 CHBUSY: Channel Busy bit
 - 1 = Channel is active or has been enabled
 - 0 = Channel is inactive or has been disabled
- bit 14-9 Unimplemented: Read as '0'
- bit 8 CHCHNS: Chain Channel Selection bit⁽¹⁾
 - 1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
 - 0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 CHEN: Channel Enable bit⁽²⁾

- 1 = Channel is enabled
- 0 = Channel is disabled

bit 6 CHAED: Channel Allow Events If Disabled bit

- 1 = Channel start/abort events will be registered, even if the channel is disabled
- 0 = Channel start/abort events will be ignored if the channel is disabled

bit CHCHN: Channel Chain Enable bit

- 1 = Allow channel to be chained
- 0 = Do not allow channel to be chained
- bit 4 CHAEN: Channel Automatic Enable bit
 - 1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
 0 = Channel is disabled on block transfer complete

bit 3 Unimplemented: Read as '0'

- bit 2 CHEDET: Channel Event Detected bit
 - 1 = An event has been detected
 - 0 = No events have been detected
- bit 1-0 CHPRI<1:0>: Channel Priority bits
 - 11 = Channel has priority 3 (highest)
 - 10 = Channel has priority 2
 - 01 = Channel has priority 1
 - 00 = Channel has priority 0
- Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).
 - 2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_		_	_	_	_	_
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8		_	_	_	_	—	_	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER

Legend:

0						
R = Readable bit	W = Writable bit	able bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-24 bit 23	Unimplemented: Read as '0' CHSDIE: Channel Source Done Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled	
bit 22	CHSHIE: Channel Source Half Empty Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled	
bit 21	CHDDIE: Channel Destination Done Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled	
bit 20	CHDHIE: Channel Destination Half Full Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled	
bit 19	CHBCIE: Channel Block Transfer Complete Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled	
bit 18	CHCCIE: Channel Cell Transfer Complete Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled	
bit 17	CHTAIE: Channel Transfer Abort Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled	
bit 16	CHERIE: Channel Address Error Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled	
bit 15-8	Unimplemented: Read as '0'	
bit 7	CHSDIF: Channel Source Done Interrupt Flag bit	
	1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)0 = No interrupt is pending	
bit 6	CHSHIF: Channel Source Half Empty Interrupt Flag bit 1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2 0 = No interrupt is pending)
bit 5	CHDDIF: Channel Destination Done Interrupt Flag bit 1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDS 0 = No interrupt is pending	IZ)
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Control Registers 10.1

TABLE 10-1: USB REGISTER MAP

(2) 31: (2) 31: (2) 31: (2) 31: (3)	31/19 :16 :16 :16 :16 :16 :16 :16 :16 :16 :16 :16 :16	30/14 	29/13 — — — —	28/12 — — —	27/11 — —	26/10 — —	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
E 15: AT(3) 31:' AT(3) 31:' 15: 15: 15: 15: 15: 15: 15: 15:	5:0 :16 5:0 :16 5:0 :16 :16		 	—	_		—										AII
$E \frac{31.^{\circ}}{15.}$ $E \frac{31.^{\circ}}{15.}$ $T = \frac{31.^{\circ}}{15.}$ $T = \frac{31.^{\circ}}{15.}$ $C = \frac{31.^{\circ}}{31.^{\circ}}$:16 5:0 :16 5:0 :16		-	—				—	—	_	_	_	_	_	_	_	000
E 15: AT ⁽³⁾ 31: 15: DN 31: 15: 15: 15: 31: 200 31: 15: 15: 15: 15: 15: 15: 15: 1	5:0 — :16 — 5:0 — :16 —	-	—				—	_	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	_	VBUSVDIF	000
15: AT ⁽³⁾ 31: 15: DN 31: 15: 15: 0 31: 15: 15: 15: 15: 15: 15: 15: 1	:16 — 5:0 — :16 —	-			—		_		_	_	—	_	_	_	_	_	000
AT(3) 15: ON 31: ⁷ 15: C 31: ⁷	5:0 <u>—</u> :16 —		—		—	—	—	-	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	000
ON 31: 	:16 —	—		—	—	—	—		—	—	-	-	—	—	—	—	000
ON 15: C 31:1			—	—	—	—	—		ID	—	LSTATE	-	SESVD	SESEND	—	VBUSVD	0000
15: C 31:1	5.0		—		—	—	—			—	—		—	—	—	—	0000
С —	5.0 —		—		—	—	—		DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
15.	:16 —		—		—	—	—			—	—		—	—	—	—	0000
15.	5:0 —		—		—	—	—		UACTPND ⁽⁴⁾	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR	0000
31:1	:16 —		—		—	—	—			—	—		—	—	—	—	0000
15:	5:0 —	-	_	_	_	_	_	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF DETACHIF	0000
31:1	:16 —		_				_		_	_	_	_	_	_	_	_	0000
15:		_	_	_	_	_	_	_	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE DETACHIE	0000
31:1	:16 —								_	_	_	_	_	_	_		0000
2) 15:			_		_	_	_	_	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF EOFEF	PIDEF	0000
31:1	:16 —	_	_	<u> </u>	_	_	_	_	_	_	_	_	_	_	_	_	0000
15:	5:0 —	_	_	_	_	_	_		BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE EOFEE	PIDEE	0000
31:1	:16 —	_	_	— —	_	_	_	_	_	_	_	_	_	_	_	_	0000
15:	5:0 —	—	_	_	_	_	_	_		ENDP	T<3:0>		DIR	PPBI	_	_	0000
31:1	:16 —	_	_	_			_	_	_		_	_	_	_	_	_	0000
l 15:	5:0 —	_	_	_	_	_	_	_	JSTATE	SE0	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN SOFEN	0000
31:1	:16 —	_					_		_	_	_	_	_	_	_		0000
~		<u> </u>					_						VADDR<6.)>			0000
.0.		<u> </u>		_					_	_	_	_	_			_	0000
31.1		_	_	_			_	_								_	0000
J	3) 31 1! 31 1! 1! 31 1! 31 1! 31 31 1! 31 31 31 31 31 31 31 31 31 31	$\begin{array}{c ccccc} 33 & 31:16 & \\ \hline 15:0 & \\ \hline 31:16 & \\ \hline 15:0 & \\ \hline 31:16 & \\ \hline 15:0 & \\ \hline 1 & 31:16 & \\ \hline 15:0 & \\ \hline 15:0 & \\ \hline \end{array}$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	a) $31:16$ $15:0$ $31:16$ $15:0$ $15:0$ $31:16$ $15:0$ 1 $31:16$ 1 $31:16$ 1 $31:16$ 1 $5:0$	a) $31:16$ - <	a) $31:16$ - <	a) $31:16$ - <	31:16	a) $31:16$ - -	a) $31:16$ $ -$ <	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information. Note 1:

2: This register does not have associated SET and INV registers.

This register does not have associated CLR, SET and INV registers. 3:

4: Reset value for this bit is undefined.

TABLE 10-1: USB REGISTER MAP (CONTINUED)

ess											Bit	s							(0
Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
E200	U1EP9	31:16	_	—		—	_	_	—	_		_	—	—	_	-	—		0000
5390	5390 U1EP9 15:0	15:0					-	-	—	_	-		—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53A0	U1EP10	31:16	_	_		_			_		_		_	—	-		—		0000
55A0	53A0 01EP10 15:0	15:0	Ι	Ι		_	-	-	_	_			—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0	U1EP11	31:16	_	_	_		_	_	—	_	_	_	—	—	_	_	—	_	0000
53BU	UIEPII	15:0	_	_	_		_	_	—	_	_	_	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53C0	U1EP12	31:16	_	_	_		_	_	—	_	_	_	—	—	_	_	—	_	0000
5500	UIEF 12	15:0	Ι	—	—	_	—	—	_	—	—	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53D0	U1EP13	31:16	Ι	—	—	_	—	—	_	—	—	_	_	—	—	—	—	—	0000
55D0	UIEF 13	15:0	Ι	—	—	_	—	—	_	—	—	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5050		31:16		_	_	_	_	_	_	_	_	_	-	_	_	_	_	_	0000
53E0	U1EP14	15:0	_	_			_	_	_	_			_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5050		31:16	_	_	_	_	_	_	_			_	_		_	_	_	_	0000
53F0	U1EP15	15:0	_	_	_	_	_	_	_			_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

REGISTER 13-1: TxCON: TYPE B TIMER 'x' CONTROL REGISTER ('x' = 2 THROUGH 5)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—		-	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	-	-	—	—	_	-	—
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
15:8	ON ^(1,3)	_	SIDL ⁽⁴⁾	—	—	_	_	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
7:0	TGATE ⁽³⁾	Т	CKPS<2:0>(3)	T32 ⁽²⁾		TCS ⁽³⁾	—

Legend:	
---------	--

R = Readable bit	W = Writable bit	t U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Timer On bit^(1,3)
 - 1 = Module is enabled 0 = Module is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit⁽⁴⁾
 - 1 = Discontinue operation when device enters Idle mode
 - 0 = Continue operation even in Idle mode
- bit 12-8 Unimplemented: Read as '0'
- bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit⁽³⁾

When TCS = 1:

This bit is ignored and is read as '0'.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

- bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits⁽³⁾
 - 111 = 1:256 prescale value
 - 110 = 1:64 prescale value
 - 101 = 1:32 prescale value
 - 100 = 1:16 prescale value
 - 011 = 1:8 prescale value
 - 010 = 1:4 prescale value
 - 001 = 1:2 prescale value
 - 000 = 1:1 prescale value
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - **2:** This bit is available only on even numbered timers (Timer2 and Timer4).
 - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3 and Timer5). All timer functions are set through the even numbered timers.
 - 4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

REGISTER 13-1: TxCON: TYPE B TIMER 'x' CONTROL REGISTER (CONTINUED)('x' = 2 THROUGH 5)

- bit 3 **T32:** 32-Bit Timer Mode Select bit⁽²⁾ 1 = Odd numbered and even numbered timers form a 32-bit timer 0 = Odd numbered and even numbered timers form a separate 16-bit timer
- bit 2 Unimplemented: Read as '0'
- bit 1 **TCS:** Timer Clock Source Select bit⁽³⁾
 - 1 = External clock from TxCK pin
 - 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit is available only on even numbered timers (Timer2 and Timer4).
 - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3 and Timer5). All timer functions are set through the even numbered timers.
 - 4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

14.0 WATCHDOG TIMER (WDT)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 9. "Watchdog, Deadman, and Power-up Timers" (DS60001114) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The Watchdog Timer (WDT), when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- · Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

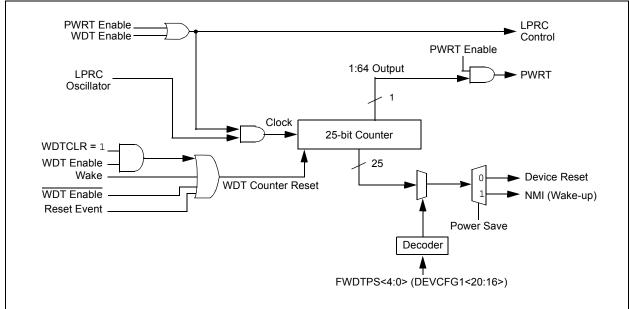


FIGURE 14-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM

16.1 Control Registers

TABLE 16-1: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 5 REGISTER MAP

ess										Bi	its								
Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
	OC1CON	31:16	—	—	—	—	—	—	—	—	—	_	_	—	—	_	—		0000
3000		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3010	OC1R	31:16 15:0								OC1R	<31:0>								xxxx xxxx
3020	OC1RS	31:16 15:0								OC1RS	6<31:0>								xxxx xxxx
		31:16	_	_	_	_	_	—	—	—	_	_	_	_	_	_	_	_	0000
3200	OC2CON	15:0	ON	_	SIDL	_	_	_	_	_	_	_	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
		31:16																	xxxx
3210	OC2R	15:0		OC2R<31:0>															
	OC2RS	31:16																	xxxx
3220		15:0		OC2RS<31:0>															
		31:16		_	_	_	_	_		_	_			_	_	_	_	_	0000
3400	OC3CON	15:0	ON	_	SIDL	-	_	_	_	_	_	_	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
0.440	0.000	31:16								0.000	-0.1.0:								xxxx
3410	OC3R	15:0	OC3R<31:0>																
3420	OC3RS	31:16	OC3RS<31:0>																
3420	UCSRS	15:0								UCSRE	5<31.0>								xxxx
3600	OC4CON	31:16	_	—	_	—	—	—	—	—	_	—	—	—	—		—		0000
3000	004001	15:0	ON	_	SIDL	_	_	_	-	_	_	_	OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3610	OC4R	31:16								OC4R	~31.0>								xxxx
3010	0040	15:0								0040	<31.02								xxxx
3620	OC4RS	31:16								OC4RS	2<31.05								xxxx
3020	00403	15:0		-		-	-	-	-	00400	5-51.02	-			-				xxxx
3800	OC5CON	31:16	—	—	—	—	—				—	—	—		—		—	—	0000
5000	00000	15:0	ON	—	SIDL	_	—	_	—	_	—		OC32	OCFLT	OCTSEL		OCM<2:0>		0000
3810	OC5R	31:16								OC5R	<31.0>								xxxx
3010	0001	15:0								0000	-01.04								xxxx
3820	OC5RS	31:16								00589	S<31:0>								xxxx
0020	000100	15:0								OUSKE	-01.0-								xxxx

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0						
04.04	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0						
31:24	—	—	—	RXBUFELM<4:0>										
00.40	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0						
23:16	— — — TXBUFELM<4:0>													
45.0	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0						
15:8		—	—	FRMERR	SPIBUSY		_	SPITUR						
7.0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0						
7:0	SRMT	SPIROV	SPIRBE		SPITBE	_	SPITBF	SPIRBF						

Legend:	C = Clearable bit	HS = Set in hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

- bit 31-29 Unimplemented: Read as '0'
- bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 23-21 Unimplemented: Read as '0'
- bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 15-13 Unimplemented: Read as '0'
- bit 12 **FRMERR:** SPI Frame Error status bit
 - 1 = Frame error detected
 - 0 = No Frame error detected
 - This bit is only valid when FRMEN = 1.
- bit 11 SPIBUSY: SPI Activity Status bit
 - 1 = SPI peripheral is currently busy with some transactions
 - 0 = SPI peripheral is currently idle
- bit 10-9 Unimplemented: Read as '0'
- bit 8 **SPITUR:** Transmit Under Run bit
 - 1 = Transmit buffer has encountered an underrun condition
 - 0 = Transmit buffer has no underrun condition
 - This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or writing a '0' to SPITUR.
- bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
 - 1 = When SPI module shift register is empty
 - 0 = When SPI module shift register is not empty
- bit 6 SPIROV: Receive Overflow Flag bit
 - 1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
 - 0 = No overflow has occurred
 - This bit is set in hardware; can bit only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or by writing a '0' to SPIROV.
- bit 5 SPIRBE: RX FIFO Empty bit (valid only when ENHBUF = 1) 1 = RX FIFO is empty (CRPTR = SWPTR) 0 = RX FIFO is not empty (CRPTR ≠ SWPTR)
- bit 4 Unimplemented: Read as '0'

NOTES:

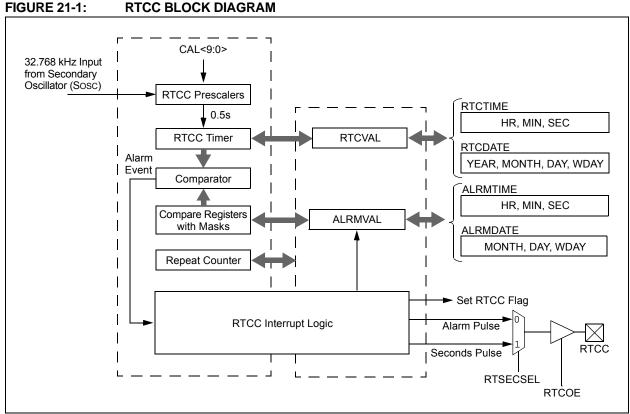
21.0 **REAL-TIME CLOCK AND** CALENDAR (RTCC)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 29. "Real-Time Clock and Calendar (RTCC)" (DS60001125) in the "PIC32 Family Reference Manual", which is available the Microchip web from site (www.microchip.com/PIC32).

The PIC32 RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are the key features of this module:

- · Time: hours. minutes and seconds
- 24-hour format (military time)
- · Visibility of one-half second period
- · Provides calendar: Weekday, date, month and year
- · Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month and one year
- · Alarm repeat with decrementing counter
- · Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- · BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- · User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- · Calibrates up to 260 ppm of crystal error
- · Requirements: External 32.768 kHz clock crystal
- · Alarm pulse or seconds clock output on RTCC pin



RTCC BLOCK DIAGRAM

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	—	—	_	—	—	—			
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:16	—	—	—	—	_	—	—	—			
45.0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	ALRMEN ^(1,2)	CHIME ⁽²⁾	PIV ⁽²⁾	ALRMSYNC ⁽³⁾	AMASK<3:0> ⁽³⁾						
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0	ARPT<7:0> ⁽³⁾										

REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-16 Unimplemented: Read as '0'

- bit 15 ALRMEN: Alarm Enable bit^(1,2)
 - 1 = Alarm is enabled
 - 0 = Alarm is disabled

bit 14 CHIME: Chime Enable bit⁽²⁾

- 1 = Chime is enabled ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit⁽²⁾

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse. When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 ALRMSYNC: Alarm Sync bit⁽³⁾

- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 AMASK<3:0>: Alarm Mask Configuration bits⁽³⁾

- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved; do not use
- 1011 = Reserved; do not use
- 11xx = Reserved; do not use
- **Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
 - 2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
 - 3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

23.1 **Control Registers**

TABLE 23-1: CAN1 REGISTER SUMMARY

ess										Bit	5								
Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
	01001	31:16	_	_	_	_	ABAT	F	REQOP<2:0	>	(OPMOD<2:0	>	CANCAP	_	_	_	_	0480
B000	C1CON	15:0	ON	_	SIDLE		CANBUSY	—	_	_	-	_	_		D	NCNT<4:0>	•	•	0000
B010	C1CFG	31:16	_	_	_		_	_	-			WAKFIL	_	-	-	S	EG2PH<2:0	>	0000
8010	CICFG	15:0	SEG2PHTS	SAM				ŀ	PRSEG<2:0	>	SJW	<1:0>			BRP<	:5:0>			0000
B020	C1INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE		_		_	_	_	_	MODIE	CTMRIE	RBIE	TBIE	0000
0020	01111	15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000
B030	C1VEC	31:16	—	—	—	—	—	_	—	—	_	—	—	—	—	—	—	—	0000
2000		15:0	—		_			FILHIT<4:0>	>						CODE<6:0>				0040
B040	C1TREC	31:16	—	_	_	—	_	_	—	—	—	_	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
		15:0				TERRC	NT<7:0>							RERRCN	T<7:0>				0000
B050	C1FSTAT	31:16	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0000
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000
B060	C1RXOVF	31:16 15:0	— RXOVF15	— RXOVF14	– RXOVF13		– RXOVF11	– RXOVF10	– RXOVF9	– RXOVF8	RXOVF7	– RXOVF6	– RXOVF5	— RXOVF4	– RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
		31:16	KAUVE 15	KAUVF14	RAUVEIS	RAUVE 12	RAUVEII	RAUVEIU	KAUVF9	CANTS<		RAUVEO	RAUVED	KAUVF4	RAUVES	RAUVF2	RAUVEI	RAUVFU	0000
B070	C1TMR	15:0											0000						
		31:16						SID<10:0>	0A		05				MIDE	_	EID<1	7.16>	xxxx
B080	C1RXM0	15:0						012 110.0		EID<1	5.0>				MIDE			7.10	XXXX
		31:16													xxxx				
B090	C1RXM1	15:0																	
		31:16						SID<10:0>		210 11					MIDE	_	EID<1	7.16>	xxxx
B0A0	C1RXM2	15:0						0.0 10.0		EID<1	5:0>						2.0		XXXX
		31:16						SID<10:0>							MIDE	_	EID<1	7:16>	xxxx
B0B0	C1RXM3	15:0								EID<1	5:0>						ļ		xxxx
		31:16	FLTEN3	MSEL	3<1:0>			FSEL3<4:0>	>		FLTEN2	MSEL	2<1:0>		F	SEL2<4:0>			0000
B0C0	C1FLTCON0	15:0	FLTEN1	MSEL	1<1:0>			FSEL1<4:0>	>		FLTEN0	MSEL	0<1:0>		F	SEL0<4:0>			0000
	0.151 700114	31:16	FLTEN7	MSEL	7<1:0>			FSEL7<4:0>	>		FLTEN6	MSEL	6<1:0>		F	SEL6<4:0>			0000
B0D0	C1FLTCON1	15:0	FLTEN5	MSEL	5<1:0>			FSEL5<4:0>	`		FLTEN4	MSEL	4<1:0>		F	SEL4<4:0>			0000
DOFO		31:16	FLTEN11	MSEL ²	11<1:0>			FSEL11<4:0	>		FLTEN10	MSEL ²	10<1:0>		F	SEL10<4:0>	•		0000
B0E0	C1FLTCON2 15:0 FLTEN9 MSEL9<1:0> FSEL9<4:0> FLTEN8 MSEL8<1:0> FSEL8<4:0>									0000									
B0F0	C1FLTCON3	31:16	FLTEN15	MSEL1	15<1:0>			FSEL15<4:0	>		FLTEN14	MSEL'	14<1:0>		F	SEL14<4:0>	•		0000
BUFU	GIFLI CONS	15:0	FLTEN13	MSEL1	13<1:0>			FSEL13<4:0	>		FLTEN12	MSEL'	12<1:0>		F	SEL12<4:0>	·		0000
B140	Onoan	31:16						SID<10:0>							EXID		EID<1	7:16>	xxxx
040	(n = 0-15)	15:0						aa ara ahawr		EID<1	5:0>								xxxx

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x = unknown value on Reset; ---- = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information. Note 1:

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REGISTER 23-11: C1FLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED) bit 20-16 FSEL6<4:0>: FIFO Selection bits 11111 = Reserved 10000 = Reserved 01111 = Message matching filter is stored in FIFO buffer 15 00000 = Message matching filter is stored in FIFO buffer 0 FLTEN5: Filter 17 Enable bit bit 15 1 = Filter is enabled 0 = Filter is disabled bit 14-13 MSEL5<1:0>: Filter 5 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected bit 12-8 FSEL5<4:0>: FIFO Selection bits 11111 = Reserved 10000 = Reserved 01111 = Message matching filter is stored in FIFO buffer 15 00000 = Message matching filter is stored in FIFO buffer 0 bit 7 FLTEN4: Filter 4 Enable bit 1 = Filter is enabled 0 = Filter is disabled bit 6-5 MSEL4<1:0>: Filter 4 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected FSEL4<4:0>: FIFO Selection bits bit 4-0 11111 = Reserved 10000 = Reserved 01111 = Message matching filter is stored in FIFO buffer 15 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	_	—	—	_	_	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
10.0	ON ⁽¹⁾	COE	CPOL ⁽²⁾	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
7:0	EVPOL	_<1:0>	_	CREF	_		CCH	<1:0>

REGISTER 24-1: CMxCON: COMPARATOR CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Comparator ON bit⁽¹⁾
 - 1 = Module is enabled. Setting this bit does not affect the other bits in this register
 - 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register
- bit 14 **COE:** Comparator Output Enable bit
 - 1 = Comparator output is driven on the output CxOUT pin
 - 0 = Comparator output is not driven on the output CxOUT pin
- bit 13 **CPOL:** Comparator Output Inversion bit⁽²⁾
 - 1 = Output is inverted
 - 0 = Output is not inverted
- bit 12-9 Unimplemented: Read as '0'
- bit 8 **COUT:** Comparator Output bit
 - 1 = Output of the Comparator is a '1'
 - 0 = Output of the Comparator is a '0'
- bit 7-6 EVPOL<1:0>: Interrupt Event Polarity Select bits
 - 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
 - 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
 - 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
 - 00 = Comparator interrupt generation is disabled
- bit 5 Unimplemented: Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit

- 1 = Comparator non-inverting input is connected to the internal CVREF
- 0 = Comparator non-inverting input is connected to the CXINA pin

bit 3-2 Unimplemented: Read as '0'

- bit 1-0 CCH<1:0>: Comparator Negative Input Select bits for Comparator
 - 11 = Comparator inverting input is connected to the IVREF
 - 10 = Comparator inverting input is connected to the CxIND pin
 - 01 = Comparator inverting input is connected to the CxINC pin
 - 00 = Comparator inverting input is connected to the CxINB pin
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

31.0 40 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX/5XX 64/100-pin Family electrical characteristics for devices that operate at 40 MHz. Refer to **Section 32.0** "**50 MHz Electrical Characteristics**" for additional specifications for operations at higher frequency. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX1XX/2XX/5XX 64/100-pin Family devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

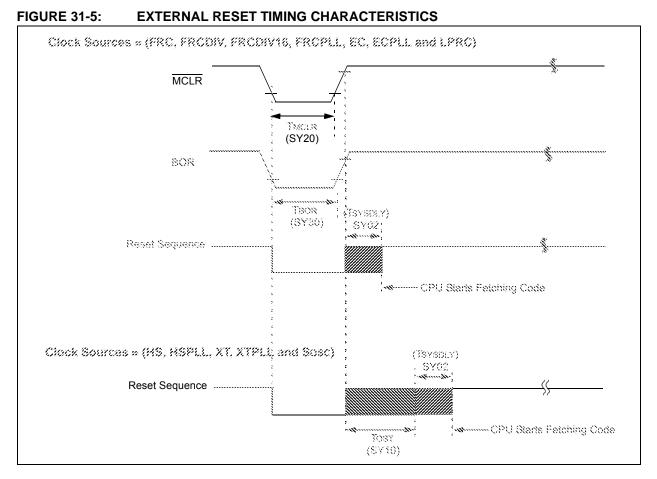
Ambient temperature under bias	40°C to +105°C
Storage temperature	
Voltage on VDD with respect to Vss	
Voltage on any pin that is not 5V tolerant, with respect to Vss (Note 3)	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 2.3V$ (Note 3)	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 2.3V (Note 3)	-0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3	0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of Vss pin(s)	
Maximum current into VDD pin(s) (Note 2)	
Maximum output current sunk by any I/O pin	15 mA
Maximum output current sourced by any I/O pin	15 mA
Maximum current sunk by all ports	
Maximum current sourced by all ports (Note 2)	200 mA

Note 1: Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

3: See the "Device Pin Tables" section for the 5V tolerant pins.

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AC CHA	RACTERI	ISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions		
SY00	Τρυ	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μS			
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.		1 μs + 8 SYSCLK cycles	_	_	_		
SY20	TMCLR	MCLR Pulse Width (low)	2	_		μS	—		
SY30	TBOR	BOR Pulse Width (low)	_	1	—	μS	_		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

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ISBN: 978-1-5224-0488-0