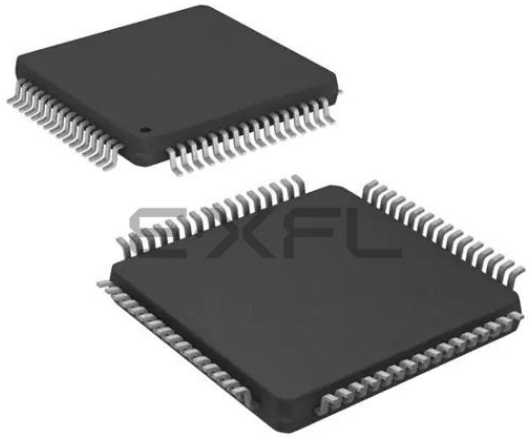
Microchip Technology - PIC32MX270F512H-I/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f512h-i-pt

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP			
PMA2	8	14	O	TTL/ST	Parallel Master Port data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMA3	6	12	O	TTL/ST	
PMA4	5	11	O	TTL/ST	
PMA5	4	10	O	TTL/ST	
PMA6	16	29	O	TTL/ST	
PMA7	22	28	O	TTL/ST	
PMA8	32	50	O	TTL/ST	
PMA9	31	49	O	TTL/ST	
PMA10	28	42	O	TTL/ST	
PMA11	27	41	O	TTL/ST	
PMA12	24	35	O	TTL/ST	
PMA13	23	34	O	TTL/ST	
PMA14	45	71	O	TTL/ST	
PMA15	44	70	O	TTL/ST	
PMCS1	45	71	O	TTL/ST	Parallel Master Port data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMCS2	44	70	O	TTL/ST	
PMD0	60	93	I/O	TTL/ST	
PMD1	61	94	I/O	TTL/ST	
PMD2	62	98	I/O	TTL/ST	
PMD3	63	99	I/O	TTL/ST	
PMD4	64	100	I/O	TTL/ST	
PMD5	1	3	I/O	TTL/ST	
PMD6	2	4	I/O	TTL/ST	
PMD7	3	5	I/O	TTL/ST	
PMD8	—	90	I/O	TTL/ST	
PMD9	—	89	I/O	TTL/ST	
PMD10	—	88	I/O	TTL/ST	
PMD11	—	87	I/O	TTL/ST	
PMD12	—	79	I/O	TTL/ST	
PMD13	—	80	I/O	TTL/ST	
PMD14	—	83	I/O	TTL/ST	
PMD15	—	84	I/O	TTL/ST	
PMRD	53	82	O	—	Parallel Master Port Read Strobe
PMWR	52	81	O	—	Parallel Master Port Write Strobe
V_{BUS} **(2)**	34	54	I	Analog	USB Bus Power Monitor

Legend: CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

2.9 Considerations When Interfacing to Remotely Powered Circuits

2.9.1 NON-5V TOLERANT INPUT PINS

A quick review of the absolute maximum rating section in **31.0 "40 MHz Electrical Characteristics"** will indicate that the voltage on any non-5v tolerant pin may not exceed AVDD/VDD + 0.3V. Figure 2-5 shows an example of a remote circuit using an independent power source, which is powered while connected to a PIC32 non-5V tolerant circuit that is not powered.

FIGURE 2-5: PIC32 NON-5V TOLERANT CIRCUIT EXAMPLE

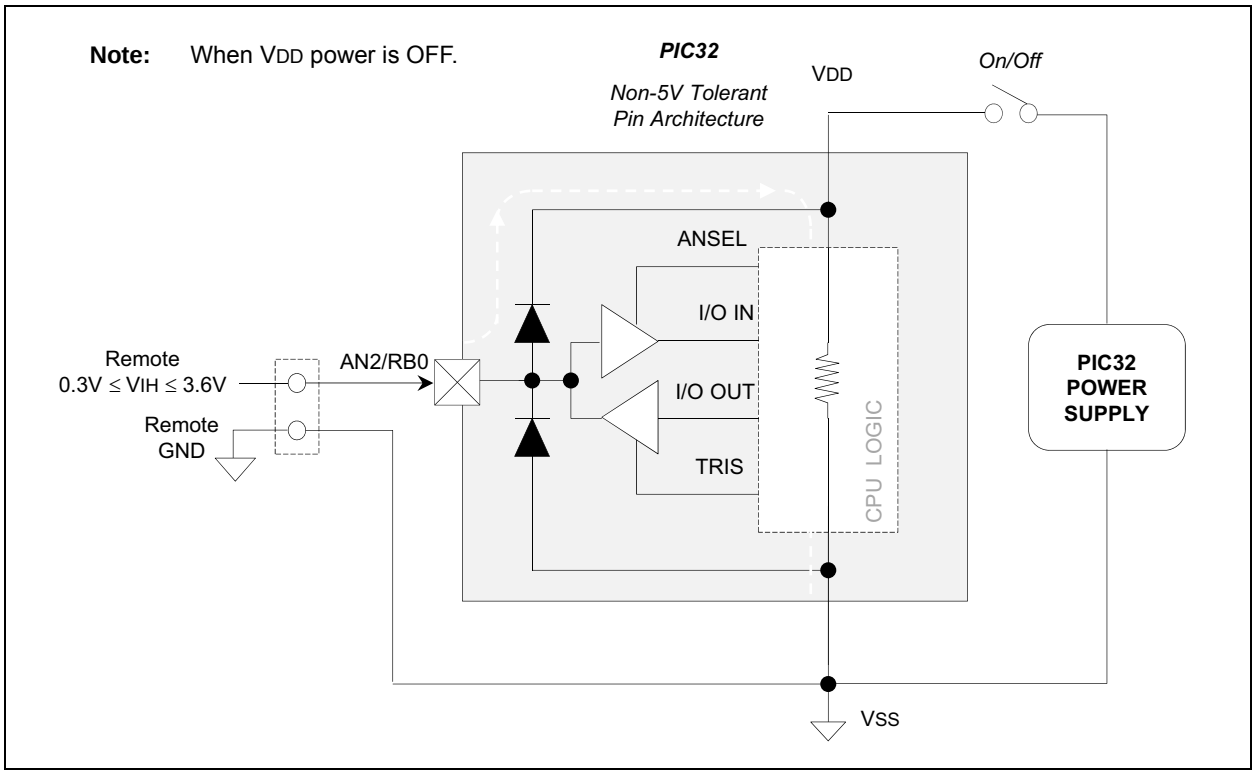
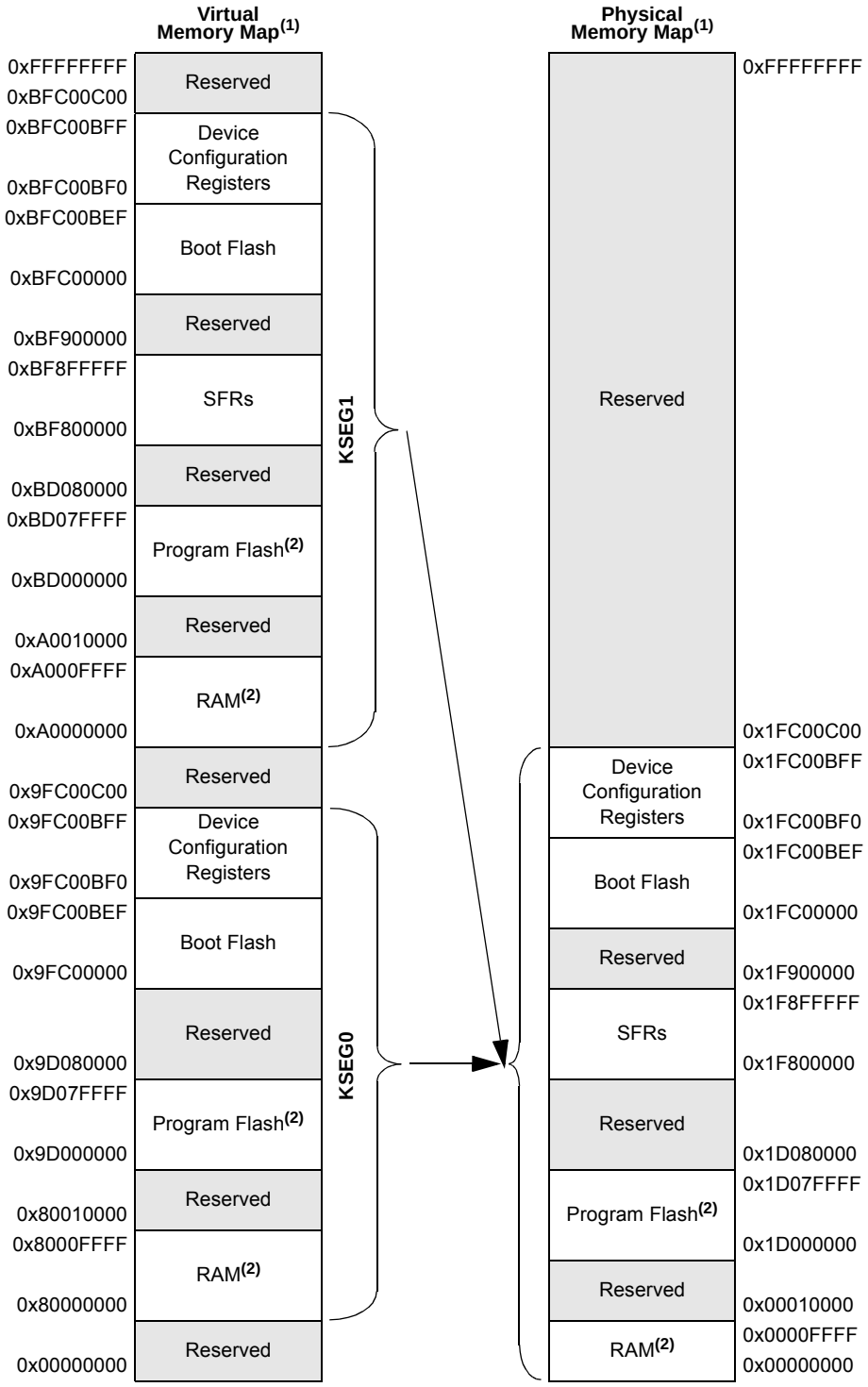


FIGURE 4-4: MEMORY MAP FOR DEVICES WITH 512 KB OF PROGRAM MEMORY + 64 KB RAM



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

REGISTER 5-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **IP1<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

Note: This register represents a generic definition of the IPCx register. Refer to Table 5-1 for the exact bit definitions.

NOTES:

REGISTER 9-16: DCHxCSIZ: DMA CHANNEL 'x' CELL-SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>:** Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event
.
.
.
0000000000000010 = 2 bytes transferred on an event
0000000000000001= 1 byte transferred on an event
0000000000000000 = 65,536 bytes transferred on an event

REGISTER 9-17: DCHxCPTR: DMA CHANNEL 'x' CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<7:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event
.
.
.
0000000000000001 = 1 byte has been transferred since the last event
0000000000000000 = 0 bytes have been transferred since the last event

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 10-18: U1BDTP2: USB BDT PAGE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<23:16>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** BDT Base Address bits

This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

REGISTER 10-19: U1BDTP3: USB BDT PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<31:24>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** BDT Base Address bits

This 8-bit value provides address bits 31 through 24 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

TABLE 11-1: INPUT PIN SELECTION

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT3	INT3R	INT3R<3:0>	0000 = RPD2 0001 = RPG8 0010 = RPF4 0011 = RPD10 0100 = RPF1 0101 = RPB9 0110 = RPB10 0111 = RPC14 1000 = RPB5(7) 1001 = Reserved 1010 = RPC1(3) 1011 = RPD14(3) 1100 = RPG1(3) 1101 = RPA14(3) 1110 = Reserved 1111 = RPF2(1)
T2CK	T2CKR	T2CKR<3:0>	
IC3	IC3R	IC3R<3:0>	
U1RX	U1RXR	U1RXR<3:0>	
U2RX	U2RXR	U2RXR<3:0>	
$\overline{\text{U5CTS}}$(3)	U5CTSR	U5CTSR<3:0>	
SDI3	SDI3R	SDI3R<3:0>	
SDI4(3)	SDI4R	SDI4R<3:0>	
REFCLKI	REFCLKIR	REFCLKIR<3:0>	
INT4	INT4R	INT4R<3:0>	0000 = RPD3 0001 = RPG7 0010 = RPF5 0011 = RPD11 0100 = RPF0 0101 = RPB1 0110 = RPE5 0111 = RPC13 1000 = RPB3 1001 = RPF12(3) 1010 = RPC4(3) 1011 = RPD15(3) 1100 = RPG0(3) 1101 = RPA15(3) 1110 = RPF2(1) 1111 = RPF7(2)
T5CK	T5CKR	T5CKR<3:0>	
IC4	IC4R	IC4R<3:0>	
U3RX	U3RXR	U3RXR<3:0>	
$\overline{\text{U4CTS}}$	U4CTSR	U4CTSR<3:0>	
SDI1	SDI1R	SDI1R<3:0>	
SDI2	SDI2R	SDI2R<3:0>	
C1RX(5)	C1RXR(5)	C1RXR<3:0>(5)	
INT2	INT2R	INT2R<3:0>	0000 = RPD9 0001 = RPG6 0010 = RPB8 0011 = RPB15 0100 = RPD4 0101 = RPB0 0110 = RPE3 0111 = RPB7 1000 = Reserved 1001 = RPF12(3) 1010 = RPD12(3) 1011 = RPF8(3) 1100 = RPC3(3) 1101 = RPE9(3) 1110 = RPD14(3) 1111 = RPB2
T4CK	T4CKR	T4CKR<3:0>	
IC2	IC2R	IC2R<3:0>	
IC5	IC5R	IC5R<3:0>	
$\overline{\text{U1CTS}}$	U1CTSR	U1CTSR<3:0>	
$\overline{\text{U2CTS}}$	U2CTSR	U2CTSR<3:0>	
$\overline{\text{SS1}}$	SS1R	SS1R<3:0>	
$\overline{\text{SS3}}$	SS3R	SS1R<3:0>	
$\overline{\text{SS4}}$(3)	SS3R	SS3R<3:0>	

Note 1: This selection is not available on 64-pin USB devices.

2: This selection is only available on 100-pin General Purpose devices.

3: This selection is not available on 64-pin devices.

4: This selection is not available when USBID functionality is used on USB devices.

5: This selection is not available on devices without a CAN module.

6: This selection is not available on USB devices.

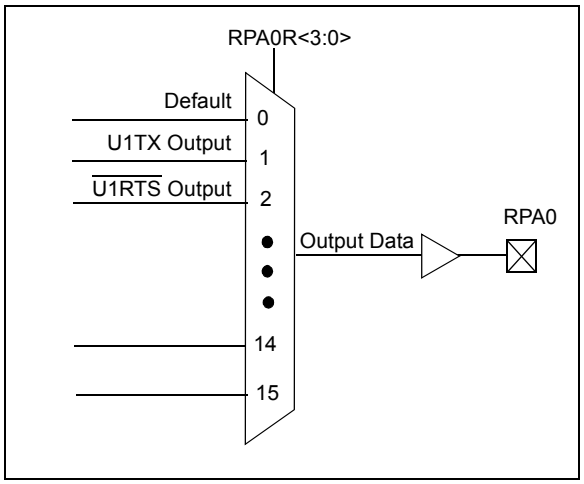
7: This selection is not available when VBUSON functionality is used on USB devices.

11.3.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the peripheral pin select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 11-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 11-2 and Figure 11-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPA0



11.3.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

11.3.6.1 Control Register Lock

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

11.3.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

NOTES:

REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(2)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPI Peripheral On bit(1)
1 = SPI Peripheral is enabled
0 = SPI Peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when CPU enters in Idle mode
0 = Continue operation in Idle mode

bit 12 **DISSDO:** Disable SDOx pin bit
1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16-Bit Communication Select bits
When AUDEN = 1:
MODE32 MODE16 Communication
11 24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
10 32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
01 16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame
00 16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame

When AUDEN = 0:
MODE32 MODE16 Communication
1x 32-bit
01 16-bit
00 8-bit

bit 9 **SMP:** SPI Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPI Clock Edge Select bit(3)
1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)

bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
1 = SSx pin used for Slave mode
0 = SSx pin not used for Slave mode, pin controlled by port function.

bit 6 **CKP:** Clock Polarity Select bit(4)
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

Note 1: When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit can only be written when the ON bit = 0.

3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

19.2 Timing Diagrams

Figure 19-2 and Figure 19-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 19-2: UART RECEPTION

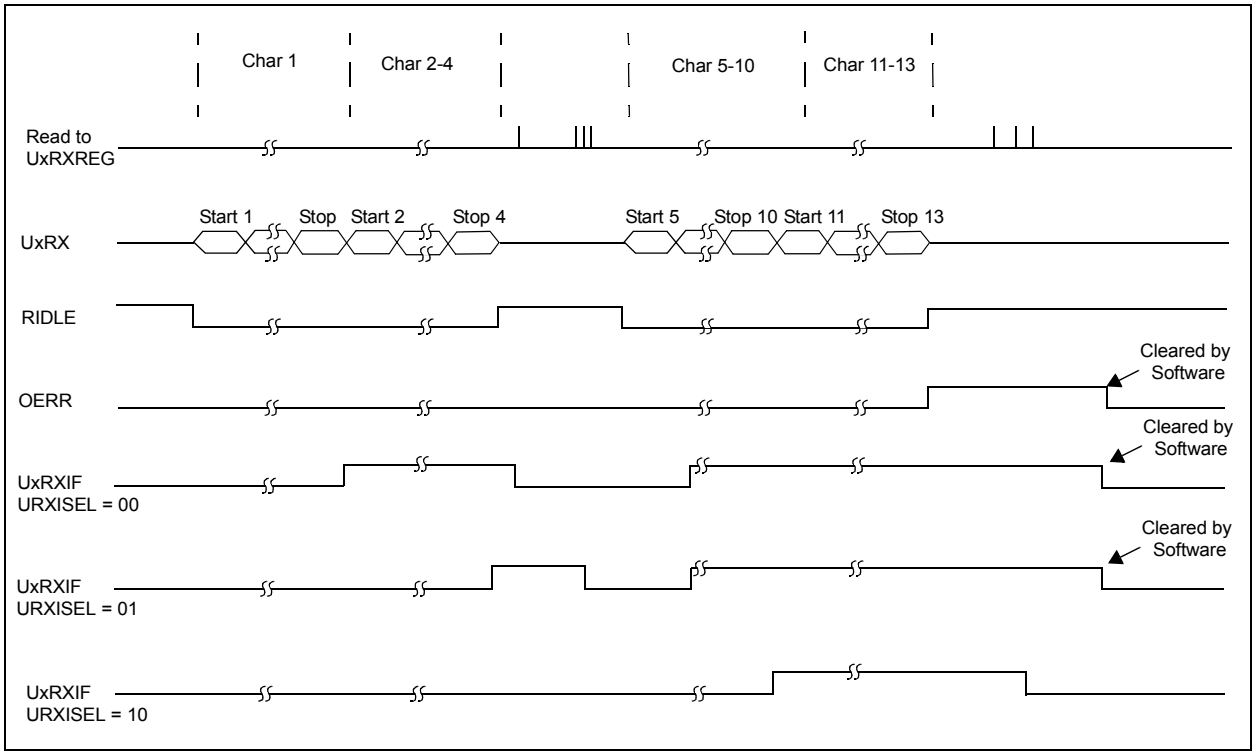
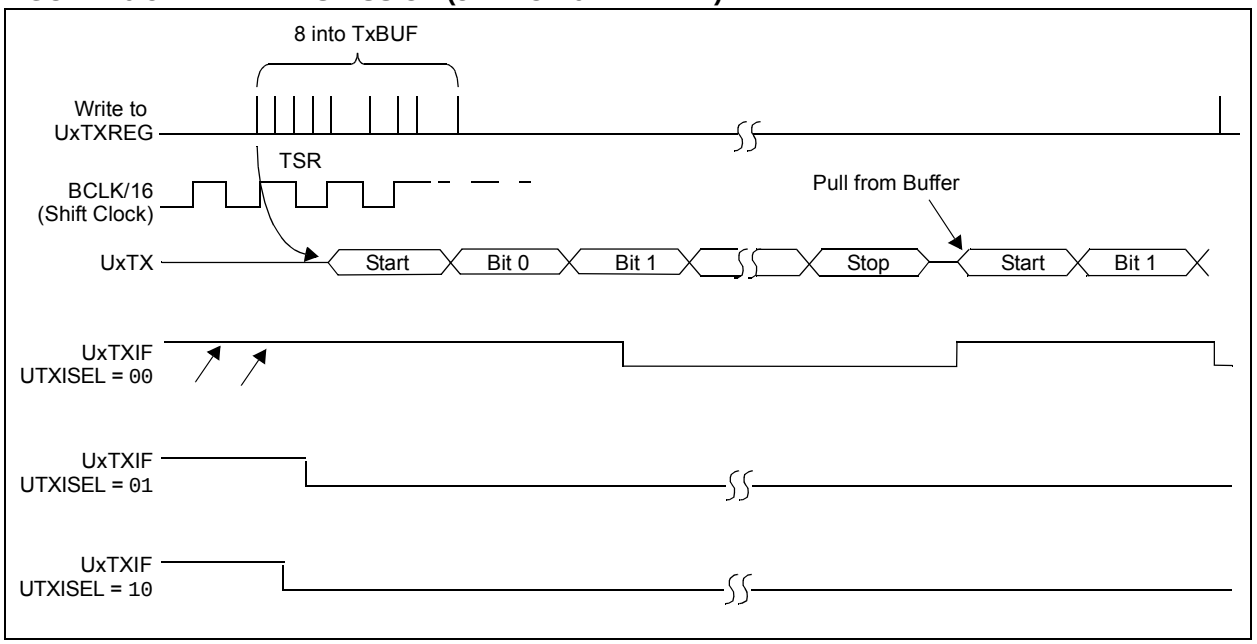


FIGURE 19-3: TRANSMISSION (8-BIT OR 9-BIT DATA)



REGISTER 23-3: C1INT: CAN INTERRUPT REGISTER (CONTINUED)

bit 14 **WAKIF:** CAN Bus Activity Wake-up Interrupt Flag bit
1 = A bus wake-up activity interrupt has occurred
0 = A bus wake-up activity interrupt has not occurred

bit 13 **CERRIF:** CAN Bus Error Interrupt Flag bit
1 = A CAN bus error has occurred
0 = A CAN bus error has not occurred

bit 12 **SERRIF:** System Error Interrupt Flag bit(1)
1 = A system error occurred (typically an illegal address was presented to the system bus)
0 = A system error has not occurred

bit 11 **RBOVIF:** Receive Buffer Overflow Interrupt Flag bit
1 = A receive buffer overflow has occurred
0 = A receive buffer overflow has not occurred

bit 10-4 **Unimplemented:** Read as '0'

bit 3 **MODIF:** CAN Mode Change Interrupt Flag bit
1 = A CAN module mode change has occurred (OPMOD<2:0> has changed to reflect REQOP)
0 = A CAN module mode change has not occurred

bit 2 **CTMRIF:** CAN Timer Overflow Interrupt Flag bit
1 = A CAN timer (CANTMR) overflow has occurred
0 = A CAN timer (CANTMR) overflow has not occurred

bit 1 **RBIF:** Receive Buffer Interrupt Flag bit
1 = A receive buffer interrupt is pending
0 = A receive buffer interrupt is not pending

bit 0 **TBIF:** Transmit Buffer Interrupt Flag bit
1 = A transmit buffer interrupt is pending
0 = A transmit buffer interrupt is not pending

Note 1: This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (C1CON<15>).

REGISTER 23-10: C1FLTCON0: CAN FILTER CONTROL REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN3	MSEL3<1:0>		FSEL3<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN2	MSEL2<1:0>		FSEL2<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN1	MSEL1<1:0>		FSEL1<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN0	MSEL0<1:0>		FSEL0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN3:** Filter 3 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL3<1:0>:** Filter 3 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL3<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN2:** Filter 2 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL2<1:0>:** Filter 2 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 23-12: C1FLTCON2: CAN FILTER CONTROL REGISTER 2 (CONTINUED)

bit 20-16 **FSEL10<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 15 **FLTEN9:** Filter 9 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL9<1:0>:** Filter 9 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL9<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN8:** Filter 8 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL8<1:0>:** Filter 8 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL8<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	CTMUSIDL	TGEN(1)	EDGEN	EDGSEQEN	IDISSEN(2)	CTTRIG
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ITRIM<5:0>						IRNG<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **EDG1MOD:** Edge 1 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 30 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 programmed for a positive edge response
0 = Edge 1 programmed for a negative edge response

bit 29-26 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = IC4 Capture Event is selected
1110 = C2OUT pin is selected
1101 = C1OUT pin is selected
1100 = IC3 Capture Event is selected
1011 = IC2 Capture Event is selected
1010 = IC1 Capture Event is selected
1001 = CTED8 pin is selected
1000 = CTED7 pin is selected
0111 = CTED6 pin is selected
0110 = CTED5 pin is selected
0101 = CTED4 pin is selected
0100 = CTED3 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 25 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control edge source
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

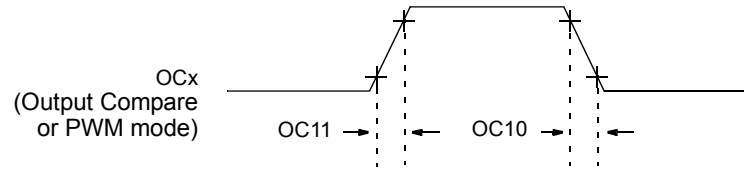
Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 31-41) in **Section 31.0 "40 MHz Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

FIGURE 31-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 31-1 for load conditions.

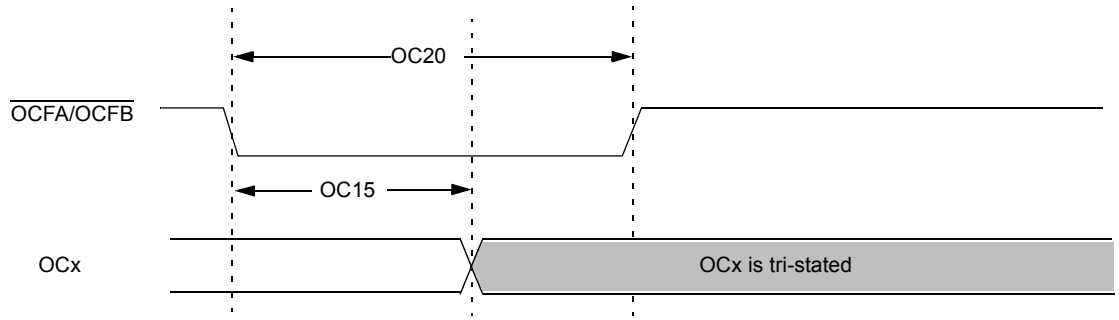
TABLE 31-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 31-9: OCx/PWM MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 31-1 for load conditions.

TABLE 31-27: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Typical(2)**	**Max**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 31-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP51	TSSH2DOZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 4)**	5	—	25	ns	—
SP52	TSCH2SSH TSCL2SSH	$\overline{SSx}$ ↑ after SCKx Edge	TSCK + 20	—	—	ns	—
SP60	TSSL2DOV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	25	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns.

4: Assumes 50 pF load on all SPIx pins.

TABLE 31-37: PARALLEL SLAVE PORT REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param.No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PS1	TdtV2wrH	Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20	—	—	ns	—
PS2	TwrH2dtI	$\overline{WR}$ or $\overline{CS}$ Inactive to Data-In Invalid (hold time)	40	—	—	ns	—
PS3	TrdL2dtV	$\overline{RD}$ and $\overline{CS}$ Active to Data-Out Valid	—	—	60	ns	—
PS4	TrdH2dtI	$\overline{RD}$ Active or $\overline{CS}$ Inactive to Data-Out Invalid	0	—	10	ns	—
PS5	Tcs	$\overline{CS}$ Active Time	TPB + 40	—	—	ns	—
PS6	TWR	$\overline{WR}$ Active Time	TPB + 25	—	—	ns	—
PS7	TRD	$\overline{RD}$ Active Time	TPB + 25	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 31-21: PARALLEL MASTER PORT READ TIMING DIAGRAM

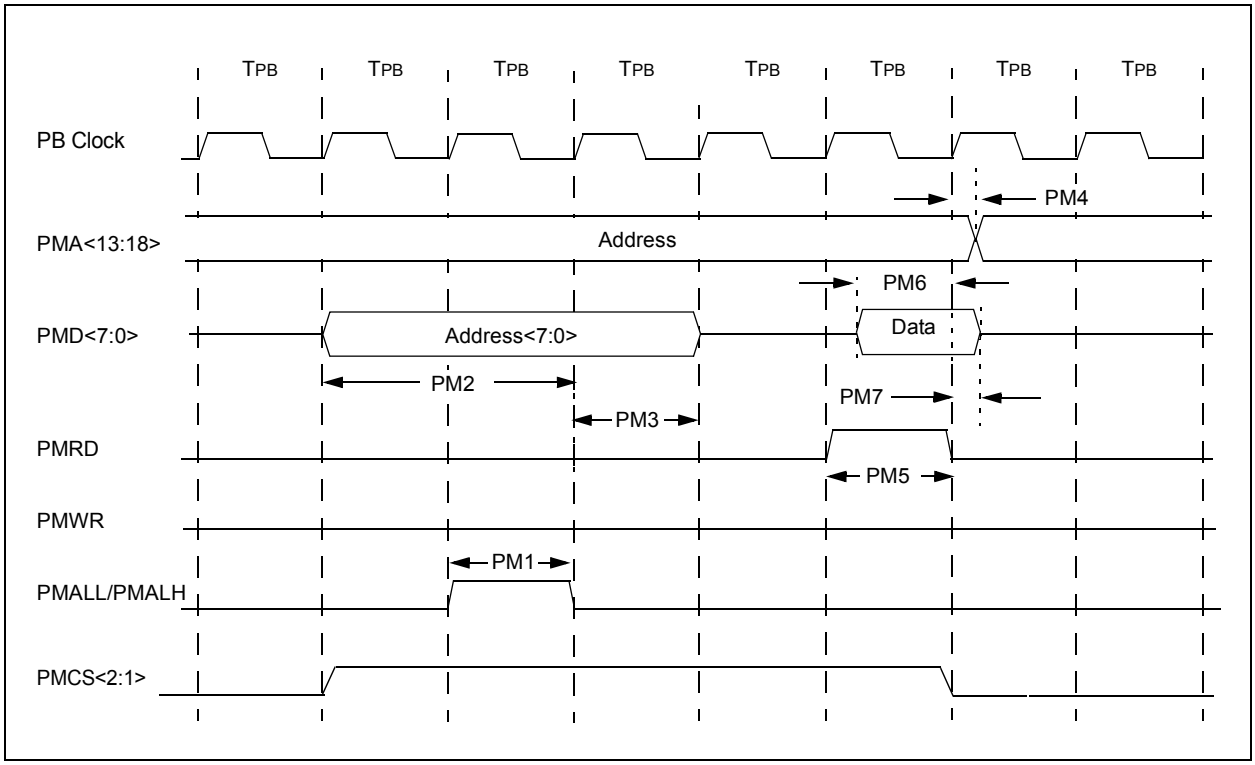


TABLE 32-3: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial	
Parameter No.	**Typical(2)**	**Max.**	**Units**	**Conditions**
Idle Current (I_{IDLE}): Core Off, Clock on Base Current (Note 1)				
MDC34a	9.5	24	mA	50 MHz

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 32-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial		
Param. No.	**Typical(2)**	**Max.**	**Units**	**Conditions**	
Power-Down Current (I_{PD}) (Note 1)					
MDC40k	50	150	µA	-40°C	Base Power-Down Current
MDC40n	250	650	µA	+85°C	
Module Differential Current					
MDC41e	15	55	µA	3.6V	Watchdog Timer Current: ΔI_{WDT} **(Note 3)**
MDC42e	34	55	µA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Note 3)**
MDC43d	1100	1800	µA	3.6V	ADC: ΔI_{ADC} **(Notes 3,4)**

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.