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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	MIPS32 ® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f512ht-50i-pt

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TABLE 5: PIN NAMES FOR 100-PIN USB DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MX230F128L PIC32MX530F128L PIC32MX250F256L PIC32MX550F256L PIC32MX270F512L PIC32MX570F512L

100

			1
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN28/RG15	36	Vss
2	Vdd	37	Vdd
3	AN22/RPE5/PMD5/RE5	38	TCK/CTED2/RA1
4	AN23/PMD6/RE6	39	AN34/RPF13/SCK3/RF13
5	AN27/PMD7/RE7	40	AN35/RPF12/RF12
6	AN29/RPC1/RC1	41	AN12/PMA11/RB12
7	AN30/RPC2/RC2	42	AN13/PMA10/RB13
8	AN31/RPC3/RC3	43	AN14/RPB14/CTED5/PMA1/RB14
9	RPC4/CTED7/RC4	44	AN15/RPB15/OCFB/CTED6/PMA0/RB15
10	AN16/C1IND/RPG6/SCK2/PMA5/RG6	45	Vss
11	AN17/C1INC/RPG7/PMA4/RG7	46	Vdd
12	AN18/C2IND/RPG8/PMA3/RG8	47	AN36/RPD14/RD14
13	MCLR	48	AN37/RPD15/SCK4/RD15
14	AN19/C2INC/RPG9/PMA2/RG9	49	RPF4/PMA9/RF4
15	Vss	50	RPF5/PMA8/RF5
16	Vdd	51	USBID/RPF3/RF3
17	TMS/CTED1/RA0	52	AN38/RPF2/RF2
18	AN32/RPE8/RE8	53	AN39/RPF8/RF8
19	AN33/RPE9/RE9	54	VBUS
20	AN5/C1INA/RPB5/VBUSON/RB5	55	VUSB3V3
21	AN4/C1INB/RB4	56	D-
22	PGED3/AN3/C2INA/RPB3/RB3	57	D+
23	PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2	58	SCL2/RA2
24	PGEC1/AN1/RPB1/CTED12/RB1	59	SDA2/RA3
25	PGED1/AN0/RPB0/RB0	60	TDI/CTED9/RA4
26	PGEC2/AN6/RPB6/RB6	61	TDO/RA5
27	PGED2/AN7/RPB7/CTED3/RB7	62	VDD
28	VREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVdd	65	Vss
31	AVss	66	RPA14/SCL1/RA14
32	AN8/RPB8/CTED10/RB8	67	RPA15/SDA1/RA15
33	AN9/RPB9/CTED4/RB9	68	RPD8/RTCC/RD8
34	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	69	RPD9/RD9
35	AN11/PMA12/RB11	70	RPD10/SCK1/PMA15/RD10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See Section 11.0 "I/O Ports" for more information.

3: Shaded pins are 5V tolerant.

Without proper signal isolation, on non-5V tolerant pins, the remote signal can power the PIC32 device through the high side ESD protection diodes. Besides violating the absolute maximum rating specification when VDD of the PIC32 device is restored and ramping up or ramping down, it can also negatively affect the internal Power-on Reset (POR) and Brown-out Reset (BOR) circuits, which can lead to improper initialization of internal PIC32 logic circuits. In these cases, it is recommended to implement digital or analog signal isolation as depicted in Figure 2-6, as appropriate. This is indicative of all industry microcontrollers and not just Microchip products.

TABLE 2-1: EXAMPLES OF DIGITAL/ ANALOG ISOLATORS WITH OPTIONAL LEVEL TRANSLATION

Example Digital/Analog Signal Isolation Circuits	Inductive Coupling	Capacitive Coupling	Opto Coupling	Analog/Digital Switch
ADuM7241 / 40 ARZ (1 Mbps)	Х			
ADuM7241 / 40 CRZ (25 Mbps)	Х			
ISO721		Х		
LTV-829S (2 Channel)			Х	
LTV-849S (4 Channel)			Х	
FSA266 / NC7WB66	_		_	Х

FIGURE 2-6: DIGITAL/ANALOG SIGNAL ISOLATION CIRCUITS





FIGURE 4-2: MEMORY MAP FOR DEVICES WITH 128 KB OF PROGRAM MEMORY + 16 KB RAM

documentation for information).



FIGURE 4-4: MEMORY MAP FOR DEVICES WITH 512 KB OF PROGRAM MEMORY + 64 KB RAM

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documentation for information).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	R/W-y	R/W-y	R/W-y	R/W-0	R/W-0	R/W-1
31.24	—	—	P	LLODIV<2:0	>	FRCDIV<2:0>		
22:16	U-0	R-0	R-1	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y
23.10	—	SOSCRDY	PBDIVRDY	BDIVRDY PBDIV<1:0>			LLMULT<2:0>	>
15.0	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
15.0	—		COSC<2:0>		—		NOSC<2:0>	
7:0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-y	R/W-0
7:0	CLKLOCK	ULOCK ⁽¹⁾	SLOCK	SLPEN	CF	UFRCEN ⁽¹⁾	SOSCEN	OSWEN

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

Legend:

bit 22

y = Value set from Configuration bits on POR

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

bit 29-27 **PLLODIV<2:0>:** Output Divider for PLL

- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 26-24 FRCDIV<2:0>: Internal Fast RC (FRC) Oscillator Clock Divider bits

- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2 (default setting)
- 000 = FRC divided by 1
- bit 23 Unimplemented: Read as '0'
 - SOSCRDY: Secondary Oscillator (SOSC) Ready Indicator bit
 - 1 = Indicates that the Secondary Oscillator is running and is stable
 - 0 = Secondary Oscillator is still warming up or is turned off
- bit 21 PBDIVRDY: Peripheral Bus Clock (PBCLK) Divisor Ready bit
 - 1 = PBDIV<1:0> bits can be written
 - 0 = PBDIV<1:0> bits cannot be written
- bit 20-19 **PBDIV<1:0>:** Peripheral Bus Clock (PBCLK) Divisor bits
 - 11 = PBCLK is SYSCLK divided by 8 (default)
 - 10 = PBCLK is SYSCLK divided by 4
 - 01 = PBCLK is SYSCLK divided by 2
 - 00 = PBCLK is SYSCLK divided by 1
- Note 1: This bit is available on PIC32MX2XX/5XX devices only.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 10-11: U1CON: USB CONTROL REGISTER (CONTINUED)

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit

- 1 = Reset all Even/Odd buffer pointers to the EVEN BD banks
- 0 = Even/Odd buffer pointers not being Reset
- bit 0 USBEN: USB Module Enable bit⁽⁴⁾
 - 1 = USB module and supporting circuitry enabled
 - 0 = USB module and supporting circuitry disabled

SOFEN: SOF Enable bit(5)

- 1 = SOF token sent every 1 ms
- 0 = SOF token disabled
- **Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).
 - 2: All host control logic is reset any time that the value of this bit is toggled.
 - 3: Software must set the RESUME bit for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.
 - 4: Device mode.
 - 5: Host mode.

11.1 Parallel I/O (PIO) Ports

All port pins have ten registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin, regardless of the output function including PPS remapped output functions to act as an open-drain output. The only exception is the l^2C pins that are open drain by default.

The open-drain feature allows the presence of outputs higher than V_{DD} (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

See the **"Device Pin Tables"** section for the available pins and their functionality.

11.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default. The ANSELx register bit, when cleared, disables the corresponding digital input buffer pin(s).

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module. The TRISx bits only control the corresponding digital output buffer pin(s).

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level; i.e., when ANSELx = 1; TRISx = x).

Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be an NOP.

11.1.4 INPUT CHANGE NOTIFICATION

The input Change Notification (CN) function of the I/O ports allows the PIC32MX1XX/2XX/5XX 64/100-pin devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Five control registers are associated with the CN functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit.

11.1.5 INTERNALLY SELECTABLE PULL-UPS AND PULL-DOWNS

Each I/O pin also has a weak pull-up and every I/O pin has a weak pull-down connected to it, which are independent of any other I/O pin functionality (i.e., PPS, Open Drain, or CN). The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note: Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output. They should also be disabled on 5V tolerant pins when the pin voltage can exceed VDD.

An additional control register (CNCONx) is shown in Register 11-3.

11.2 CLR, SET, and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

REGISTER 18-2: I2CxSTAT: I²C STATUS REGISTER (CONTINUED)

bit 4	P: Stop bit
	 1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last Hardware set or clear when Start, Repeated Start or Stop detected.
bit 3	S: Start bit
	 1 = Indicates that a Start (or Repeated Start) bit has been detected last 0 = Start bit was not detected last Hardware set or clear when Start, Repeated Start or Stop detected.
bit 2	R_W: Read/Write Information bit (when operating as I ² C slave)
	 1 = Read – indicates data transfer is output from slave 0 = Write – indicates data transfer is input to slave Hardware set or clear after reception of I²C device address byte.
bit 1	RBF: Receive Buffer Full Status bit
	 1 = Receive complete, I2CxRCV is full 0 = Receive not complete, I2CxRCV is empty Hardware set when I2CxRCV is written with received byte. Hardware clear when reads I2CxRCV.
bit 0	TBF: Transmit Buffer Full Status bit
	1 = Transmit in progress, I2CxTRN is full

0 = Transmit complete, I2CxTRN is empty

Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

software

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
23:16	R/W-0, HC	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
	RDSTART	—	—	—	—	—	DUALBUF	—
15.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	ON ⁽¹⁾	—	SIDL	ADRMU	JX<1:0>	PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
7:0	CSF<	1:0> (2)	ALP ⁽²⁾	CS2P ⁽²⁾	CS1P ⁽²⁾	—	WRSP	RDSP

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER

Legend:	HC = Hardware cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 Unimplemented: Read as '0'

- bit 23 RDSTART: Start a Read on the PMP Bus bit⁽³⁾
 - 1 = Start a read cycle on the PMP bus
 - 0 = No effect

This bit is cleared by hardware at the end of the read cycle when the BUSY bit (PMMODE<15>) = 0.

bit 22-18 Unimplemented: Read as '0'

bit 17 **DUALBUF:** Parallel Master Port Dual Read/Write Buffer Enable bit

- This bit is only valid in Master mode.
- PMP uses separate registers for reads and writes Reads: PMRADDR and PMRDIN Writes: PMRWADDR and PMDOUT
- 0 = PMP uses legacy registers for reads and writes Reads/Writes: PMADDR and PMRDIN
- bit 16 Unimplemented: Read as '0'
- bit 15 **ON:** Parallel Master Port Enable bit⁽¹⁾
 - 1 = PMP enabled
 - 0 = PMP disabled, no off-chip access performed
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit

bit 10

- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

bit 12-11 ADRMUX<1:0>: Address/Data Multiplexing Selection bits

- 11 = Lower 8 bits of address are multiplexed on PMD<15:0> pins
- 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
- 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>
- 00 = Address and data appear on separate pins
- PMPTTL: PMP Module TTL Input Buffer Select bit
 - 1 = PMP module uses TTL input buffers
 - 0 = PMP module uses Schmitt Trigger input buffer
- bit 9 PTWREN: Write Enable Strobe Port Enable bit
 - 1 = PMWR/PMENB port enabled
 - 0 = PMWR/PMENB port disabled
 - **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.
 - **2:** These bits have no effect when their corresponding pins are used as address lines.

REGISTE bit 7-0	ER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED) ARPT<7:0>: Alarm Repeat Counter Value bits ⁽³⁾ 11111111 = Alarm will trigger 256 times
Note 1:	Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0 .
2:	This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
3:	This assumes a CPU read will execute in less than 32 PBCLKs.
Note:	This register is reset only on a Power-on Reset (POR).

23.0 CONTROLLER AREA NETWORK (CAN)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 34. "Controller Area Network (CAN)" (DS60001154) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The Controller Area Network (CAN) module supports the following key features:

- · Standards Compliance:
 - Full CAN 2.0B compliance
 - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
 - 16 message FIFOs
 - Each FIFO can have up to 16 messages for a total of 256 messages

- FIFO can be a transmit message FIFO or a receive message FIFO
- User-defined priority levels for message FIFOs used for transmission
- 16 acceptance filters for message filtering
- Four acceptance filter mask registers for message filtering
- Automatic response to remote transmit request
- DeviceNet[™] addressing support
- Additional Features:
 - Loopback, Listen All Messages, and Listen Only modes for self-test, system diagnostics and bus monitoring
 - Low-power operating modes
 - CAN module is a bus master on the PIC32 system bus
 - Use of DMA is not required
 - Dedicated time-stamp timer
 - Dedicated DMA channels
- Data-only Message Reception mode

Figure 23-1 illustrates the general structure of the CAN module.

FIGURE 23-1: PIC32 CAN MODULE BLOCK DIAGRAM



REGISTER 23-2: C1CFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

- bit 10-8 **PRSEG<2:0>:** Propagation Time Segment bits⁽⁴⁾ 111 = Length is $8 \times TQ$ $000 = \text{Length is } 1 \times TQ$ SJW<1:0>: Synchronization Jump Width bits⁽³⁾ bit 7-6 11 = Length is $4 \times TQ$ $10 = \text{Length is } 3 \times TQ$ 01 = Length is 2 x TQ $00 = \text{Length is } 1 \times TQ$ bit 5-0 BRP<5:0>: Baud Rate Prescaler bits 111111 = Tq = (2 x 64)/SYSCLK 111110 = TQ = (2 x 63)/SYSCLK • 000001 = TQ = (2 x 2)/SYSCLK $000000 = TQ = (2 \times 1)/SYSCLK$ Note 1: SEG2PH \leq SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically. 2: 3 Time bit sampling is not allowed for BRP < 2.
 - **3:** SJW \leq SEG2PH.
 - **4:** The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = 100).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	FLTEN15	MSEL1	5<1:0>	FSEL15<4:0>				
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	FLTEN14	MSEL14<1:0>		FSEL14<4:0>				
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	FLTEN13	MSEL1	3<1:0>		F	SEL13<4:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	FLTEN12	MSEL1	2<1:0>		F	SEL12<4:0>		

REGISTER 23-13: C1FLTCON3: CAN FILTER CONTROL REGISTER 3

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	FLTEN15: Filter 15 Enable bit 1 = Filter is enabled
	0 = Filter is disabled
bit 30-29	MSEL15<1:0>: Filter 15 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 28-24	FSEL15<4:0>: FIFO Selection bits 11111 = Reserved 10000 = Reserved 01111 = Message matching filter is stored in FIFO buffer 15 00000 = Message matching filter is stored in FIFO buffer 0
bit 23	FLTEN14: Filter 14 Enable bit 1 = Filter is enabled 0 = Filter is disabled
bit 22-21	MSEL14<1:0>: Filter 14 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
Note:	The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
00.40	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
23:10	—	—	—	—	—	FPLLODIV<2:0>		
15:8	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	UPLLEN ⁽¹⁾	—	—	—	—	UPLLIDIV<2:0> ⁽¹⁾		
7:0	r-1	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P
	_	FPLLMUL<2:0>			_	FPLLIDIV<2:0>		

DEVCFG2: DEVICE CONFIGURATION WORD 2 REGISTER 28-3:

Legend:	r = Reserved bit	P = Programmable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-19 Reserved: Write '1'

bit 15

bit 7

bit 6-4

bit 18-16 FPLLODIV<2:0>: Default PLL Output Divisor bits

- 111 = PLL output divided by 256 110 = PLL output divided by 64 101 = PLL output divided by 32 100 = PLL output divided by 16 011 = PLL output divided by 8 010 = PLL output divided by 4 001 = PLL output divided by 2 000 = PLL output divided by 1 UPLLEN: USB PLL Enable bit⁽¹⁾ 1 = Disable and bypass USB PLL 0 = Enable USB PLL bit 14-11 Reserved: Write '1' bit 10-8 UPLLIDIV<2:0>: USB PLL Input Divider bits⁽¹⁾ 111 = 12x divider 110 = 10x divider 101 = 6x divider100 = 5x divider 011 = 4x divider 010 = 3x divider 010 = 3x divider 001 = 2x divider000 = 1x divider Reserved: Write '1' FPLLMUL<2:0>: PLL Multiplier bits 111 = 24x multiplier 110 = 21x multiplier
 - 101 = 20x multiplier
 - 100 = 19x multiplier
 - 011 = 18x multiplier
 - 010 = 17x multiplier
 - 001 = 16x multiplier 000 = 15x multiplier
- bit 3 Reserved: Write '1'

Note 1: This bit is available on PIC32MX2XX/5XX devices only.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	_	—	-	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	_	—	_	—
15:8	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	—	—	IOLOCK ⁽¹⁾	PMDLOCK ⁽¹⁾		—		_
7:0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	R/W-1
	_	_	_	_	JTAGEN	_	_	TDOEN

REGISTER 28-5: CFGCON: CONFIGURATION CONTROL REGISTER

Legend:

Logonan					
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-14 Unimplemented: Read as '0'

- bit 13 **IOLOCK:** Peripheral Pin Select Lock bit⁽¹⁾
 - 1 = Peripheral Pin Select is locked. Writes to PPS registers is not allowed
 - 0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed
- bit 12 PMDLOCK: Peripheral Module Disable bit⁽¹⁾
 - 1 = Peripheral module is locked. Writes to PMD registers is not allowed
 - 0 = Peripheral module is not locked. Writes to PMD registers is allowed
- bit 11-4 Unimplemented: Read as '0'
- bit 3 JTAGEN: JTAG Port Enable bit
 - 1 = Enable the JTAG port
 - 0 = Disable the JTAG port
- bit 2-1 Unimplemented: Read as '0'
- bit 0 TDOEN: TDO Enable for 2-Wire JTAG
 - 1 = 2-wire JTAG protocol uses TDO
 - 0 = 2-wire JTAG protocol does not use TDO
- Note 1: To change this bit, the unlock sequence must be performed. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.





TABLE 31-29: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +105^\circ C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time (Note 3)	Tsck/2	_		ns	—
SP11	TscH	SCKx Output High Time (Note 3)	Tsck/2	—	_	ns	—
SP20	TscF	SCKx Output Fall Time (Note 4)		—	_	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time (Note 4)		_		ns	See parameter DO31
SP30	TDOF	SDOx Data Output Fall Time (Note 4)		_		ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	_	—		ns	See parameter DO31
SP35 TscH2doV,		SDOx Data Output Valid after	—	—	15	ns	VDD > 2.7V
	TscL2doV	SCKx Edge		—	20	ns	VDD < 2.7V
SP36	TDOV2SC, TDOV2SCL	SDOx Data Output Setup to First SCKx Edge	15	_		ns	
SP40	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	15	—		ns	VDD > 2.7V
			20	—	_	ns	VDD < 2.7V
SP41	TscH2DIL,	Hold Time of SDIx Data Input to SCKx Edge	15	—	_	ns	VDD > 2.7V
	TscL2DIL		20	—	_	ns	VDD < 2.7V

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.



34.2 Package Details

The following sections give the technical details of the packages.

64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Chamfers at corners are optional; size may vary.

Overall Width

Overall Length

Lead Thickness

Lead Width

Molded Package Width

Mold Draft Angle Top

Mold Draft Angle Bottom

Molded Package Length

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

Е

D

E1

D1

с

b

α

β

0.09

0.17

11°

11°

- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B

0.20

0.27

13°

13

12.00 BSC

12.00 BSC

10.00 BSC

10.00 BSC

0.22

12°

12°

w

WWW Address	
WWW, On-Line Support	9

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