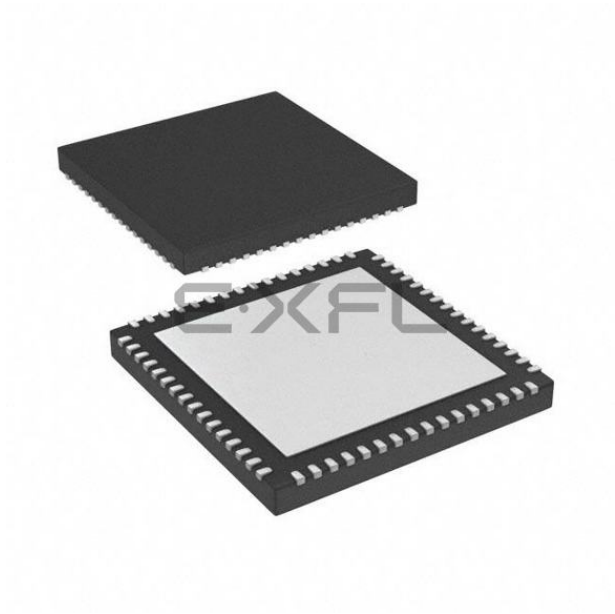
Microchip Technology - PIC32MX270F512HT-I/MR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f512ht-i-mr

TABLE 5: PIN NAMES FOR 100-PIN USB DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MX230F128L
PIC32MX530F128L
PIC32MX250F256L
PIC32MX550F256L
PIC32MX270F512L
PIC32MX570F512L

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN28/RG15	36	VSS
2	VDD	37	VDD
3	AN22/RPE5/PMD5/RE5	38	TCK/CTED2/RA1
4	AN23/PMD6/RE6	39	AN34/RPF13/SCK3/RF13
5	AN27/PMD7/RE7	40	AN35/RPF12/RF12
6	AN29/RPC1/RC1	41	AN12/PMA11/RB12
7	AN30/RPC2/RC2	42	AN13/PMA10/RB13
8	AN31/RPC3/RC3	43	AN14/RPB14/CTED5/PMA1/RB14
9	RPC4/CTED7/RC4	44	AN15/RPB15/OCFB/CTED6/PMA0/RB15
10	AN16/C1IND/RPG6/SCK2/PMA5/RG6	45	VSS
11	AN17/C1INC/RPG7/PMA4/RG7	46	VDD
12	AN18/C2IND/RPG8/PMA3/RG8	47	AN36/RPD14/RD14
13	$\overline{\text{MCLR}}$	48	AN37/RPD15/SCK4/RD15
14	AN19/C2INC/RPG9/PMA2/RG9	49	RPF4/PMA9/RF4
15	VSS	50	RPF5/PMA8/RF5
16	VDD	51	USBID/RPF3/RF3
17	TMS/CTED1/RA0	52	AN38/RPF2/RF2
18	AN32/RPE8/RE8	53	AN39/RPF8/RF8
19	AN33/RPE9/RE9	54	VBUS
20	AN5/C1INA/RPB5/VBUSON/RB5	55	VUSB3V3
21	AN4/C1INB/RB4	56	D-
22	PGED3/AN3/C2INA/RPB3/RB3	57	D+
23	PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2	58	SCL2/RA2
24	PGEC1/AN1/RPB1/CTED12/RB1	59	SDA2/RA3
25	PGED1/AN0/RPB0/RB0	60	TDI/CTED9/RA4
26	PGEC2/AN6/RPB6/RB6	61	TDO/RA5
27	PGED2/AN7/RPB7/CTED3/RB7	62	VDD
28	VREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	VSS
31	AVSS	66	RPA14/SCL1/RA14
32	AN8/RPB8/CTED10/RB8	67	RPA15/SDA1/RA15
33	AN9/RPB9/CTED4/RB9	68	RPD8/RTCC/RD8
34	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	69	RPD9/RD9
35	AN11/PMA12/RB11	70	RPD10/SCK1/PMA15/RD10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP			
AN36	—	47	I	Analog	Analog input channels.
AN37	—	48	I	Analog	
AN38	—	52	I	Analog	
AN39	—	53	I	Analog	
AN40	—	79	I	Analog	
AN41	—	80	I	Analog	
AN42	—	83	I	Analog	
AN43	—	84	I	Analog	
AN44	—	87	I	Analog	
AN45	—	88	I	Analog	
AN46	—	93	I	Analog	
AN47	—	94	I	Analog	
CLKI	39	63	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	40	64	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with the OSC2 pin function.
OSC1	39	63	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	40	64	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	47	73	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	48	74	O	—	32.768 kHz low-power oscillator crystal output.
IC1	PPS	PPS	I	ST	Capture Input 1-5
IC2	PPS	PPS	I	ST	
IC3	PPS	PPS	I	ST	
IC4	PPS	PPS	I	ST	
IC5	PPS	PPS	I	ST	
OC1	PPS	PPS	O	ST	Output Compare Output 1
OC2	PPS	PPS	O	ST	Output Compare Output 2
OC3	PPS	PPS	O	ST	Output Compare Output 3
OC4	PPS	PPS	O	ST	Output Compare Output 4
OC5	PPS	PPS	O	ST	Output Compare Output 5
OCFA	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	30	44	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

6.1 Control Registers

TABLE 6-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F400	NVMCON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	LVDSTAT	—	—	—	—	—	—	—	NVMOP<3:0>				0000
F410	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
F420	NVMADDR(1)	31:16	NVMADDR<31:0>																0000
		15:0																	0000
F430	NVMDATA	31:16	NVMDATA<31:0>																0000
		15:0																	0000
F440	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

7.0 RESETS

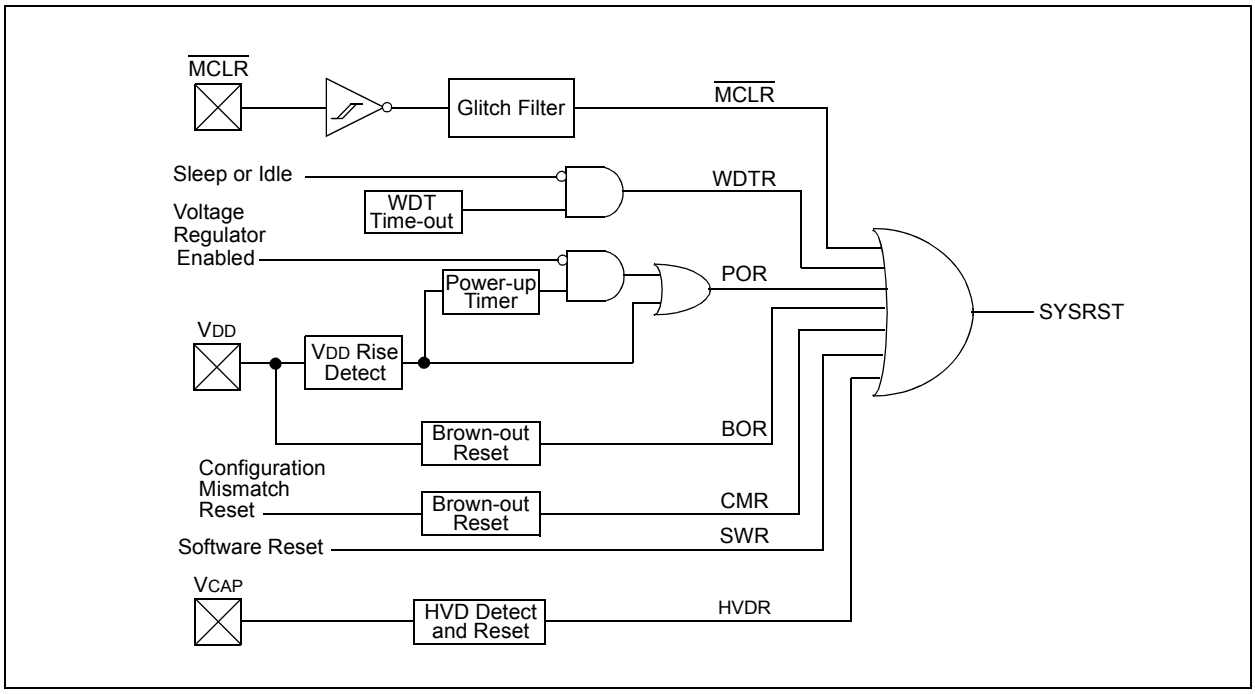
Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- $\overline{\text{MCLR}}$: Master Clear Reset pin
- SWR: Software Reset
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- CMR: Configuration Mismatch Reset
- HVDR: High Voltage Detect Reset

A simplified block diagram of the Reset module is illustrated in Figure 7-1.

FIGURE 7-1: SYSTEM RESET BLOCK DIAGRAM



NOTES:

TABLE 10-1: USB REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

REGISTER 10-6: U1IR: USB INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R-0	R/WC-0, HS
	STALLIF	ATTACHIF(1)	RESUMEIF(2)	IDLEIF	TRNIF(3)	SOFIF	UERRIF(4)	URSTIF(5) / DETACHIF(6)

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit
- 1 = In Host mode, a STALL handshake was received during the handshake phase of the transaction
  In Device mode, a STALL handshake was transmitted during the handshake phase of the transaction
- 0 = STALL handshake has not been sent

bit 6 **ATTACHIF:** Peripheral Attach Interrupt bit(1)
- 1 = Peripheral attachment was detected by the USB module
- 0 = Peripheral attachment was not detected

bit 5 **RESUMEIF:** Resume Interrupt bit(2)
- 1 = K-State is observed on the D+ or D- pin for 2.5 µs
- 0 = K-State is not observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
- 1 = Idle condition detected (constant Idle state of 3 ms or more)
- 0 = No Idle condition detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit(3)
- 1 = Processing of current token is complete; a read of the U1STAT register will provide endpoint information
- 0 = Processing of current token not complete

bit 2 **SOFIF:** SOF Token Interrupt bit
- 1 = SOF token received by the peripheral or the SOF threshold reached by the host
- 0 = SOF token was not received nor threshold reached

bit 1 **UERRIF:** USB Error Condition Interrupt bit(4)
- 1 = Unmasked error condition has occurred
- 0 = Unmasked error condition has not occurred

bit 0 **URSTIF:** USB Reset Interrupt bit (Device mode)(5)
- 1 = Valid USB Reset has occurred
- 0 = No USB Reset has occurred

bit 0 **DETACHIF:** USB Detach Interrupt bit (Host mode)(6)
- 1 = Peripheral detachment was detected by the USB module
- 0 = Peripheral detachment was not detected

Note 1: This bit is valid only if the HOSTEN bit is set (see Register 10-11), there is no activity on the USB for 2.5 µs, and the current bus state is not SE0.
2: When not in Suspend mode, this interrupt should be disabled.
3: Clearing this bit will cause the STAT FIFO to advance.
4: Only error conditions enabled through the U1EIE register will set this bit.
5: Device mode.
6: Host mode.

TABLE 11-2: OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD2	RPD2R	RPD2R<3:0>	0000 = No Connect 0001 = U3TX 0010 = U4RTS 0011 = Reserved 0100 = Reserved 0101 = Reserved 0110 = SDO2 0111 = Reserved 1000 = Reserved 1001 = Reserved 1010 = Reserved 1011 = OC3 1100 = C1TX(5) 1101 = C2OUT 1110 = SDO3 1111 = SDO4(3)
RPG8	RPG8R	RPG8R<3:0>	
RPF4	RPF4R	RPF4R<3:0>	
RPD10	RPD10R	RPD10R<3:0>	
RPF1	RPF1R	RPF1R<3:0>	
RPB9	RPB9R	RPB9R<3:0>	
RPB10	RPB10R	RPB10R<3:0>	
RPC14	RPC14R	RPC14R<3:0>	
RPB5(7)	RPB5R	RPB5R<3:0>	
RPC1(3)	RPC1R	RPC1R<3:0>	
RPD14(3)	RPD14R	RPD14R<3:0>	
RPG1(3)	RPG1R	RPG1R<3:0>	
RPA14(3)	RPA14R	RPA14R<3:0>	
RPD3	RPD3R	RPD3R<3:0>	0000 = No Connect 0001 = U2TX 0010 = Reserved 0011 = U1TX 0100 = U5RTS(3) 0101 = Reserved 0110 = SDO2 0111 = Reserved 1000 = SDO1 1001 = Reserved 1010 = Reserved 1011 = OC4 1100 = Reserved 1101 = C3OUT 1110 = SDO3 1111 = SDO4(3)
RPG7	RPG7R	RPG7R<3:0>	
RPF5	RPF5R	RPF5R<3:0>	
RPD11	RPD11R	RPD11R<3:0>	
RPF0	RPF0R	RPF0R<3:0>	
RPB1	RPB1R	RPB1R<3:0>	
RPE5	RPE5R	RPE5R<3:0>	
RPC13	RPC13R	RPC13R<3:0>	
RPB3	RPB3R	RPB3R<3:0>	
RPF3(4)	RPF3R	RPF3R<3:0>	
RPC4(3)	RPC4R	RPC4R<3:0>	
RPD15(3)	RPD15R	RPD15R<3:0>	
RPG0(3)	RPG0R	RPG0R<3:0>	
RPA15(3)	RPA15R	RPA15R<3:0>	

Note 1: This selection is not available on 64-pin USB devices.

2: This selection is only available on 100-pin General Purpose devices.

3: This selection is not available on 64-pin devices.

4: This selection is not available when USBID functionality is used on USB devices.

5: This selection is not available on devices without a CAN module.

6: This selection is not available on USB devices.

7: This selection is not available when VBUSON functionality is used on USB devices.

TABLE 11-7: PORTD REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSELD15	ANSELD14	ANSELD13	ANSELD12	—	—	—	—	ANSELD7	ANSELD6	—	—	ANSELD3	ANSELD2	ANSELD1	—	F0CE
6310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
5320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
6330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
6340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
6350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	CNPUD8	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
6360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	CNPDD8	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
6370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIED15	CNIED14	CNIED13	CNIED12	CNIED11	CNIED10	CNIED9	CNIED8	CNIED7	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	0000
6390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNS TATD15	CN STATD14	CN STATD13	CN STATD12	CN STATD11	CN STATD10	CN STATD9	CN STATD8	CN STATD7	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

TABLE 11-10: PORTE REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ANSELE7	ANSELE6	ANSELE5	ANSELE4	—	ANSELE2	—	—	03F4
6410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	00FF
6420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6440	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000
6450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPDE3	CNPUE2	CNPUE1	CNPUE0	0000
6460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPDE7	CNPDE6	CNPDE5	CNPDE4	CNPDE3	CNPDE2	CNPDE1	CNPDE0	0000
6470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNIEE7	CNIEE6	CNIEE5	CNIEE4	CNIEE3	CNIEE2	CNIEE1	CNIEE0	0000
6490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CN STATE7	CN STATE6	CN STATE5	CN STATE4	CN STATE3	CN STATE2	CN STATE1	CN STATE0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

TABLE 14-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	WDTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	SWDTPS<4:0>					WDTWINEN	WDTCLR	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 21-6: ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<1:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-20 **MONTH10<3:0>:** Binary Coded Decimal value of months bits, 10s place digits; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary Coded Decimal value of days bits, 10s place digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1s place digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary Coded Decimal value of weekdays bits, 1s place digit; contains a value from 0 to 6

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 4 **CLRASAM:** Stop Conversion Sequence bit (when the first ADC interrupt is generated)
1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
0 = Normal operation, buffer contents will be overwritten by the next conversion sequence

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** ADC Sample Auto-Start bit
1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set.
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit(2)
1 = The ADC sample and hold amplifier is sampling
0 = The ADC sample/hold amplifier is holding
When ASAM = 0, writing '1' to this bit starts sampling.
When SSRC = 000, writing '0' to this bit will end sampling and start conversion.

bit 0 **DONE:** Analog-to-Digital Conversion Status bit(3)
1 = Analog-to-digital conversion is done
0 = Analog-to-digital conversion is not done or has not started
Clearing this bit will not affect any operation in progress.

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ 0, this bit is automatically cleared by hardware to end sampling and start conversion.

3: This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

23.1 Control Registers

TABLE 23-1: CAN1 REGISTER SUMMARY

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B000	C1CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>					0000
B010	C1CFG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	SEG2PH<2:0>			0000
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>		BRP<5:0>						0000
B020	C1INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000
B030	C1VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
B040	C1TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000
B050	C1FSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000
B060	C1RXOVF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
B070	C1TMR	31:16	CANTS<15:0>																0000
		15:0	CANTSPRE<15:0>																0000
B080	C1RXM0	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
B090	C1RXM1	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
B0A0	C1RXM2	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
B0B0	C1RXM3	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
B0C0	C1FLTCON0	31:16	FLTEN3	MSEL3<1:0>		FSEL3<4:0>					FLTEN2	MSEL2<1:0>		FSEL2<4:0>					0000
		15:0	FLTEN1	MSEL1<1:0>		FSEL1<4:0>					FLTEN0	MSEL0<1:0>		FSEL0<4:0>					0000
B0D0	C1FLTCON1	31:16	FLTEN7	MSEL7<1:0>		FSEL7<4:0>					FLTEN6	MSEL6<1:0>		FSEL6<4:0>					0000
		15:0	FLTEN5	MSEL5<1:0>		FSEL5<4:0>					FLTEN4	MSEL4<1:0>		FSEL4<4:0>					0000
B0E0	C1FLTCON2	31:16	FLTEN11	MSEL11<1:0>		FSEL11<4:0>					FLTEN10	MSEL10<1:0>		FSEL10<4:0>					0000
		15:0	FLTEN9	MSEL9<1:0>		FSEL9<4:0>					FLTEN8	MSEL8<1:0>		FSEL8<4:0>					0000
B0F0	C1FLTCON3	31:16	FLTEN15	MSEL15<1:0>		FSEL15<4:0>					FLTEN14	MSEL14<1:0>		FSEL14<4:0>					0000
		15:0	FLTEN13	MSEL13<1:0>		FSEL13<4:0>					FLTEN12	MSEL12<1:0>		FSEL12<4:0>					0000
B140	C1RXFn (n = 0-15)	31:16	SID<10:0>											-—	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 23-18: C1FIFOUAn: CAN FIFO USER ADDRESS REGISTER 'n' ('n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	C1FIFOUAn<31:24>							
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	C1FIFOUAn<23:16>							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	C1FIFOUAn<15:8>							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-0(1)	R-0(1)
	C1FIFOUAn<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **C1FIFOUAn<31:0>:** CAN FIFO User Address bits

TXEN = 1: (FIFO configured as a transmit buffer)

A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0: (FIFO configured as a receive buffer)

A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This bit will always read '0', which forces byte-alignment of messages.

Note: This register is not guaranteed to read correctly in Configuration mode, and should only be accessed when the module is not in Configuration mode.

REGISTER 23-19: C1FIFOCIn: CAN MODULE MESSAGE INDEX REGISTER 'n' ('n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	C1FIFOCIn<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-5 **Unimplemented:** Read as '0'

bit 4-0 **C1FIFOCIn<4:0>:** CAN Side FIFO Message Index bits

TXEN = 1: (FIFO configured as a transmit buffer)

A read of this register will return an index to the message that the FIFO will next attempt to transmit.

TXEN = 0: (FIFO configured as a receive buffer)

A read of this register will return an index to the message that the FIFO will use to save the next message.

25.1 Control Registers

TABLE 25-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9800	CVRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	CVROE	CVRR	CVRSS	CVR<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

30.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

30.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 31-10: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.(1)**	**Typical**	**Max.**	**Units**	**Conditions**
BO10	VBOR	BOR Event on VDD transition high-to-low(2)	2.0	—	2.3	V	—

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.

TABLE 31-11: ELECTRICAL CHARACTERISTICS: HVD

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.(1)	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
HV10	VHVD	High Voltage Detect on VCAP pin	—	2.5	—	V	—

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

31.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX/5XX 64/100-pin AC characteristics and timing parameters.

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

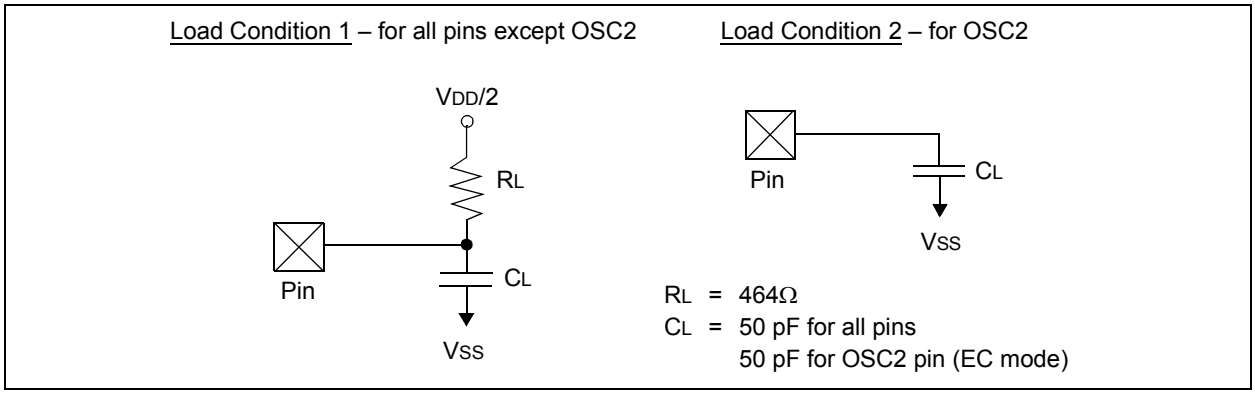
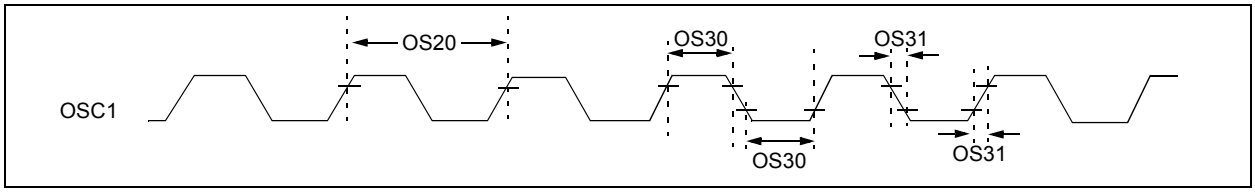


TABLE 31-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DO50	COSCO	OSC2 pin	—	—	15	pF	In XT and HS modes when an external crystal is used to drive OSC1
DO50a	CSOSC	SOSCI/SOSCO pins	—	33	—	pF	Epson P/N: MC-306 32.7680K-A0:ROHS
DO56	CIO	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C mode

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 31-2: EXTERNAL CLOCK TIMING



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