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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f512ht-v-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f512ht-v-pt</a>

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**TABLE 3: PIN NAMES FOR 64-PIN USB DEVICES**

64-PIN QFN <sup>(4)</sup> AND TQFP (TOP VIEW)			
<b>PIC32MX230F128H</b> <b>PIC32MX530F128H</b> <b>PIC32MX250F256H</b> <b>PIC32MX550F256H</b> <b>PIC32MX270F512H</b> <b>PIC32MX570F512H</b>		64	1
		QFN <sup>(4)</sup>	TQFP <sup>1</sup>
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN22/RPE5/PMD5/RE5	33	USBID/RPF3/RF3
2	AN23/PMD6/RE6	34	VBUS
3	AN27/PMD7/RE7	35	VUSB3V3
4	AN16/C1IND/RPG6/SCK2/PMA5/RG6	36	D-
5	AN17/C1INC/RPG7/PMA4/RG7	37	D+
6	AN18/C2IND/RPG8/PMA3/RG8	38	VDD
7	MCLR	39	OSC1/CLKI/RC12
8	AN19/C2INC/RPG9/PMA2/RG9	40	OSC2/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	RPD8/RTCC/RD8
11	AN5/C1INA/RPB5/VBUSON/RB5	43	RPD9/SDA1/RD9
12	AN4/C1INB/RB4	44	RPD10/SCL1/PMA15/RD10
13	PGED3/AN3/C2INA/RPB3/RB3	45	RPD11/PMA14/RD11
14	PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2	46	RPD0/INT0/RD0
15	PGEC1/VREF-/AN1/RPB1/CTED12/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN6/RPB6/RB6	49	AN24/RPD1/RD1
18	PGED2/AN7/RPB7/CTED3/RB7	50	AN25/RPD2/SCK1/RD2
19	AVDD	51	AN26/C3IND/RPD3/RD3
20	AVSS	52	RPD4/PMWR/RD4
21	AN8/RPB8/CTED10/RB8	53	RPD5/PMRD/RD5
22	AN9/RPB9/CTED4/PMA7/RB9	54	C3INC/RD6
23	TMS/CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	55	C3INB/RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	VSS	57	VDD
26	VDD	58	C3INA/RPF0/RF0
27	TCK/AN12/PMA11/RB12	59	RPF1/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/RPB14/SCK3/CTED5/PMA1/RB14	61	PMD1/RE1
30	AN15/RPB15/OCFB/CTED6/PMA0/RB15	62	AN20/PMD2/RE2
31	RPF4/SDA2/PMA9/RF4	63	RPE3/CTPLS/PMD3/RE3
32	RPF5/SCL2/PMA8/RF5	64	AN21/PMD4/RE4

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
  - 2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 11.0 “I/O Ports”** for more information.
  - 3: Shaded pins are 5V tolerant.
  - 4: The metal plane at the bottom of the QFN device is not connected to any pins and is recommended to be connected to VSS externally.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**TABLE 4: PIN NAMES FOR 100-PIN GENERAL PURPOSE DEVICES (CONTINUED)**

<b>100-PIN TQFP (TOP VIEW)</b>  <b>PIC32MX130F128L</b> <b>PIC32MX150F256L</b> <b>PIC32MX170F512L</b>			
		100	1
Pin #	Full Pin Name	Pin #	Full Pin Name
71	RPD11/PMA14/RD11	86	VDD
72	RPD0/RD0	87	AN44/C3INA/RPF0/PMD11/RF0
73	SOSCI/RPC13/RC13	88	AN45/RPF1/PMD10/RF1
74	SOSCO/RPC14/T1CK/RC14	89	RPG1/PMD9/RG1
75	VSS	90	RPG0/PMD8/RG0
76	AN24/RPD1/RD1	91	RA6
77	AN25/RPD2/RD2	92	CTED8/RA7
78	AN26/C3IND/RPD3/RD3	93	AN46/PMD0/RE0
79	AN40/RPD12/PMD12/RD12	94	AN47/PMD1/RE1
80	AN41/PMD13/RD13	95	RG14
81	RPD4/PMWR/RD4	96	RG12
82	RPD5/PMRD/RD5	97	RG13
83	AN42/C3INC/PMD14/RD6	98	AN20/PMD2/RE2
84	AN43/C3INB/PMD15/RD7	99	RPE3/CTPLS/PMD3/RE3
85	VCAP	100	AN21/PMD4/RE4

- Note** 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
- 2: Every I/O port pin (RAX-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- 3: Shaded pins are 5V tolerant.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
Interrupt Controller	0xBF88	0x1000
Bus Matrix		0x2000
DMA		0x3000
USB		0x5000
PORTA-PORTG		0x6000
CAN1		0xB000
Watchdog Timer	0xBF80	0x0000
RTCC		0x0200
Timer1-Timer5		0x0600
IC1-IC5		0x2000
OC1-OC5		0x3000
I2C1-I2C2		0x5000
SPI1-SPI4		0x5800
UART1-UART5		0x6000
PMP		0x7000
ADC1		0x9000
DAC		0x9800
Comparator 1, 2, 3		0xA000
Oscillator		0xF000
Device and Revision ID		0xF200
Flash Controller		0xF400
PPS		0xFA00
Configuration	0xBFC0	0x0BF0

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**REGISTER 8-4: REFOTRIM: REFERENCE OSCILLATOR TRIM REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ROTRIM<8:1>							
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ROTRIM<0>	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

**Legend:**

R = Readable bit

-n = Value at POR

y = Value set from Configuration bits on POR

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-23 **ROTRIM<8:0>**: Reference Oscillator Trim bits

111111111 = 511/512 divisor added to RODIV value

111111110 = 510/512 divisor added to RODIV value

•

•

•

100000000 = 256/512 divisor added to RODIV value

•

•

•

000000010 = 2/512 divisor added to RODIV value

000000001 = 1/512 divisor added to RODIV value

000000000 = 0/512 divisor added to RODIV value

bit 22-0 **Unimplemented**: Read as '0'

**Note:** While the ON bit (REFOCON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

**TABLE 9-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP (CONTINUED)**

Virtual Address (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	Bits															All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0	
3280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>															0000		
3290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHPDAT<7:0>										0000
32A0	DCH3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000	
32B0	DCH3ECON	31:16	—	—	—	—	—	—	—	CHAIRQ<7:0>										00FF
		15:0	CHSIRQ<7:0>							CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FFF8		
32C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000	
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000	
32D0	DCH3SSA	31:16	CHSSA<31:0>															0000		
		15:0																0000		
32E0	DCH3DSA	31:16	CHDSA<31:0>															0000		
		15:0																0000		
32F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSSIZ<15:0>															0000		
3300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>															0000		
3310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>															0000		
3320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>															0000		
3330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>															0000		
3340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>															0000		
3350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>									

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET, and INV Registers” for more information.

**TABLE 10-1: USB REGISTER MAP (CONTINUED)**

Virtual Address (BF88_#)	Register Name <sup>(f)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.
- 2: This register does not have associated SET and INV registers.
- 3: This register does not have associated CLR, SET and INV registers.
- 4: Reset value for this bit is undefined.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## 11.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only options.

Peripheral pin select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The peripheral pin select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. Peripheral pin select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

### 11.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the peripheral pin select feature include the designation “RPn” in their full pin designation, where “RP” designates a remappable peripheral and “n” is the remappable port number.

### 11.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the peripheral pin select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the peripheral pin select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I<sup>2</sup>C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

### 11.3.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral pin select features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

### 11.3.4 INPUT MAPPING

The inputs of the peripheral pin select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [pin name]R registers, where [pin name] refers to the peripheral pins listed in Table 11-1, are used to configure peripheral input mapping (see Register 11-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 11-1.

For example, Figure 11-2 illustrates the remappable pin selection for the U1RX input.

**FIGURE 11-2: REMAPPABLE INPUT EXAMPLE FOR U1RX**

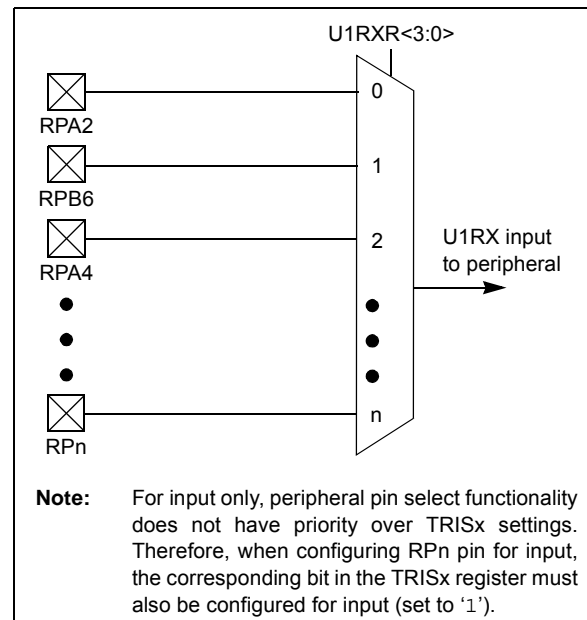




TABLE 14-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	WDTCN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	SWDTPS<4:0>					WDTWINEN	WDTCLR	0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 17 **SPIFE**: Frame Sync Pulse Edge Select bit (Framed SPI mode only)  
1 = Frame synchronization pulse coincides with the first bit clock  
0 = Frame synchronization pulse precedes the first bit clock
- bit 16 **ENHBUF**: Enhanced Buffer Enable bit<sup>(2)</sup>  
1 = Enhanced Buffer mode is enabled  
0 = Enhanced Buffer mode is disabled
- bit 15 **ON**: SPI Peripheral On bit<sup>(1)</sup>  
1 = SPI Peripheral is enabled  
0 = SPI Peripheral is disabled
- bit 14 **Unimplemented**: Read as '0'
- bit 13 **SIDL**: Stop in Idle Mode bit  
1 = Discontinue operation when CPU enters in Idle mode  
0 = Continue operation in Idle mode
- bit 12 **DISSDO**: Disable SDOx pin bit  
1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register  
0 = SDOx pin is controlled by the module
- bit 11-10 **MODE<32,16>**: 32/16-Bit Communication Select bits  
When AUDEN = 1:  
MODE32 MODE16 Communication  
11 24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame  
10 32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame  
01 16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame  
00 16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame  
  
When AUDEN = 0:  
MODE32 MODE16 Communication  
1x 32-bit  
01 16-bit  
00 8-bit
- bit 9 **SMP**: SPI Data Input Sample Phase bit  
Master mode (MSTEN = 1):  
1 = Input data sampled at end of data output time  
0 = Input data sampled at middle of data output time  
Slave mode (MSTEN = 0):  
SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.
- bit 8 **CKE**: SPI Clock Edge Select bit<sup>(3)</sup>  
1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)  
0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)
- bit 7 **SSEN**: Slave Select Enable (Slave mode) bit  
1 = SSx pin used for Slave mode  
0 = SSx pin not used for Slave mode, pin controlled by port function.
- bit 6 **CKP**: Clock Polarity Select bit<sup>(4)</sup>  
1 = Idle state for clock is a high level; active state is a low level  
0 = Idle state for clock is a low level; active state is a high level
- bit 5 **MSTEN**: Master Mode Enable bit  
1 = Master mode  
0 = Slave mode

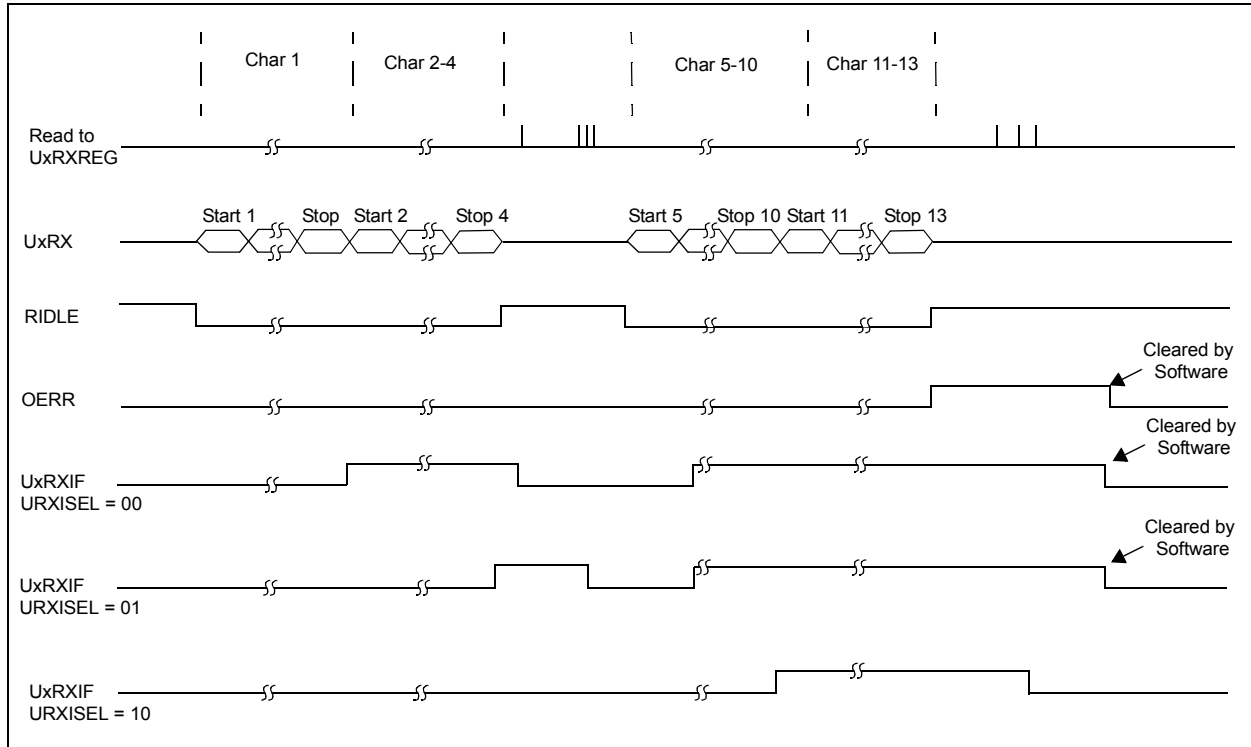
- Note 1:** When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSClk cycle immediately following the instruction that clears the module's ON bit.
- 2:** This bit can only be written when the ON bit = 0.
- 3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
- 4:** When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

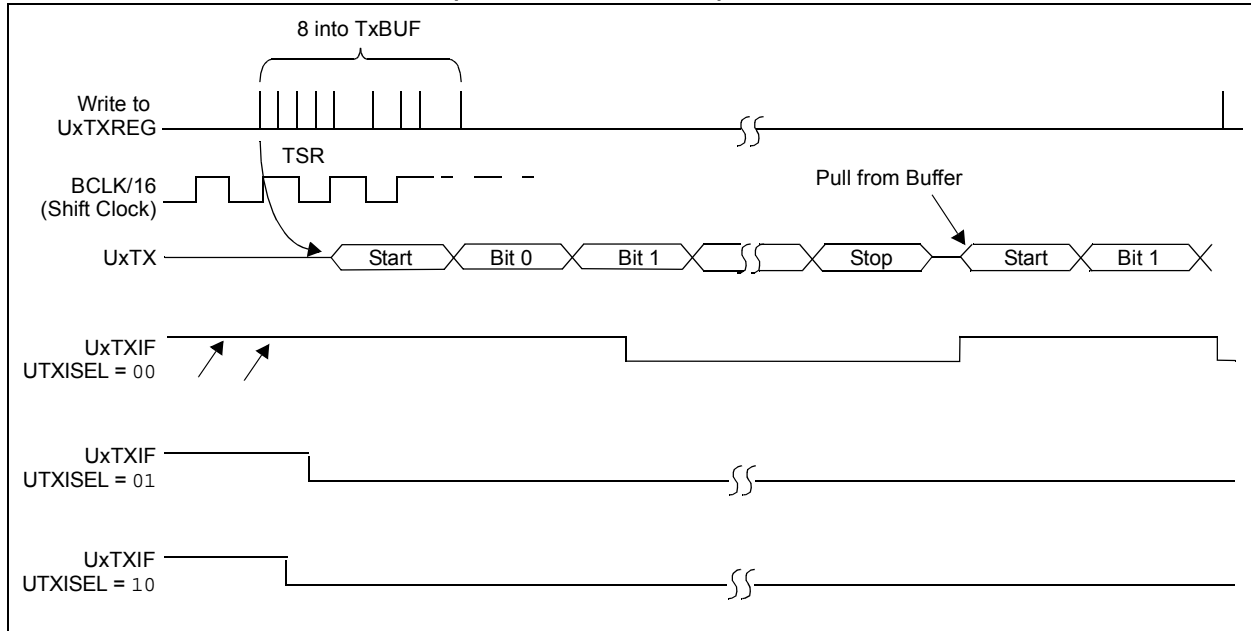
## 19.2 Timing Diagrams

Figure 19-2 and Figure 19-3 illustrate typical receive and transmit timing for the UART module.

**FIGURE 19-2: UART RECEPTION**



**FIGURE 19-3: TRANSMISSION (8-BIT OR 9-BIT DATA)**



# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**REGISTER 21-3: RTCTIME: RTC TIME VALUE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **HR10<3:0>**: Binary-Coded Decimal Value of Hours bits, 10s place digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>**: Binary-Coded Decimal Value of Hours bits, 1s place digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>**: Binary-Coded Decimal Value of Minutes bits, 10s place digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>**: Binary-Coded Decimal Value of Minutes bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>**: Binary-Coded Decimal Value of Seconds bits, 10s place digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>**: Binary-Coded Decimal Value of Seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 **Unimplemented**: Read as '0'

**Note:** This register is only writable when RTCWREN = 1 (RTCCON<3>).

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**REGISTER 23-2: C1CFG: CAN BAUD RATE CONFIGURATION REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	WAKFIL	—	—	—	SEG2PH<2:0> <sup>(1,4)</sup>		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEG2PHTS <sup>(1)</sup>	SAM <sup>(2)</sup>	SEG1PH<2:0>			PRSEG<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SJW<1:0> <sup>(3)</sup>		BRP<5:0>					

**Legend:**

R = Readable bit

-n = Value at POR

HC = Hardware Clear

W = Writable bit

'1' = Bit is set

S = Settable bit

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit

1 = Use CAN bus line filter for wake-up

0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as '0'

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits<sup>(1,4)</sup>

111 = Length is 8 x Tq

•  
•  
•

000 = Length is 1 x Tq

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit<sup>(1)</sup>

1 = Freely programmable

0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit<sup>(2)</sup>

1 = Bus line is sampled three times at the sample point

0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits<sup>(4)</sup>

111 = Length is 8 x Tq

•  
•  
•

000 = Length is 1 x Tq

**Note 1:**  $SEG2PH \leq SEG1PH$ . If SEG2PHTS is clear, SEG2PH will be set automatically.

**2:** 3 Time bit sampling is not allowed for BRP < 2.

**3:**  $SJW \leq SEG2PH$ .

**4:** The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C1CON<23:21>) = 100).

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**REGISTER 23-5: C1TREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 31-22 **Unimplemented:** Read as '0'
- bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT ≥ 256)
- bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT ≥ 128)
- bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT ≥ 128)
- bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)
- bit 17 **RXWARN:** Receiver in Error State Warning (128 > RERRCNT ≥ 96)
- bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning
- bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter
- bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

**REGISTER 23-6: C1FSTAT: CAN FIFO STATUS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 31-16 **Unimplemented:** Read as '0'
- bit 15-0 **FIFOIP<15:0>:** FIFOx Interrupt Pending bits  
 1 = One or more enabled FIFO interrupts are pending  
 0 = No FIFO interrupts are pending

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## REGISTER 23-7: C1RXOVF: CAN RECEIVE FIFO OVERFLOW STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RXOVF<15:0>:** FIFOx Receive Overflow Interrupt Pending bit

1 = FIFO has overflowed

0 = FIFO has not overflowed

## REGISTER 23-8: C1TMR: CAN TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<7:0>							

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 31-0 **CANTS<15:0>:** CAN Time Stamp Timer bits

This is a free-running timer that increments every CANTSPRE system clocks when the CANCAP bit (C1CON<20>) is set.

bit 15-0 **CANTSPRE<15:0>:** CAN Time Stamp Timer Prescaler bits

1111 1111 1111 1111 = CAN time stamp timer (CANTS) increments every 65,535 system clocks

.

.

0000 0000 0000 0000 = CAN time stamp timer (CANTS) increments every system clock

**Note 1:** C1TMR will be paused when CANCAP = 0.

**2:** The C1TMR prescaler count will be reset on any write to C1TMR (CANTSPRE will be unaffected).

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

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## REGISTER 28-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

- bit 15-14 **FCKSM<1:0>**: Clock Switching and Monitor Selection Configuration bits  
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled  
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled  
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
- bit 13-12 **FPBDIV<1:0>**: Peripheral Bus Clock Divisor Default Value bits  
11 = PBCLK is SYSCLK divided by 8  
10 = PBCLK is SYSCLK divided by 4  
01 = PBCLK is SYSCLK divided by 2  
00 = PBCLK is SYSCLK divided by 1
- bit 11 **Reserved**: Write '1'
- bit 10 **OSCIOFNC**: CLKO Enable Configuration bit  
1 = CLKO output disabled  
0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)
- bit 9-8 **POSCMOD<1:0>**: Primary Oscillator Configuration bits  
11 = Primary Oscillator disabled  
10 = HS Oscillator mode selected  
01 = XT Oscillator mode selected  
00 = External Clock mode selected
- bit 7 **IESO**: Internal External Switchover bit  
1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)  
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)
- bit 6 **Reserved**: Write '1'
- bit 5 **FSOSCEN**: Secondary Oscillator Enable bit  
1 = Enable Secondary Oscillator  
0 = Disable Secondary Oscillator
- bit 4-3 **Reserved**: Write '1'
- bit 2-0 **FNOSC<2:0>**: Oscillator Selection bits  
111 = Fast RC Oscillator with divide-by-N (FRCDIV)  
110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler  
101 = Low-Power RC Oscillator (LPRC)  
100 = Secondary Oscillator (Sosc)  
011 = Primary Oscillator (Posc) with PLL module (XT+PLL, HS+PLL, EC+PLL)  
010 = Primary Oscillator (XT, HS, EC)<sup>(1)</sup>  
001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)  
000 = Fast RC Oscillator (FRC)

**Note 1:** Do not disable the Posc (POSCMOD = 11) when using this oscillator source.



# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**REGISTER 28-3: DEVCFG2: DEVICE CONFIGURATION WORD 2**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
23:16	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	R/P FPLLODIV<2:0>	R/P	R/P
15:8	R/P UPLLEN <sup>(1)</sup>	r-1 —	r-1 —	r-1 —	r-1 —	R/P UPLLDIV<2:0> <sup>(1)</sup>	R/P	R/P
7:0	r-1 —	R/P-1 FPLLMUL<2:0>	R/P	R/P-1	r-1 —	R/P FPLLDIV<2:0>	R/P	R/P

<b>Legend:</b>	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLLODIV<2:0>:** Default PLL Output Divisor bits

111 = PLL output divided by 256  
110 = PLL output divided by 64  
101 = PLL output divided by 32  
100 = PLL output divided by 16  
011 = PLL output divided by 8  
010 = PLL output divided by 4  
001 = PLL output divided by 2  
000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit<sup>(1)</sup>  
1 = Disable and bypass USB PLL  
0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLLDIV<2:0>:** USB PLL Input Divider bits<sup>(1)</sup>

111 = 12x divider  
110 = 10x divider  
101 = 6x divider  
100 = 5x divider  
011 = 4x divider  
010 = 3x divider  
010 = 3x divider  
001 = 2x divider  
000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits

111 = 24x multiplier  
110 = 21x multiplier  
101 = 20x multiplier  
100 = 19x multiplier  
011 = 18x multiplier  
010 = 17x multiplier  
001 = 16x multiplier  
000 = 15x multiplier

bit 3 **Reserved:** Write '1'

**Note 1:** This bit is available on PIC32MX2XX/5XX devices only.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**REGISTER 28-4: DEVCFG3: DEVICE CONFIGURATION WORD 3**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	U-0	U-0	U-0	U-0
	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

<b>Legend:</b>	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

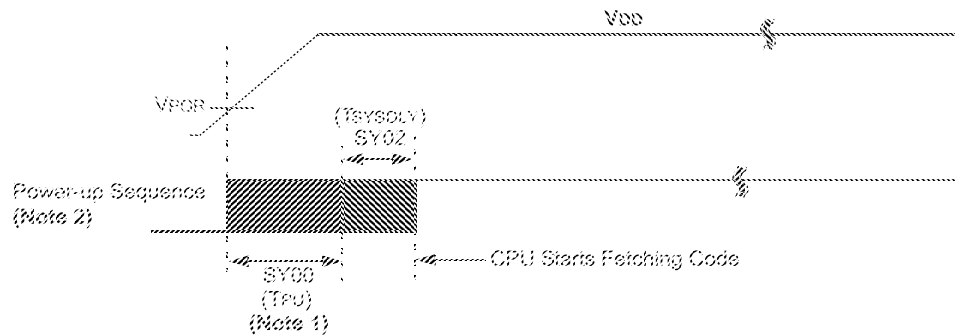
- bit 31    **FVBUSONIO:** USB VBUS\_ON Selection bit  
1 = VBUSON pin is controlled by the USB module  
0 = VBUSON pin is controlled by the port function
- bit 30    **FUSBIDIO:** USB USBID Selection bit  
1 = USBID pin is controlled by the USB module  
0 = USBID pin is controlled by the port function
- bit 29    **IOL1WAY:** Peripheral Pin Select Configuration bit  
1 = Allow only one reconfiguration  
0 = Allow multiple reconfigurations
- bit 28    **PMDL1WAY:** Peripheral Module Disable Configuration bit  
1 = Allow only one reconfiguration  
0 = Allow multiple reconfigurations
- bit 27-16 **Unimplemented:** Read as '0'
- bit 15-0    **USERID<15:0>:** This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**FIGURE 31-4: POWER-ON RESET TIMING CHARACTERISTICS**

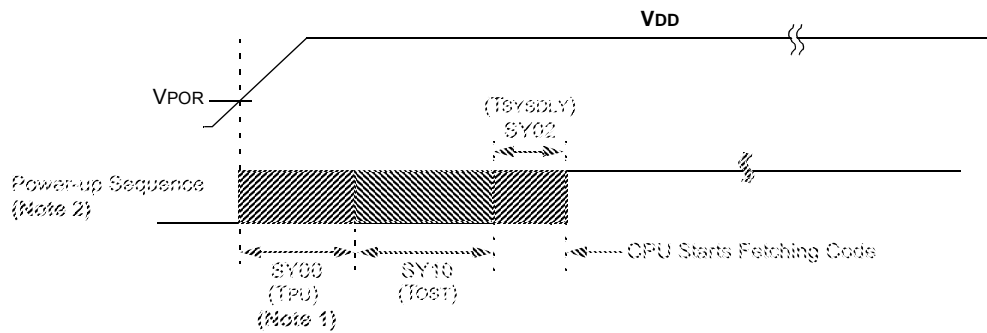
*Internal Voltage Regulator Enabled*

*Clock Sources = {FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC}*



*Internal Voltage Regulator Enabled*

*Clock Sources = {HS, HSPLL, XT, XTPLL and Sosc}*

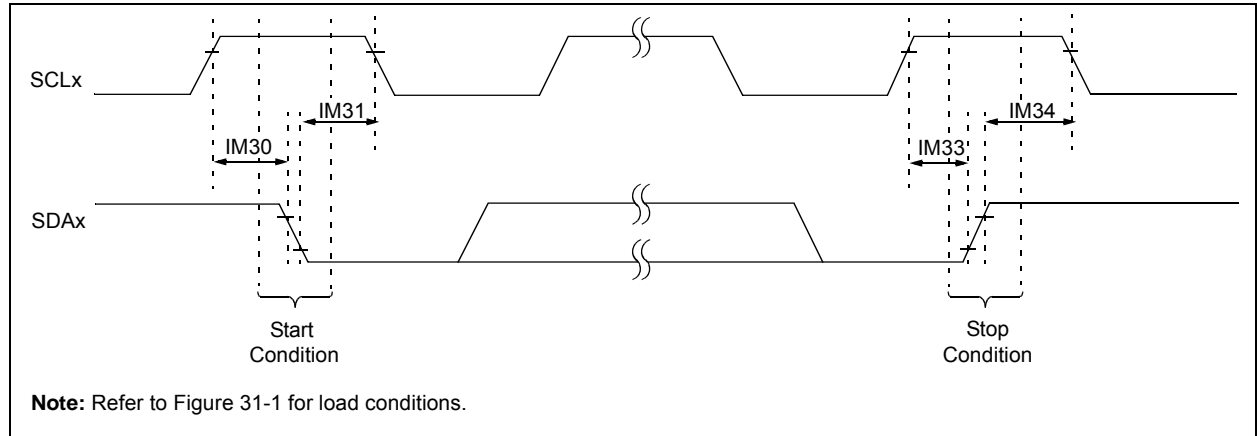


**Note 1:** The power-up period will be extended if the power-up sequence completes before the device exits from BOR ( $VDD < VDDMIN$ ).

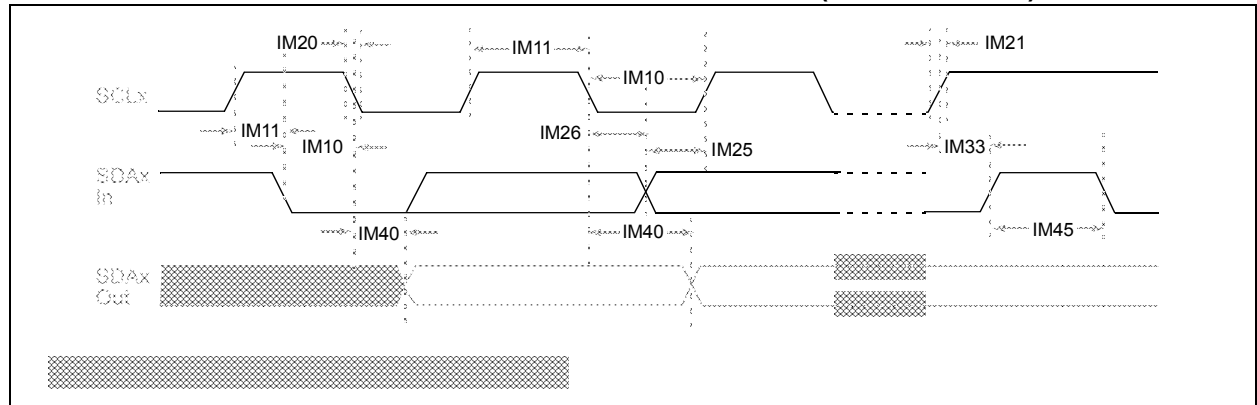
**2:** Includes interval voltage regulator stabilization delay.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**FIGURE 31-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**



**FIGURE 31-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**



# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

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