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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx270f512l-v-pt

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TABLE 3: **PIN NAMES FOR 64-PIN USB DEVICES**

64-PIN QFN⁽⁴⁾ AND TQFP (TOP VIEW)

PIC32MX230F128H PIC32MX530F128H PIC32MX250F256H PIC32MX550F256H PIC32MX270F512H PIC32MX570F512H

		QFN ⁽⁴) TQFP
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN22/RPE5/PMD5/RE5	33	USBID/RPF3/RF3
2	AN23/PMD6/RE6	34	VBUS
3	AN27/PMD7/RE7	35	VUSB3V3
4	AN16/C1IND/RPG6/SCK2/PMA5/RG6	36	D-
5	AN17/C1INC/RPG7/PMA4/RG7	37	D+
6	AN18/C2IND/RPG8/PMA3/RG8	38	Vdd
7	MCLR	39	OSC1/CLKI/RC12
8	AN19/C2INC/RPG9/PMA2/RG9	40	OSC2/CLKO/RC15
9	Vss	41	Vss
10	Vdd	42	RPD8/RTCC/RD8
11	AN5/C1INA/RPB5/VBUSON/RB5	43	RPD9/SDA1/RD9
12	AN4/C1INB/RB4	44	RPD10/SCL1/PMA15/RD10
13	PGED3/AN3/C2INA/RPB3/RB3	45	RPD11/PMA14/RD11
14	PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2	46	RPD0/INT0/RD0
15	PGEC1/VREF-/AN1/RPB1/CTED12/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN6/RPB6/RB6	49	AN24/RPD1/RD1
18	PGED2/AN7/RPB7/CTED3/RB7	50	AN25/RPD2/SCK1/RD2
19	AVDD	51	AN26/C3IND/RPD3/RD3
20	AVss	52	RPD4/PMWR/RD4
21	AN8/RPB8/CTED10/RB8	53	RPD5/PMRD/RD5
22	AN9/RPB9/CTED4/PMA7/RB9	54	C3INC/RD6
23	TMS/CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	55	C3INB/RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	Vss	57	Vdd
26	VDD	58	C3INA/RPF0/RF0
27	TCK/AN12/PMA11/RB12	59	RPF1/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/RPB14/SCK3/CTED5/PMA1/RB14	61	PMD1/RE1
30	AN15/RPB15/OCFB/CTED6/PMA0/RB15	62	AN20/PMD2/RE2
31	RPF4/SDA2/PMA9/RF4	63	RPE3/CTPLS/PMD3/RE3
32	RPF5/SCL2/PMA8/RF5	64	AN21/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See Section 11.0 "I/O Ports" for more information. 2: 3: Shaded pins are 5V tolerant.

4: The metal plane at the bottom of the QFN device is not connected to any pins and is recommended to be connected to Vss externally.

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

				`	,			
	Pin Number							
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	Pin Type	Buffer Type	Description			
AN36	-	47	I	Analog				
AN37	—	48	I	Analog				
AN38	_	52	I	Analog				
AN39	_	53	I	Analog				
AN40	_	79	I	Analog				
AN41	_	80	I	Analog				
AN42	_	83	I	Analog	Analog input channels.			
AN43	_	84	I	Analog				
AN44	_	87	I	Analog				
AN45	_	88	I	Analog				
AN46	_	93	I	Analog				
AN47	_	94	I	Analog				
CLKI	39	63	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.			
CLKO	40	64	0	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with the OSC2 pin function.			
OSC1	39	63	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.			
OSC2	40	64	0	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.			
SOSCI	47	73	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.			
SOSCO	48	74	0	—	32.768 kHz low-power oscillator crystal output.			
IC1	PPS	PPS	I	ST				
IC2	PPS	PPS	Ι	ST				
IC3	PPS	PPS	I	ST	Capture Input 1-5			
IC4	PPS	PPS	I	ST				
IC5	PPS	PPS	I	ST				
OC1	PPS	PPS	0	ST	Output Compare Output 1			
OC2	PPS	PPS	0	ST	Output Compare Output 2			
OC3	PPS	PPS	0	ST	Output Compare Output 3			
OC4	PPS	PPS	0	ST	Output Compare Output 4			
OC5	PPS	PPS	0	ST	Output Compare Output 5			
OCFA	PPS	PPS	I	ST	Output Compare Fault A Input			
OCFB	30	44	Ι	ST	Output Compare Fault B Input			
Legend:	CMOS = CN	IOS compat	ible inp	ut or output	Analog = Analog input I = Input O = Output			

ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = P

P = Power

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 18-16 PLLMULT<2:0>: Phase-Locked Loop (PLL) Multiplier bits

- 111 = Clock is multiplied by 24
- 110 = Clock is multiplied by 21
- 101 = Clock is multiplied by 20
- 100 = Clock is multiplied by 19
- 011 = Clock is multiplied by 18
- 010 =Clock is multiplied by 17
- 001 =Clock is multiplied by 16
- 000 = Clock is multiplied by 15
- bit 15 Unimplemented: Read as '0'
- bit 14-12 COSC<2:0>: Current Oscillator Selection bits
 - 111 = Internal Fast RC (FRC) Oscillator divided by OSCCON<FRCDIV> bits
 - 110 = Internal Fast RC (FRC) Oscillator divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator (Posc) with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (Posc) (XT, HS or EC)
 - 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast RC (FRC) Oscillator
- bit 11 Unimplemented: Read as '0'
- bit 10-8 NOSC<2:0>: New Oscillator Selection bits
 - 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
 - 110 = Internal Fast RC Oscillator (FRC) divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (XT, HS or EC)
 - 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast Internal RC Oscillator (FRC)

On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).

- bit 7 CLKLOCK: Clock Selection Lock Enable bit
 - If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):
 - 1 = Clock and PLL selections are locked
 - 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x): Clock and PLL selections are never locked and may be modified.

- bit 6 ULOCK: USB PLL Lock Status bit⁽¹⁾
 - 1 = Indicates that the USB PLL module is in lock or USB PLL module start-up timer is satisfied
 - 0 = Indicates that the USB PLL module is out of lock or USB PLL module start-up timer is in progress or USB PLL is disabled
- bit 5 SLOCK: PLL Lock Status bit
 - 1 = PLL module is in lock or PLL module start-up timer is satisfied
 - 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled
- bit 4 SLPEN: Sleep Mode Enable bit
 - 1 = Device will enter Sleep mode when a WAIT instruction is executed
 - 0 = Device will enter Idle mode when a WAIT instruction is executed
- bit 3 **CF:** Clock Fail Detect bit
 - 1 = FSCM has detected a clock failure
 - 0 = No clock failure has been detected
- Note 1: This bit is available on PIC32MX2XX/5XX devices only.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—		—		—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	-	—	-	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—		—		—
	R/WC-0, HS	U-0	R/WC-0, HS					
7:0	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	_	VBUSVDIF

REGISTER 10-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Legend:	WC = Write '1' to clear	HS = Hardware Settable b	bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7 IDIF: ID State Change Indicator bit
 - 1 = Change in ID state detected
 - 0 = No change in ID state detected
- bit 6 T1MSECIF: 1 Millisecond Timer bit
 - 1 = 1 millisecond timer has expired
 - 0 = 1 millisecond timer has not expired

bit 5 LSTATEIF: Line State Stable Indicator bit

- 1 = USB line state has been stable for 1millisecond, but different from last time
- 0 = USB line state has not been stable for 1 millisecond

bit 4 ACTVIF: Bus Activity Indicator bit

- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected
- bit 3 SESVDIF: Session Valid Change Indicator bit
 - 1 = VBUS voltage has dropped below the session end level
 - 0 = VBUS voltage has not dropped below the session end level
- bit 2 SESENDIF: B-Device VBUS Change Indicator bit
 - 1 = A change on the session end input was detected
 - 0 = No change on the session end input was detected
- bit 1 Unimplemented: Read as '0'
- bit 0 VBUSVDIF: A-Device VBUS Change Indicator bit
 - 1 = Change on the session valid input detected
 - 0 = No change on the session valid input detected

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0						
31.24	—	-	—	—	—	_	_	—
22.16	U-0	U-0						
23.10	—		—	-	-			—
15.0	U-0	U-0						
15.0	—		—	-	-			—
	R/WC-0, HS	R-0	R/WC-0, HS					
7:0	STALLIE		DESIMEIE(2)		TRNIF(3)	SOFIE	UERRIF ⁽⁴⁾	URSTIF ⁽⁵⁾
	OTALLI		REGOMEN	IDEEIF		00111		DETACHIF ⁽⁶⁾

REGISTER 10-6: U1IR: USB INTERRUPT REGISTER

Legend:	WC = Write '1' to clear	HS = Hardware Settable	e bit
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

510 0 1	Ŭ	
bit 7		STALLIF: STALL Handshake Interrupt bit
		1 = In Host mode, a STALL handshake was received during the handshake phase of the transaction
		In Device mode, a STALL handshake was transmitted during the handshake phase of the transaction
		0 = STALL handshake has not been sent
bit 6		ATTACHIF: Peripheral Attach Interrupt bit ⁽¹⁾
		1 = Peripheral attachment was detected by the USB module
		0 = Peripheral attachment was not detected
bit 5		RESUMEIF: Resume Interrupt bit ⁽²⁾
		$1 =$ K-State is observed on the D+ or D- pin for 2.5 μ s
		0 = K-State is not observed
bit 4		IDLEIF: Idle Detect Interrupt bit
		1 = Idle condition detected (constant Idle state of 3 ms or more)
		0 = NO idle condition detected
bit 3		TRNIF: loken Processing Complete Interrupt bit ⁽⁹⁾
		\perp = Processing of current token is complete; a read of the UTSTAT register will provide endpoint information
hit O		
DIL Z		1 = SOF token received by the peripheral or the SOF threshold reached by the bost
		0 = SOF token was not received nor threshold reached
hit 1		UERRIE: USB Error Condition Interrupt bit ⁽⁴⁾
Sit 1		1 = Unmasked error condition has occurred
		0 = Unmasked error condition has not occurred
bit 0		URSTIF: USB Reset Interrupt bit (Device mode) ⁽⁵⁾
		1 = Valid USB Reset has occurred
		0 = No USB Reset has occurred
bit 0		DETACHIF: USB Detach Interrupt bit (Host mode) ⁽⁶⁾
		1 = Peripheral detachment was detected by the USB module
		0 = Peripheral detachment was not detected
Note	1:	This bit is valid only if the HOSTEN bit is set (see Register 10-11), there is no activity on the USB for
		2.5 μ s, and the current bus state is not SE0.
	2:	When not in Suspend mode, this interrupt should be disabled.
	3:	Clearing this bit will cause the STAT FIFO to advance.
	4:	Only error conditions enabled through the U1EIE register will set this bit.
	5:	Device mode.
	6:	Host mode.

REGISTER 10-10: U1STAT: USB STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—		—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—		—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—		—	—	—	—	—
7.0	R-x	R-x	R-x	R-x	R-x	R-x	U-0	U-0
7.0		ENDP.	T<3:0>		DIR	PPBI	_	_

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits (Represents the number of the BDT, updated by the last USB transfer.)
 - 1111 = Endpoint 15 1110 = Endpoint 14 . . 0001 = Endpoint 1 0000 = Endpoint 0
- bit 3 **DIR:** Last BD Direction Indicator bit
 - 1 = Last transaction was a transmit transfer (TX)
 - 0 = Last transaction was a receive transfer (RX)
- bit 2 **PPBI:** Ping-Pong BD Pointer Indicator bit
 - 1 = The last transaction was to the ODD BD bank
 - 0 = The last transaction was to the EVEN BD bank
- bit 1-0 Unimplemented: Read as '0'

Note: The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. U1STAT value is only valid when the TRNIF bit (U1IR<3>) is active. Clearing the TRNIF bit advances the FIFO. Data in register is invalid when the TRNIF bit = 0.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	—	—	—	—	—	—	—	—		
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	—	—	—	—	—	—		
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	WCS2 ⁽¹⁾	WCS1 ⁽³⁾								
	WADDR15 ⁽²⁾	WADDR14 ⁽⁴⁾		WADDR<13:8>						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				WADDR<	7:0>					

REGISTER 20-8: PMWADDR: PARALLEL PORT WRITE ADDRESS REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 31-16 Unimplemented: Read as '0'
- bit 15 WCS2: Chip Select 2 bit⁽¹⁾
 - 1 = Chip Select 2 is active
 - 0 = Chip Select 2 is inactive
- bit 15 WADDR<15>: Target Address bit 15⁽²⁾
- bit 14 WCS1: Chip Select 1 bit⁽³⁾
 - 1 = Chip Select 1 is active
 - 0 = Chip Select 1 is inactive
- bit 14 WADDR<14>: Target Address bit 14⁽⁴⁾
- bit 13-0 WADDR<13:0>: Address bits
- **Note 1:** When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
 - **2:** When the CSF<1:0> bits (PMCON<7:6>) = 00.
 - **3:** When the CSF<1:0> bits (PMCON<7:6>) = 10.
 - **4:** When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to '1'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
31:24		YEAR1	0<3:0>			YEAR0	1<3:0>	
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
23:16		MONTH	10<3:0>			MONTH	01<3:0>	
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15:8		DAY10	<3:0>			DAY01	<3:0>	
7.0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
7:0	—	—	—	—		WDAYO)1<3:0>	
Legend:								
R = Read	lable bit		W = Writable	e bit	U = Unimple	emented bit, re	ead as '0'	
-n = Value	e at POR		'1' = Bit is se	et	'0' = Bit is cl	eared	x = Bit is un	known

REGISTER 21-4: RTCDATE: RTC DATE VALUE REGISTER

bit 31-28 YEAR10<3:0>: Binary-Coded Decimal Value of Years bits, 10s place digits

bit 27-24 YEAR01<3:0>: Binary-Coded Decimal Value of Years bits, 1s place digit

bit 23-20 MONTH10<3:0>: Binary-Coded Decimal Value of Months bits, 10s place digits; contains a value of 0 or 1

bit 19-16 MONTH01<3:0>: Binary-Coded Decimal Value of Months bits, 1s place digit; contains a value from 0 to 9

bit 15-12 DAY10<3:0>: Binary-Coded Decimal Value of Days bits, 10s place digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary-Coded Decimal Value of Days bits, 1s place digit; contains a value from 0 to 9

bit 7-4 Unimplemented: Read as '0'

bit 3-0 WDAY01<3:0>: Binary-Coded Decimal Value of Weekdays bits,1s place digit; contains a value from 0 to 6

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
31.24	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	-	—
22.16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
10.0	IVRIF	WAKIF	CERRIF	SERRIF ⁽¹⁾	RBOVIF	—	-	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0					MODIF	CTMRIF	RBIF	TBIF

REGISTER 23-3: C1INT: CAN INTERRUPT REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	IVRIE: Invalid Message Received Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 30	WAKIE: CAN Bus Activity Wake-up Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 29	CERRIE: CAN Bus Error Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 28	SERRIE: System Error Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 27	RBOVIE: Receive Buffer Overflow Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 26-20	Unimplemented: Read as '0'
bit 19	MODIE: Mode Change Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 18	CTMRIE: CAN Timestamp Timer Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 17	RBIE: Receive Buffer Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 16	TBIE: Transmit Buffer Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 15	IVRIF: Invalid Message Received Interrupt Flag bit 1 = An invalid messages interrupt has occurred 0 = An invalid message interrupt has not occurred
Note 1:	This bit can only be cleared by turning the CAN module Off and On by cl

learing or setting the ON bit N (C1CON<15>).

REGISTER 23-16: C1FIFOCONn: CAN FIFO CONTROL REGISTER 'n' ('n' = 0 THROUGH 15) (CONTINUED)

- bit 7 TXEN: TX/RX Buffer Selection bit 1 = FIFO is a Transmit FIFO 0 = FIFO is a Receive FIFO TXABAT: Message Aborted bit⁽²⁾ bit 6 1 = Message was aborted 0 = Message completed successfully TXLARB: Message Lost Arbitration bit⁽³⁾ bit 5 1 = Message lost arbitration while being sent 0 = Message did not lose arbitration while being sent TXERR: Error Detected During Transmission bit⁽³⁾ bit 4 1 = A bus error occured while the message was being sent 0 = A bus error did not occur while the message was being sent bit 3 **TXREQ:** Message Send Request TXEN = 1: (FIFO configured as a Transmit FIFO) Setting this bit to '1' requests sending a message. The bit will automatically clear when all the messages queued in the FIFO are successfully sent. Clearing the bit to '0' while set ('1') will request a message abort. TXEN = 0: (FIFO configured as a receive FIFO) This bit has no effect. bit 2 RTREN: Auto RTR Enable bit 1 = When a remote transmit is received, TXREQ will be set 0 = When a remote transmit is received. TXREQ will be unaffected bit 1-0 TXPR<1:0>: Message Transmit Priority bits 11 = Highest message priority 10 = High intermediate message priority 01 = Low intermediate message priority
 - 00 = Lowest message priority
- **Note 1:** These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (C1CON<23:21>) = 100).
 - 2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
 - 3: This bit is reset on any read of this register or when the FIFO is reset.

NOTES:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P
31:24	—	—	—	—	—	—	FWDTWI	NSZ<1:0>
00.40	R/P	R/P	r-1	R/P	R/P	R/P	R/P	R/P
23:10	FWDTEN	WINDIS	—			WDTPS<4:0>		
45.0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
15:8	FCKSM	/<1:0>	FPBDI	V<1:0>	—	OSCIOFNC	POSCM	OD<1:0>
7.0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
7:0	IESO	_	FSOSCEN	_	_	F	NOSC<2:0>	

REGISTER 28-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 Reserved: Write '1'

bit 25-24 **FWDTWINSZ:** Watchdog Timer Window Size bits

- 11 = Window size is 25%
- 10 = Window size is 37.5%
- 01 = Window size is 50%
- 00 = Window size is 75%

bit 23 FWDTEN: Watchdog Timer Enable bit

- 1 = Watchdog Timer is enabled and cannot be disabled by software
- 0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 WINDIS: Watchdog Timer Window Enable bit

- 1 = Watchdog Timer is in non-Window mode
- 0 = Watchdog Timer is in Window mode
- bit 21 Reserved: Write '1'

bit 20-16 WDTPS<4:0>: Watchdog Timer Postscale Select bits

•
10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

FIGURE 31-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



TABLE 31-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHA	RACTER	ISTICS	Standar (unless Operatin	d Operating C otherwise stat g temperature	onditions: ted) -40°C ≤ ⁻ -40°C ≤ ⁻	2.3V to 5 TA ≤ +85° TA ≤ +105	3.6V C for Industrial i°C for V-temp
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	_	_	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time		—	_	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 31-9: OCx/PWM MODULE TIMING CHARACTERISTICS



TABLE 31-27: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHAF	RACTERIST	rics	Standard (unless of Operating	d Operating C otherwise sta g temperature	Conditions ited) -40°C ≤ -40°C ≤	s: 2.3V to ≤ Ta ≤ +85° ≤ Ta ≤ +105	3.6V C for Industrial 5°C for V-temp
Param No.	Symbol	Characteristics ⁽¹⁾	Min	Typical ⁽²⁾	Max	Units	Conditions
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	
OC20	TFLT	Fault Input Pulse Width	50	—	_	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.



FIGURE 31-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

TABLE 31-30: SPIX MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHA	ARACTERIS	TICS	Standard (unless of Operating	Operati therwise tempera	ng Con e stated ture -40 -40	ditions J) P°C ≤ TA : P°C ≤ TA :	: 2.3V to 3.6V ≤ +85°C for Industrial ≤ +105°C for V-temp
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time (Note 3)	TSCK/2	—		ns	—
SP71	TscH	SCKx Input High Time (Note 3)	TSCK/2	—		ns	—
SP72	TscF	SCKx Input Fall Time	—	—		ns	See parameter DO32
SP73	TscR	SCKx Input Rise Time	—	_		ns	See parameter DO31
SP30	TDOF	SDOx Data Output Fall Time (Note 4)	—	_		ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	—	_		ns	See parameter DO31
SP35	TSCH2DOV,	SDOx Data Output Valid after	_	_	15	ns	VDD > 2.7V
	TscL2DoV	SCKx Edge	—	_	20	ns	VDD < 2.7V
SP40	TDIV2sCH, TDIV2sCL	Setup Time of SDIx Data Input to SCKx Edge	10	—		ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10			ns	—
SP50	TssL2scH, TssL2scL	SSx \downarrow to SCKx \uparrow or SCKx Input	175	_	—	ns	—
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance (Note 3)	5	_	25	ns	—
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	Тѕск + 20	—		ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns.

4: Assumes 50 pF load on all SPIx pins.



FIGURE 31-13: SPIX MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

TABLE 31-31: SPIX MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHA	RACTERIS	TICS	Standard (unless of Operating	d Operating otherwise st temperature	Conditi tated) e -40°C -40°C	ions: 2.3 ≤ Ta ≤ +8 ≤ Ta ≤ +3	3V to 3.6V 35°C for Industrial 105°C for V-temp
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time (Note 3)	Tsck/2		_	ns	—
SP71	TscH	SCKx Input High Time (Note 3)	Tsck/2	—	_	ns	—
SP72	TscF	SCKx Input Fall Time	_	5	10	ns	—
SP73	TscR	SCKx Input Rise Time	_	5	10	ns	—
SP30	TDOF	SDOx Data Output Fall Time (Note 4)	_	—	_	ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	_	—	_	ns	See parameter DO31
SP35	TscH2doV,	SDOx Data Output Valid after	_	_	20	ns	VDD > 2.7V
	TscL2DoV	SCKx Edge	_	_	30	ns	VDD < 2.7V
SP40	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	_	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	_		ns	_
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \downarrow or SCKx \uparrow Input	175			ns	_

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 3: The minimum clock period for SCKx is 50 ns.
- **4:** Assumes 50 pF load on all SPIx pins.

|--|

АС СНА	RACTER	ISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Charact	eristics	Min. ⁽¹⁾	Max.	Units	Conditions	
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Трв * (BRG + 2)		μs	_	
			400 kHz mode	Трв * (BRG + 2)		μs	—	
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μs	_	
IM11	THI:SCL	Clock High Time	100 kHz mode	Трв * (BRG + 2)	_	μS		
			400 kHz mode	Трв * (BRG + 2)	_	μS	—	
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μS	—	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	_	300	ns	CB is specified to be from 10 to 400 pF	
			400 kHz mode	20 + 0.1 Св	300	ns		
			1 MHz mode (Note 2)	—	100	ns		
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	_	1000	ns	CB is specified to be from 10 to 400 pF	
			400 kHz mode	20 + 0.1 Св	300	ns		
			1 MHz mode (Note 2)	_	300	ns		
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250		ns		
			400 kHz mode	100		ns	-	
			1 MHz mode (Note 2)	100	—	ns		
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	_	
			400 kHz mode	0	0.9	μS		
			1 MHz mode (Note 2)	0	0.3	μS		
IM30	Tsu:sta	Start Condition Setup Time	100 kHz mode	Трв * (BRG + 2)	—	μs	Only relevant for Repeated Start condition	
			400 kHz mode	Трв * (BRG + 2)		μs		
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μS		
IM31	Thd:sta	Start Condition Hold Time	100 kHz mode	Трв * (BRG + 2)		μs	After this period, the first clock pulse is generated	
			400 kHz mode	Трв * (BRG + 2)	—	μS		
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μS		
IM33	Tsu:sto	Stop Condition Setup Time	100 kHz mode	Трв * (BRG + 2)		μs		
			400 kHz mode	Трв * (BRG + 2)	—	μS		
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μS		
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	Трв * (BRG + 2)		ns	_	
			400 kHz mode	Трв * (BRG + 2)		ns		
			1 MHz mode (Note 2)	Трв * (BRG + 2)	_	ns		

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

FIGURE 31-20: PARALLEL SLAVE PORT TIMING



64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimensior	MIN	NOM	MAX			
ontact Pitch E			0.50 BSC			
Contact Pad Spacing	C1		11.40			
Contact Pad Spacing	C2		11.40			
Contact Pad Width (X64)	X1			0.30		
Contact Pad Length (X64)	Y1			1.50		
Distance Between Pads	G	0.20				

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]



Microchip Technology Drawing C04-154A Sheet 1 of 2