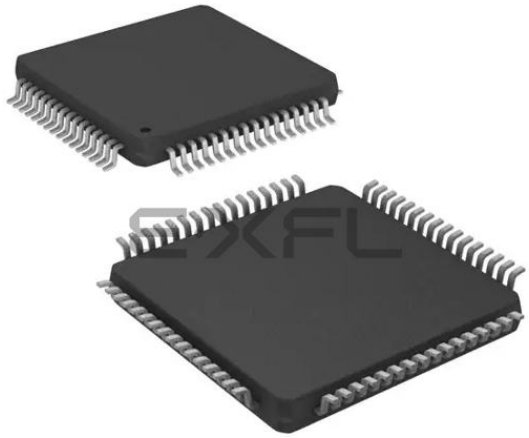
Microchip Technology - PIC32MX530F128HT-50I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx530f128ht-50i-pt

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP			
$\overline{MCLR}$	7	13	I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	19	30	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	20	31	P	P	Ground reference for analog modules
VDD	10, 26, 38, 57	2, 16, 37, 46, 62, 86	P	—	Positive supply for peripheral logic and I/O pins
VCAP	56	85	P	—	Capacitor for Internal Voltage Regulator
VSS	9, 25, 41	15, 36, 45, 65, 75	P	—	Ground reference for logic and I/O pins
VREF+	16	29	P	Analog	Analog Voltage Reference (High) Input
VREF-	15	28	P	Analog	Analog Voltage Reference (Low) Input

Legend: CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

TABLE 3-3: MIPS32® M4K® PROCESSOR CORE EXCEPTION TYPES

Exception	Description
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR).
DSS	EJTAG debug single step.
DINT	EJTAG debug interrupt. Caused by the assertion of the external *EJ_DINT* input or by setting the EjtagBrk bit in the ECR register.
NMI	Assertion of NMI signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
DIB	EJTAG debug hardware instruction break matched.
AdEL	Fetch address alignment error. Fetch reference to protected address.
IBE	Instruction fetch bus error.
DBp	EJTAG breakpoint (execution of SDBBP instruction).
Sys	Execution of SYSCALL instruction.
Bp	Execution of BREAK instruction.
RI	Execution of a reserved instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a CorExtend instruction when CorExtend is not enabled.
Ov	Execution of an arithmetic instruction that overflowed.
Tr	Execution of a trap (when trap condition is true).
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
DBE	Load or store bus error.
DDBL	EJTAG data hardware breakpoint matched in load data compare.

3.3 Power Management

The MIPS® M4K® processor core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see **Section 27.0 "Power-Saving Features"**.

3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the PIC32MX-1XX/2XX/5XX 64/100-pin family core is in the clock tree and clocking registers. The PIC32MX family uses extensive use of local gated-clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The MIPS® M4K® processor core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K® core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

4.2 Special Function Register Maps

TABLE 4-2: BUS MATRIX REGISTER MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	BMXCON(1)	31:16	—	—	—	—	—	BMXCHEDMA	—	—	—	—	—	BMXERRIXI	BMXERRICD	BMXERRDMA	BMXERRDS	BMXERRIS	041F
		15:0	—	—	—	—	—	—	—	—	—	BMXWSDRM	—	—	—	BMXARB<2:0>			0047
2010	BMXDKPBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDKPBA<15:0>																0000
2020	BMXDUDBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDUDBA<15:0>																0000
2030	BMXDUPBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDUPBA<15:0>																0000
2040	BMXDRMSZ	31:16	BMXDRMSZ<31:0>																xxxx
		15:0																	xxxx
2050	BMXPUPBA(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	BMXPUPBA<19:16>				0000
		15:0	BMXPUPBA<15:0>																0000
2060	BMXPFMSZ	31:16	BMXPFMSZ<31:0>																xxxx
		15:0																	xxxx
2070	BMXBOOTSZ	31:16	BMXBOOTSZ<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

7.0 RESETS

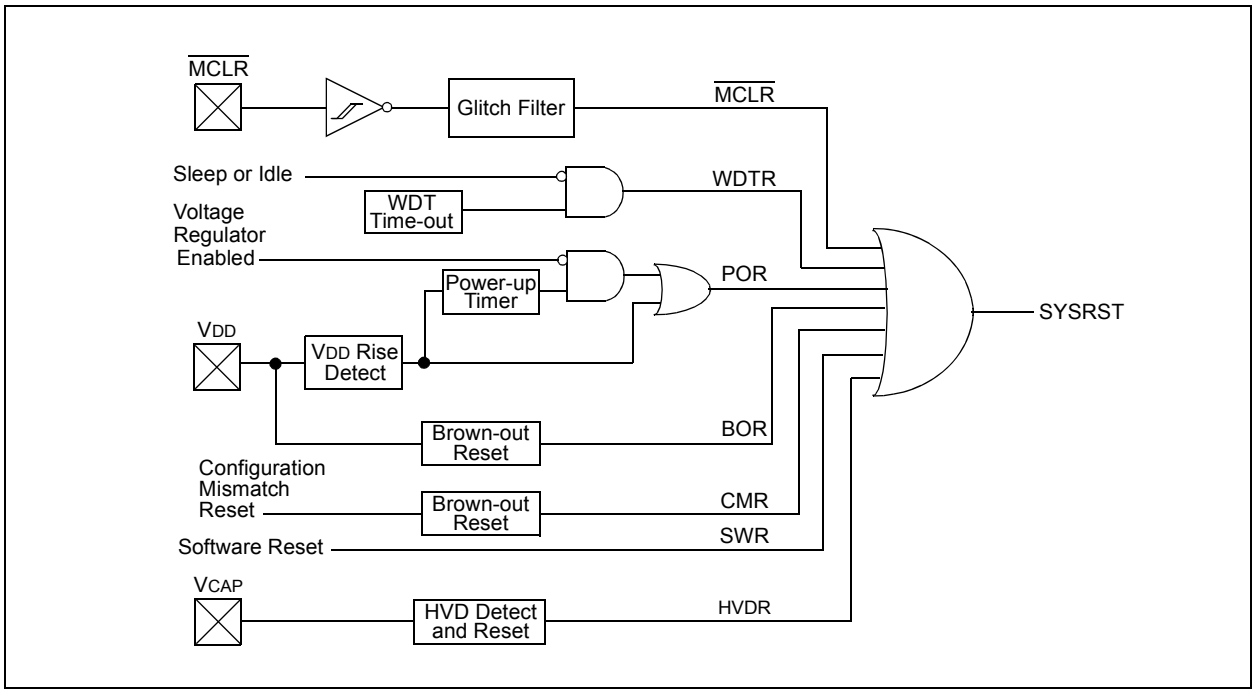
Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- $\overline{\text{MCLR}}$: Master Clear Reset pin
- SWR: Software Reset
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- CMR: Configuration Mismatch Reset
- HVDR: High Voltage Detect Reset

A simplified block diagram of the Reset module is illustrated in Figure 7-1.

FIGURE 7-1: SYSTEM RESET BLOCK DIAGRAM



REGISTER 7-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0, HS	U-0	U-0	U-0	U-0	U-0
	—	—	HVDR	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0
	—	—	—	—	—	—	CMR	VREGS
7:0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR(1)	POR(1)

Legend:	HS = Set by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29 **HVDR:** High Voltage Detect Reset Flag bit
- 1 = High Voltage Detect (HVD) Reset has occurred, voltage on V_{CAP} > 2.5V
- 0 = HVD Reset has not occurred

bit 28-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
- 1 = Configuration mismatch Reset has occurred
- 0 = Configuration mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby Enable bit
- 1 = Regulator is enabled and is on during Sleep mode
- 0 = Regulator is disabled and is off during Sleep mode

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit
- 1 = Master Clear (pin) Reset has occurred
- 0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit
- 1 = Software Reset was executed
- 0 = Software Reset as not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
- 1 = WDT Time-out has occurred
- 0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
- 1 = Device was in Sleep mode
- 0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit
- 1 = Device was in Idle mode
- 0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
- 1 = Brown-out Reset has occurred
- 0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
- 1 = Power-on Reset has occurred
- 0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view next detection.

9.1 Control Registers

TABLE 9-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	0000
3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	DMACH<2:0>			0000
3020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

TABLE 9-2: DMA CRC REGISTER MAP

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>			0000
3040	DCRCDATA	31:16	DCRCDATA<31:0>																0000
		15:0																	0000
3050	DCRCXOR	31:16	DCRCXOR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO(1)	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP(1)	CRCTYP	—	—	CRCCH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits
- 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
- 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
- 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
- 00 = No swapping (i.e., source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit(1)
- 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
- 0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit(1

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits(1)

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit
- 1 = CRC module is enabled and channel transfers are routed through the CRC module
- 0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

10.0 USB ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS60001126) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, full-speed device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 10-1.

The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The PIC32 USB module includes the following features:

- USB Full-speed support for host and device
- Low-speed host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

Note: The implementation and use of the USB specifications, and other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

11.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

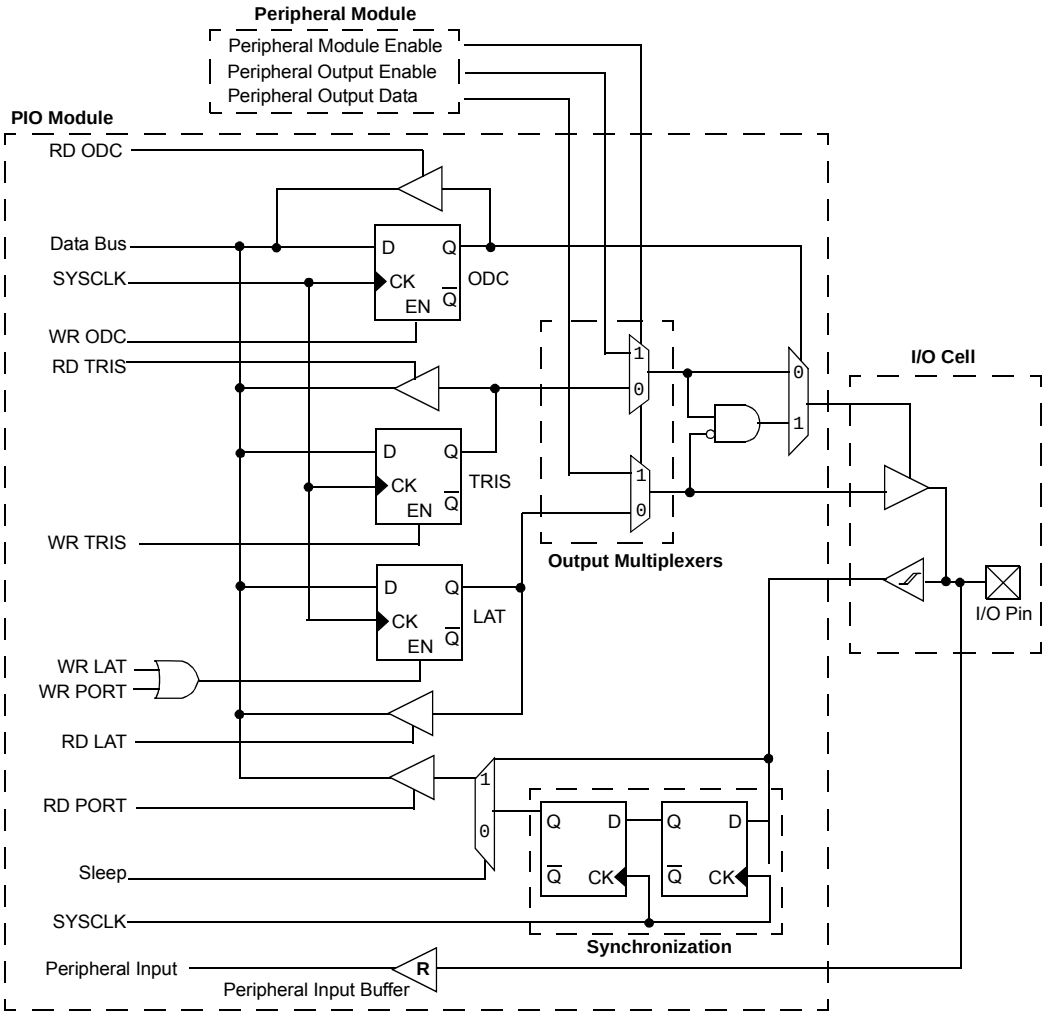
General purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate functions. These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

The following are the key features of this module:

- Individual output pin open-drain enable or disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

Figure 11-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE



Legend: R = Peripheral input buffer types may vary. Refer to Table 1-1 for peripheral details.

Note: This block diagram is a general representation of a shared port/peripheral structure for illustration purposes only. The actual structure for any specific port/peripheral combination may be different than shown here.

TABLE 11-18: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FBFC	RPD15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD15<3:0>				0000
FC0C	RPE3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE3<3:0>				0000
FC14	RPE5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE5<3:0>				0000
FC20	RPE8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE8<3:0>				0000
FC24	RPE9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE9<3:0>				0000
FC40	RPF0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF0<3:0>				0000
FC44	RPF1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF1<3:0>				0000
FC48	RPF2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF2<3:0>				0000
FC4C	RPF3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF3<3:0>				0000
FC50	RPF4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF4<3:0>				0000
FC54	RPF5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF5<3:0>				0000
FC58	RPF6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF6<3:0>				0000
FC5C	RPF7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF6<3:0>				0000
FC60	RPF8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF7<3:0>				0000
FC70	RPF12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF12<3:0>				0000
FC74	RPF13R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF13<3:0>				0000
FC80	RPG0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG0<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available if the associated RPx function is not present on the device. Refer to the pin table for the specific device to determine availability.

REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit

When TCS = 1:

1 = External clock input is synchronized

0 = External clock input is not synchronized

When TCS = 0:

This bit is ignored.

bit 1 **TCS:** Timer Clock Source Select bit

1 = External clock from TxCKI pin

0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/PMWR port enabled
0 = PMRD/PMWR port disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits(2)
11 = Reserved
10 = PMCS1 and PMCS2 function as Chip Select
01 = PMCS1 functions as address bit 14; PMCS2 functions as Chip Select
00 = PMCS1 and PMCS2 function as address bits 14 and 15, respectively

bit 5 **ALP:** Address Latch Polarity bit(2)
1 = Active-high (PMALL and PMALH)
0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

bit 4 **CS2P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS2)
0 = Active-low ($\overline{\text{PMCS2}}$)

bit 3 **CS1P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS1)
0 = Active-low ($\overline{\text{PMCS1}}$)

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Write strobe active-high (PMWR)
0 = Write strobe active-low ($\overline{\text{PMWR}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Read Strobe active-high (PMRD)
0 = Read Strobe active-low ($\overline{\text{PMRD}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 20-10: PMRDIN: PARALLEL PORT READ INPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RDATAIN<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RDATAIN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RDATAIN<15:0>:** Port Read Input Data bits

Note:	This register is only used when the DUALBUF bit (PMCON<17>) is set to '1' and exclusively for reads. If the DUALBUF bit is '0', the PMDIN register (Register 20-5) is used for reads instead of PMRDIN.

REGISTER 23-13: C1FLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED)

bit 20-16 **FSEL14<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 15 **FLTEN13:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL13<1:0>:** Filter 13 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL13<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN12:** Filter 12 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL12<1:0>:** Filter 12 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL12<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

28.2 Registers

TABLE 28-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0BF0	DEVCFG3	31:16	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	USERID<15:0>																xxxx
0BF4	DEVCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	FPLLODIV<2:0>			xxxx
		15:0	UPLLEN(1)	—	—	—	—	UPLLIDIV<2:0>(1)			—	FPLLMUL<2:0>			—	FPLLIDIV<2:0>			xxxx
0BF8	DEVCFG1	31:16	—	—	—	—	—	—	FWDTWINSZ<1:0>		FWDTEN	WINDIS	—	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>		IESO	—	FSOSCEN	—	—	FNOSC<2:0>			xxxx
0BFC	DEVCFG0	31:16	—	—	—	CP	—	—	—	BWP	—	—	—	—	PWP<9:6>				xxxx
		15:0	PWP<5:0>				—	—	—	—	—	—	—	ICESEL<1:0>		JTAGEN	DEBUG<1:0>		xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This bit is only available on devices with a USB module.

TABLE 28-2: DEVICE AND REVISION ID SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F200	CFGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	IOLOCK	PMDLOCK	—	—	—	—	—	—	—	—	JTAGEN	TROEN(2)	—	TDOEN	000B
F220	DEVID	31:16	VER<3:0>				DEVID<27:16>												xxxx
		15:0	DEVID<15:0>																xxxx
F230	SYSKEY(3)	31:16	SYSKEY<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device.

2: This bit is not available on 64-pin devices.

REGISTER 28-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P
	—	—	—	—	—	—	FWDTWINSZ<1:0>	
23:16	R/P	R/P	r-1	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	—	WDTPS<4:0>				
15:8	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Reserved:** Write '1'

bit 25-24 **FWDTWINSZ:** Watchdog Timer Window Size bits
11 = Window size is 25%
10 = Window size is 37.5%
01 = Window size is 50%
00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled and cannot be disabled by software
0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit
1 = Watchdog Timer is in non-Window mode
0 = Watchdog Timer is in Window mode

bit 21 **Reserved:** Write '1'

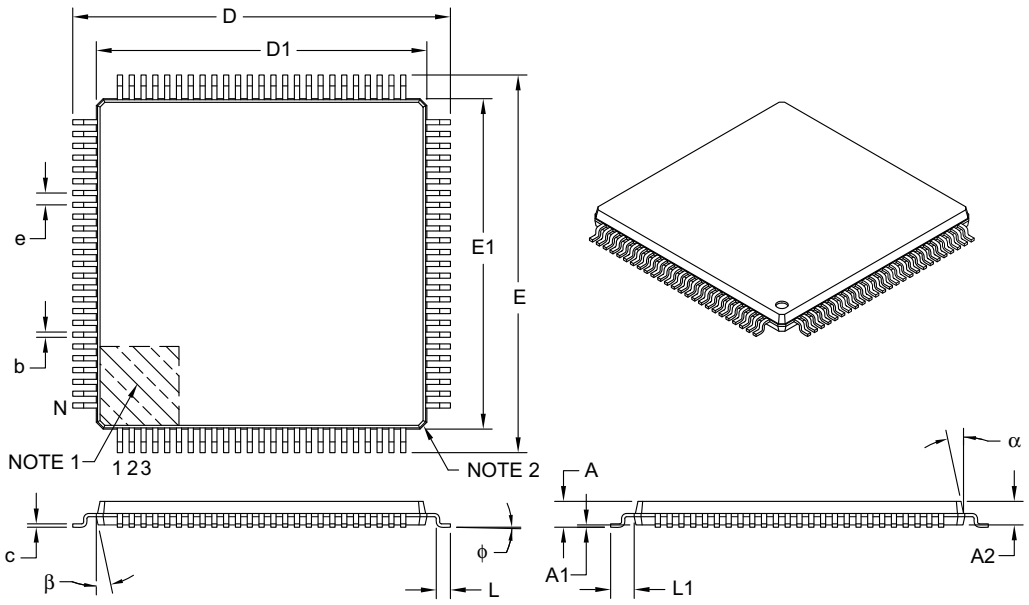
bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits
10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

Note 1: Do not disable the POSC (POSCMOD = 11) when using this oscillator source.

NOTES:

100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		16.00 BSC	
Overall Length	D		16.00 BSC	
Molded Package Width	E1		14.00 BSC	
Molded Package Length	D1		14.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

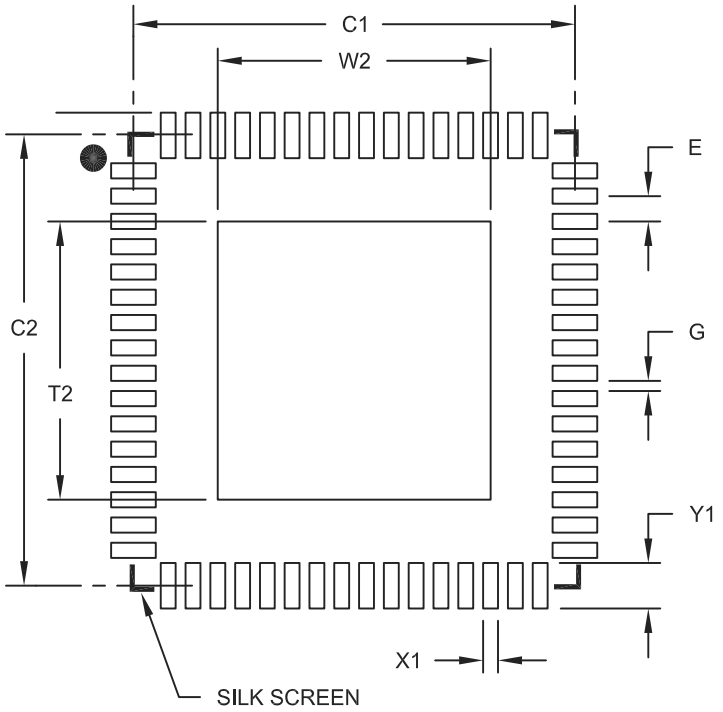
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 5.40x5.40mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			5.50
Optional Center Pad Length	T2			5.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2154A

