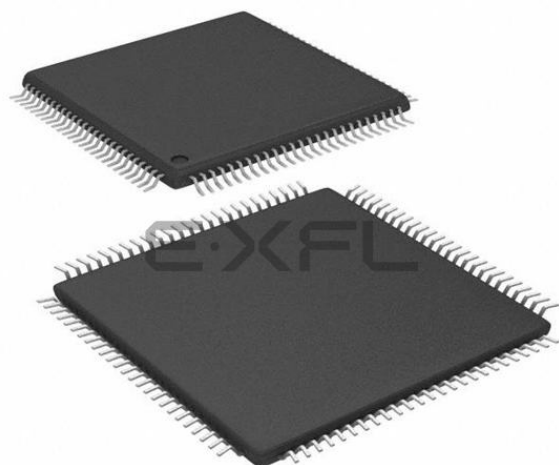




Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                                 |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                                          |
| Core Processor             | MIPS32® M4K™                                                                                                                                                                    |
| Core Size                  | 32-Bit Single-Core                                                                                                                                                              |
| Speed                      | 50MHz                                                                                                                                                                           |
| Connectivity               | CANbus, I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG                                                                                                           |
| Peripherals                | Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT                                                                                                                    |
| Number of I/O              | 81                                                                                                                                                                              |
| Program Memory Size        | 128KB (128K x 8)                                                                                                                                                                |
| Program Memory Type        | FLASH                                                                                                                                                                           |
| EEPROM Size                | -                                                                                                                                                                               |
| RAM Size                   | 16K x 8                                                                                                                                                                         |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V                                                                                                                                                                     |
| Data Converters            | A/D 48x10b                                                                                                                                                                      |
| Oscillator Type            | Internal                                                                                                                                                                        |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                               |
| Mounting Type              | Surface Mount                                                                                                                                                                   |
| Package / Case             | 100-TQFP                                                                                                                                                                        |
| Supplier Device Package    | 100-TQFP (12x12)                                                                                                                                                                |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx530f128l-50i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx530f128l-50i-pt</a> |

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**REGISTER 4-3: BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R-0           | R-0           |
|           | BMXDUDBA<15:8> |                |                |                |                |                |               |               |
| 7:0       | R-0            | R-0            | R-0            | R-0            | R-0            | R-0            | R-0           | R-0           |
|           | BMXDUDBA<7:0>  |                |                |                |                |                |               |               |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUDBA<15:10>:** DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 **BMXDUDBA<9:0>:** Read-Only bits

Value is always '0', which forces 1 KB increments

- Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.
- 2:** The value in this register must be less than or equal to BMXDRMSZ.

## 6.1 Control Registers

**TABLE 6-1: FLASH CONTROLLER REGISTER MAP**

| Virtual Address<br>(BF80_#) | Register<br>Name       | Bit Range | Bits             |       |       |        |         |       |      |      |      |      |      |      |            |      |      |      | All Resets |
|-----------------------------|------------------------|-----------|------------------|-------|-------|--------|---------|-------|------|------|------|------|------|------|------------|------|------|------|------------|
|                             |                        |           | 31/15            | 30/14 | 29/13 | 28/12  | 27/11   | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3       | 18/2 | 17/1 | 16/0 |            |
| F400                        | NVMCON <sup>(1)</sup>  | 31:16     | —                | —     | —     | —      | —       | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                        | 15:0      | WR               | WREN  | WRERR | LVDERR | LVDSTAT | —     | —    | —    | —    | —    | —    | —    | NVMOP<3:0> |      |      |      | 0000       |
| F410                        | NVMKEY                 | 31:16     | NVMKEY<31:0>     |       |       |        |         |       |      |      |      |      |      |      |            |      |      |      | 0000       |
|                             |                        | 15:0      |                  |       |       |        |         |       |      |      |      |      |      |      |            |      |      |      | 0000       |
| F420                        | NVMADDR <sup>(1)</sup> | 31:16     | NVMADDR<31:0>    |       |       |        |         |       |      |      |      |      |      |      |            |      |      |      | 0000       |
|                             |                        | 15:0      |                  |       |       |        |         |       |      |      |      |      |      |      |            |      |      |      | 0000       |
| F430                        | NVMDATA                | 31:16     | NVMDATA<31:0>    |       |       |        |         |       |      |      |      |      |      |      |            |      |      |      | 0000       |
|                             |                        | 15:0      |                  |       |       |        |         |       |      |      |      |      |      |      |            |      |      |      | 0000       |
| F440                        | NVMSRC<br>ADDR         | 31:16     | NVMSRCADDR<31:0> |       |       |        |         |       |      |      |      |      |      |      |            |      |      |      | 0000       |
|                             |                        | 15:0      |                  |       |       |        |         |       |      |      |      |      |      |      |            |      |      |      | 0000       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

---

NOTES:

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## 9.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

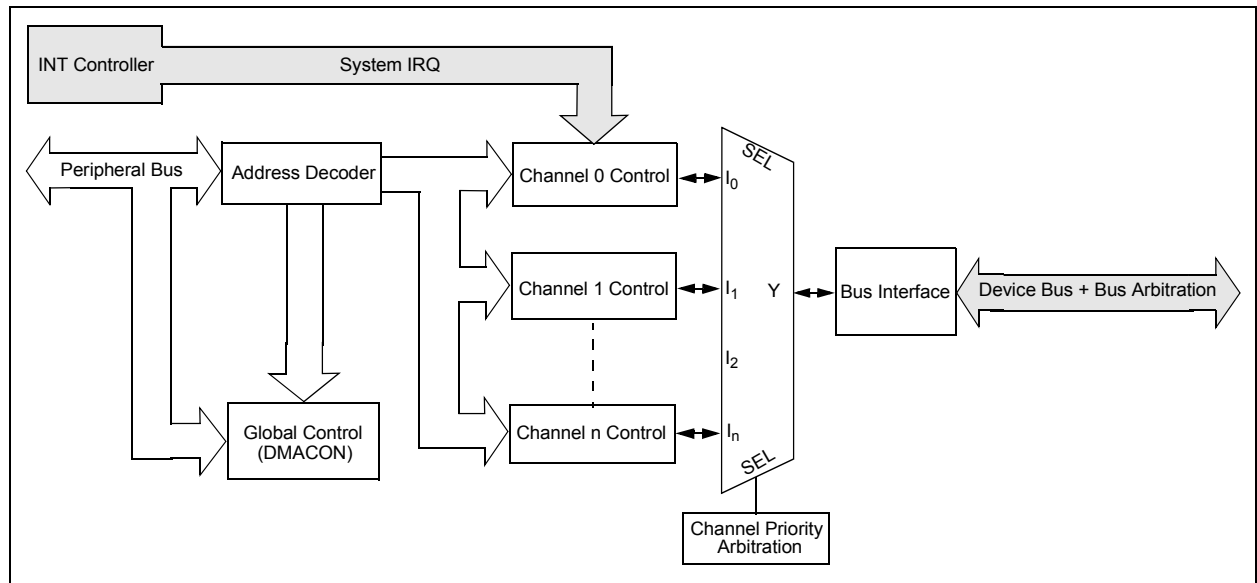
The PIC32 Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32 (such as Peripheral Bus (PBUS) devices: SPI, UART, PMP, etc.) or memory itself.

The following are some of the key features of the DMA controller module:

- Four identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination

- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

**FIGURE 9-1: DMA BLOCK DIAGRAM**



**TABLE 9-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP**

| Virtual Address<br>(BF88_#) | Register<br>Name <sup>(1)</sup> | Bit Range | Bits         |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | All Resets |
|-----------------------------|---------------------------------|-----------|--------------|-------|-------|-------|-------|-------|------|-------------|-------------|--------|--------|--------|--------|--------|------------|------|------------|
|                             |                                 |           | 31/15        | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8        | 23/7        | 22/6   | 21/5   | 20/4   | 19/3   | 18/2   | 17/1       | 16/0 |            |
| 3060                        | DCH0CON                         | 31:16     | —            | —     | —     | —     | —     | —     | —    | —           | —           | —      | —      | —      | —      | —      | —          | —    | 0000       |
|                             |                                 | 15:0      | CHBUSY       | —     | —     | —     | —     | —     | —    | CHCHNS      | CHEN        | CHAED  | CHCHN  | CHAEN  | —      | CHEDET | CHPRI<1:0> |      | 0000       |
| 3070                        | DCH0ECON                        | 31:16     | —            | —     | —     | —     | —     | —     | —    | CHAIRQ<7:0> |             |        |        |        |        |        |            |      | 00FF       |
|                             |                                 | 15:0      | CHSIRQ<7:0>  |       |       |       |       |       |      |             | CFORCE      | CABORT | PATEN  | SIRQEN | AIRQEN | —      | —          | —    | FFF8       |
| 3080                        | DCH0INT                         | 31:16     | —            | —     | —     | —     | —     | —     | —    | CHSDIE      | CHSHIE      | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE     | 0000 |            |
|                             |                                 | 15:0      | —            | —     | —     | —     | —     | —     | —    | CHSDIF      | CHSHIF      | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF     | 0000 |            |
| 3090                        | DCH0SSA                         | 31:16     | CHSSA<31:0>  |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
|                             |                                 | 15:0      |              |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
| 30A0                        | DCH0DSA                         | 31:16     | CHDSA<31:0>  |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
|                             |                                 | 15:0      |              |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
| 30B0                        | DCH0SSIZ                        | 31:16     | —            | —     | —     | —     | —     | —     | —    | —           | —           | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHSSIZ<15:0> |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
| 30C0                        | DCH0DSIZ                        | 31:16     | —            | —     | —     | —     | —     | —     | —    | —           | —           | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHDSIZ<15:0> |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
| 30D0                        | DCH0SPTR                        | 31:16     | —            | —     | —     | —     | —     | —     | —    | —           | —           | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHSPTR<15:0> |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
| 30E0                        | DCH0DPTR                        | 31:16     | —            | —     | —     | —     | —     | —     | —    | —           | —           | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHDPTR<15:0> |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
| 30F0                        | DCH0CSIZ                        | 31:16     | —            | —     | —     | —     | —     | —     | —    | —           | —           | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHCSIZ<15:0> |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
| 3100                        | DCH0CPTR                        | 31:16     | —            | —     | —     | —     | —     | —     | —    | —           | —           | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHCPTR<15:0> |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
| 3110                        | DCH0DAT                         | 31:16     | —            | —     | —     | —     | —     | —     | —    | —           | —           | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | —            | —     | —     | —     | —     | —     | —    | —           | CHPDAT<7:0> |        |        |        |        |        |            |      | 0000       |
| 3120                        | DCH1CON                         | 31:16     | —            | —     | —     | —     | —     | —     | —    | —           | —           | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHBUSY       | —     | —     | —     | —     | —     | —    | CHCHNS      | CHEN        | CHAED  | CHCHN  | CHAEN  | —      | CHEDET | CHPRI<1:0> |      | 0000       |
| 3130                        | DCH1ECON                        | 31:16     | —            | —     | —     | —     | —     | —     | —    | CHAIRQ<7:0> |             |        |        |        |        |        |            |      | 00FF       |
|                             |                                 | 15:0      | CHSIRQ<7:0>  |       |       |       |       |       |      |             | CFORCE      | CABORT | PATEN  | SIRQEN | AIRQEN | —      | —          | —    | FFF8       |
| 3140                        | DCH1INT                         | 31:16     | —            | —     | —     | —     | —     | —     | —    | CHSDIE      | CHSHIE      | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE     | 0000 |            |
|                             |                                 | 15:0      | —            | —     | —     | —     | —     | —     | —    | CHSDIF      | CHSHIF      | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF     | 0000 |            |
| 3150                        | DCH1SSA                         | 31:16     | CHSSA<31:0>  |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
|                             |                                 | 15:0      |              |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
| 3160                        | DCH1DSA                         | 31:16     | CHDSA<31:0>  |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |
|                             |                                 | 15:0      |              |       |       |       |       |       |      |             |             |        |        |        |        |        |            |      | 0000       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET, and INV Registers” for more information.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

---

NOTES:

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**REGISTER 10-16: U1SOF: USB SOF THRESHOLD REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 7:0       | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0         | R/W-0         |
|           | CNT<7:0>       |                |                |                |                |                |               |               |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical values of the threshold are:

01001010 = 64-byte packet

00101010 = 32-byte packet

00011010 = 16-byte packet

00010010 = 8-byte packet

**REGISTER 10-17: U1BDTP1: USB BDT PAGE 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 7:0       | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0         | U-0           |
|           | BDTPTRL<15:9>  |                |                |                |                |                |               | —             |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-1 **BDTPTRL<15:9>:** BDT Base Address bits

This 7-bit value provides address bits 15 through 9 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

bit 0 **Unimplemented:** Read as '0'



**TABLE 11-15: PORTG REGISTER MAP FOR 100-PIN DEVICES ONLY**

| Virtual Address<br>(BF88_#) | Register<br>Name <sup>(1)</sup> | Bit Range | Bits          |               |               |               |       |       |              |              |              |              |      |      |                    |                    |              |              | All<br>Resets |
|-----------------------------|---------------------------------|-----------|---------------|---------------|---------------|---------------|-------|-------|--------------|--------------|--------------|--------------|------|------|--------------------|--------------------|--------------|--------------|---------------|
|                             |                                 |           | 31/15         | 30/14         | 29/13         | 28/12         | 27/11 | 26/10 | 25/9         | 24/8         | 23/7         | 22/6         | 21/5 | 20/4 | 19/3               | 18/2               | 17/1         | 16/0         |               |
| 6600                        | ANSELG                          | 31:16     | —             | —             | —             | —             | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —            | —            | 0000          |
|                             |                                 | 15:0      | ANSELG15      | —             | —             | —             | —     | —     | ANSELG9      | ANSELG8      | ANSELG7      | ANSELG6      | —    | —    | —                  | —                  | —            | —            | 83C0          |
| 6610                        | TRISG                           | 31:16     | —             | —             | —             | —             | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —            | —            | 0000          |
|                             |                                 | 15:0      | TRISG15       | TRISG14       | TRISG13       | TRISG12       | —     | —     | TRISG9       | TRISG8       | TRISG7       | TRISG6       | —    | —    | TRISG3             | TRISG2             | TRISG1       | TRISG0       | F3CF          |
| 6620                        | PORTG                           | 31:16     | —             | —             | —             | —             | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —            | —            | 0000          |
|                             |                                 | 15:0      | RG15          | RG14          | RG13          | RG12          | —     | —     | RG9          | RG8          | RG7          | RG6          | —    | —    | RG3 <sup>(2)</sup> | RG2 <sup>(2)</sup> | RG1          | RG0          | xxxx          |
| 6630                        | LATG                            | 31:16     | —             | —             | —             | —             | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —            | —            | 0000          |
|                             |                                 | 15:0      | LATG15        | LATG14        | LATG13        | LATG12        | —     | —     | LATG9        | LATG8        | LATG7        | LATG6        | —    | —    | LATG3              | LATG2              | LATG1        | LATG0        | xxxx          |
| 6640                        | ODCG                            | 31:16     | —             | —             | —             | —             | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —            | —            | 0000          |
|                             |                                 | 15:0      | ODCG15        | ODCG14        | ODCG13        | ODCG12        | —     | —     | ODCG9        | ODCG8        | ODCG7        | ODCG6        | —    | —    | ODCG3              | ODCG2              | ODCG1        | ODCG0        | 0000          |
| 6650                        | CNPUG                           | 31:16     | —             | —             | —             | —             | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —            | —            | 0000          |
|                             |                                 | 15:0      | CNPUG15       | CNPUG14       | CNPUG13       | CNPUG12       | —     | —     | CNPUG9       | CNPUG8       | CNPUG7       | CNPUG6       | —    | —    | CNPUG3             | CNPUG2             | CNPUG1       | CNPUG0       | 0000          |
| 6660                        | CNPDG                           | 31:16     | —             | —             | —             | —             | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —            | —            | 0000          |
|                             |                                 | 15:0      | CNPDG15       | CNPDG14       | CNPDG13       | CNPDG12       | —     | —     | CNPDG9       | CNPDG8       | CNPDG7       | CNPDG6       | —    | —    | CNPDG3             | CNPDG2             | CNPDG1       | CNPDG0       | 0000          |
| 6670                        | CNCONG                          | 31:16     | —             | —             | —             | —             | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —            | —            | 0000          |
|                             |                                 | 15:0      | ON            | —             | SIDL          | —             | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —            | —            | 0000          |
| 6680                        | CNENG                           | 31:16     | —             | —             | —             | —             | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —            | —            | 0000          |
|                             |                                 | 15:0      | CNIEG15       | CNIEG14       | CNIEG13       | CNIEG12       | —     | —     | CNIEG9       | CNIEG8       | CNIEG7       | CNIEG6       | —    | —    | CNIEG3             | CNIEG2             | CNIEG1       | CNIEG0       | 0000          |
| 6690                        | CNSTATG                         | 31:16     | —             | —             | —             | —             | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —            | —            | 0000          |
|                             |                                 | 15:0      | CN<br>STATG15 | CN<br>STATG14 | CN<br>STATG13 | CN<br>STATG12 | —     | —     | CN<br>STATG9 | CN<br>STATG8 | CN<br>STATG7 | CN<br>STATG6 | —    | —    | CN<br>STATG3       | CN<br>STATG2       | CN<br>STATG1 | CN<br>STATG0 | 0000          |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

- Note** 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.
- 2: This bit is only available on devices without a USB module.

**TABLE 11-16: PORTG REGISTER MAP FOR 64-PIN DEVICES ONLY**

| Virtual Address<br>(BF88_#) | Register<br>Name(s) | Bit Range | Bits  |       |       |       |       |       |              |              |              |              |      |      |                    |                    |      |      | All<br>Resets |
|-----------------------------|---------------------|-----------|-------|-------|-------|-------|-------|-------|--------------|--------------|--------------|--------------|------|------|--------------------|--------------------|------|------|---------------|
|                             |                     |           | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9         | 24/8         | 23/7         | 22/6         | 21/5 | 20/4 | 19/3               | 18/2               | 17/1 | 16/0 |               |
| 6600                        | ANSELG              | 31:16     | —     | —     | —     | —     | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —    | —    | 0000          |
|                             |                     | 15:0      | —     | —     | —     | —     | —     | —     | ANSELG9      | ANSELG8      | ANSELG7      | ANSELG6      | —    | —    | —                  | —                  | —    | —    | 03C0          |
| 6610                        | TRISG               | 31:16     | —     | —     | —     | —     | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —    | —    | 0000          |
|                             |                     | 15:0      | —     | —     | —     | —     | —     | —     | TRISG9       | TRISG8       | TRISG7       | TRISG6       | —    | —    | TRISG3             | TRISG2             | —    | —    | 03CC          |
| 6620                        | PORTG               | 31:16     | —     | —     | —     | —     | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —    | —    | 0000          |
|                             |                     | 15:0      | —     | —     | —     | —     | —     | —     | RG9          | RG8          | RG7          | RG6          | —    | —    | RG3 <sup>(2)</sup> | RG2 <sup>(2)</sup> | —    | —    | xxxx          |
| 6630                        | LATG                | 31:16     | —     | —     | —     | —     | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —    | —    | 0000          |
|                             |                     | 15:0      | —     | —     | —     | —     | —     | —     | LATG9        | LATG8        | LATG7        | LATG6        | —    | —    | LATG3              | LATG2              | —    | —    | xxxx          |
| 6640                        | ODCG                | 31:16     | —     | —     | —     | —     | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —    | —    | 0000          |
|                             |                     | 15:0      | —     | —     | —     | —     | —     | —     | ODCG9        | ODCG8        | ODCG7        | ODCG6        | —    | —    | ODCG3              | ODCG2              | —    | —    | 0000          |
| 6650                        | CNPUG               | 31:16     | —     | —     | —     | —     | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —    | —    | 0000          |
|                             |                     | 15:0      | —     | —     | —     | —     | —     | —     | CNPUG9       | CNPUG8       | CNPUG7       | CNPUG6       | —    | —    | CNPUG3             | CNPUG2             | —    | —    | 0000          |
| 6660                        | CNPDG               | 31:16     | —     | —     | —     | —     | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —    | —    | 0000          |
|                             |                     | 15:0      | —     | —     | —     | —     | —     | —     | CNPDG9       | CNPDG8       | CNPDG7       | CNPDG6       | —    | —    | CNPDG3             | CNPDG2             | —    | —    | 0000          |
| 6670                        | CNCONG              | 31:16     | —     | —     | —     | —     | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —    | —    | 0000          |
|                             |                     | 15:0      | ON    | —     | SIDL  | —     | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —    | —    | 0000          |
| 6680                        | CNENG               | 31:16     | —     | —     | —     | —     | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —    | —    | 0000          |
|                             |                     | 15:0      | —     | —     | —     | —     | —     | —     | CNIEG9       | CNIEG8       | CNIEG7       | CNIEG6       | —    | —    | CNIEG3             | CNIEG2             | —    | —    | 0000          |
| 6690                        | CNSTATG             | 31:16     | —     | —     | —     | —     | —     | —     | —            | —            | —            | —            | —    | —    | —                  | —                  | —    | —    | 0000          |
|                             |                     | 15:0      | —     | —     | —     | —     | —     | —     | CN<br>STATG9 | CN<br>STATG8 | CN<br>STATG7 | CN<br>STATG6 | —    | —    | CN<br>STATG3       | CN<br>STATG2       | —    | —    | 0000          |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.

**2:** This bit is only available on devices without a USB module.

TABLE 11-18: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

| Virtual Address<br>(BF80_#) | Register<br>Name | Bit Range | Bits  |       |       |       |       |       |      |      |      |      |      |      |            |      |      |      | All Resets |
|-----------------------------|------------------|-----------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------------|------|------|------|------------|
|                             |                  |           | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3       | 18/2 | 17/1 | 16/0 |            |
| FBFC                        | RPD15R           | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPD15<3:0> |      |      |      | 0000       |
| FC0C                        | RPE3R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPE3<3:0>  |      |      |      | 0000       |
| FC14                        | RPE5R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPE5<3:0>  |      |      |      | 0000       |
| FC20                        | RPE8R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPE8<3:0>  |      |      |      | 0000       |
| FC24                        | RPE9R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPE9<3:0>  |      |      |      | 0000       |
| FC40                        | RPF0R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPF0<3:0>  |      |      |      | 0000       |
| FC44                        | RPF1R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPF1<3:0>  |      |      |      | 0000       |
| FC48                        | RPF2R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPF2<3:0>  |      |      |      | 0000       |
| FC4C                        | RPF3R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPF3<3:0>  |      |      |      | 0000       |
| FC50                        | RPF4R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPF4<3:0>  |      |      |      | 0000       |
| FC54                        | RPF5R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPF5<3:0>  |      |      |      | 0000       |
| FC58                        | RPF6R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPF6<3:0>  |      |      |      | 0000       |
| FC5C                        | RPF7R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPF7<3:0>  |      |      |      | 0000       |
| FC60                        | RPF8R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPF8<3:0>  |      |      |      | 0000       |
| FC70                        | RPF12R           | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPF12<3:0> |      |      |      | 0000       |
| FC74                        | RPF13R           | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPF13<3:0> |      |      |      | 0000       |
| FC80                        | RPG0R            | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —          | —    | —    | —    | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | RPG0<3:0>  |      |      |      | 0000       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register is not available if the associated RPx function is not present on the device. Refer to the pin table for the specific device to determine availability.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

---

## REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>**: Alarm Repeat Counter Value bits<sup>(3)</sup>

11111111 =Alarm will trigger 256 times

.  
.  
.

00000000 =Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

- Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
- 2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
- 3:** This assumes a CPU read will execute in less than 32 PBCLKs.

|                                                                     |
|---------------------------------------------------------------------|
| <b>Note:</b> This register is reset only on a Power-on Reset (POR). |
|---------------------------------------------------------------------|

## 25.1 Control Registers

**TABLE 25-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP**

| Virtual Address<br>(BF80_#) | Register<br>Name <sup>(1)</sup> | Bit Range | Bits  |       |       |       |       |       |      |      |      |       |      |       |          |      |      |      | All Resets |
|-----------------------------|---------------------------------|-----------|-------|-------|-------|-------|-------|-------|------|------|------|-------|------|-------|----------|------|------|------|------------|
|                             |                                 |           | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6  | 21/5 | 20/4  | 19/3     | 18/2 | 17/1 | 16/0 |            |
| 9800                        | CVRCON                          | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —     | —    | —     | —        | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | ON    | —     | —     | —     | —     | —     | —    | —    | —    | CVROE | CVRR | CVRSS | CVR<3:0> |      |      |      | 0000       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** The register in this table has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

---

## 27.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to enabled or disabled peripherals:

- Control register lock sequence
- Configuration bit select lock

### 27.4.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes.

To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 6. “Oscillator”** (DS60001112) in the *“PIC32 Family Reference Manual”* for details.

### 27.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If PMDLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

TABLE 27-2: PERIPHERAL MODULE DISABLE REGISTER SUMMARY

| Virtual Address<br>(BF80_#) | Register<br>Name | Bit Range | Bits  |       |       |        |        |        |        |                      |      |      |      |       |       |        |        |        | All Resets <sup>(1)</sup> |
|-----------------------------|------------------|-----------|-------|-------|-------|--------|--------|--------|--------|----------------------|------|------|------|-------|-------|--------|--------|--------|---------------------------|
|                             |                  |           | 31/15 | 30/14 | 29/13 | 28/12  | 27/11  | 26/10  | 25/9   | 24/8                 | 23/7 | 22/6 | 21/5 | 20/4  | 19/3  | 18/2   | 17/1   | 16/0   |                           |
| F240                        | PMD1             | 31:16     | —     | —     | —     | —      | —      | —      | —      | —                    | —    | —    | —    | —     | —     | —      | —      | —      | 0000                      |
|                             |                  | 15:0      | —     | —     | —     | CVRMD  | —      | —      | —      | CTMUMD               | —    | —    | —    | —     | —     | —      | —      | AD1MD  | 0000                      |
| F250                        | PMD2             | 31:16     | —     | —     | —     | —      | —      | —      | —      | —                    | —    | —    | —    | —     | —     | —      | —      | —      | 0000                      |
|                             |                  | 15:0      | —     | —     | —     | —      | —      | —      | —      | —                    | —    | —    | —    | —     | —     | CMP3MD | CMP2MD | CMP1MD | 0000                      |
| F260                        | PMD3             | 31:16     | —     | —     | —     | —      | —      | —      | —      | —                    | —    | —    | —    | OC5MD | OC4MD | OC3MD  | OC2MD  | OC1MD  | 0000                      |
|                             |                  | 15:0      | —     | —     | —     | —      | —      | —      | —      | —                    | —    | —    | —    | IC5MD | IC4MD | IC3MD  | IC2MD  | IC1MD  | 0000                      |
| F270                        | PMD4             | 31:16     | —     | —     | —     | —      | —      | —      | —      | —                    | —    | —    | —    | —     | —     | —      | —      | —      | 0000                      |
|                             |                  | 15:0      | —     | —     | —     | —      | —      | —      | —      | —                    | —    | —    | —    | T5MD  | T4MD  | T3MD   | T2MD   | T1MD   | 0000                      |
| F280                        | PMD5             | 31:16     | —     | —     | —     | CAN1MD | —      | —      | —      | USBMD <sup>(4)</sup> | —    | —    | —    | —     | —     | —      | I2C1MD | I2C1MD | 0000                      |
|                             |                  | 15:0      | —     | —     | —     | —      | SPI4MD | SPI3MD | SPI2MD | SPI1MD               | —    | —    | —    | U5MD  | U4MD  | U3MD   | U2MD   | U1MD   | 0000                      |
| F290                        | PMD6             | 31:16     | —     | —     | —     | —      | —      | —      | —      | —                    | —    | —    | —    | —     | —     | —      | —      | PMPMD  | 0000                      |
|                             |                  | 15:0      | —     | —     | —     | —      | —      | —      | —      | —                    | —    | —    | —    | —     | —     | —      | REFOMD | RTCCMD | 0000                      |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This bit is only available on devices with a USB module.

## 29.0 INSTRUCTION SET

The PIC32MX1XX/2XX/5XX 64/100-pin family instruction set complies with the MIPS32® Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

|                                                                                                                                                                                        |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p><b>Note:</b> Refer to “MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set” at <a href="http://www.imgtec.com">www.imgtec.com</a> for more information.</p> |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

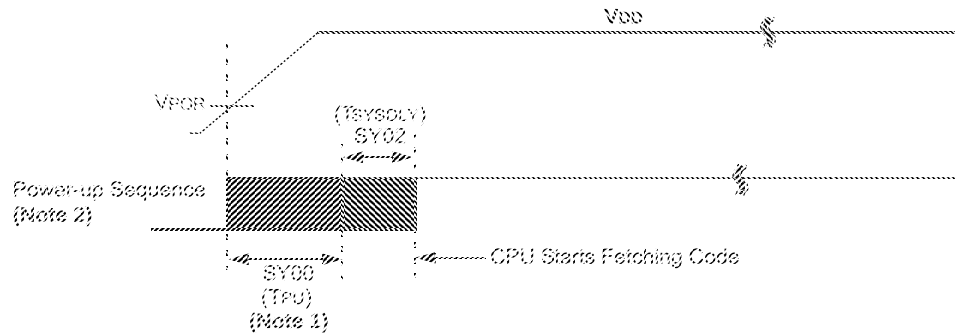


# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**FIGURE 31-4: POWER-ON RESET TIMING CHARACTERISTICS**

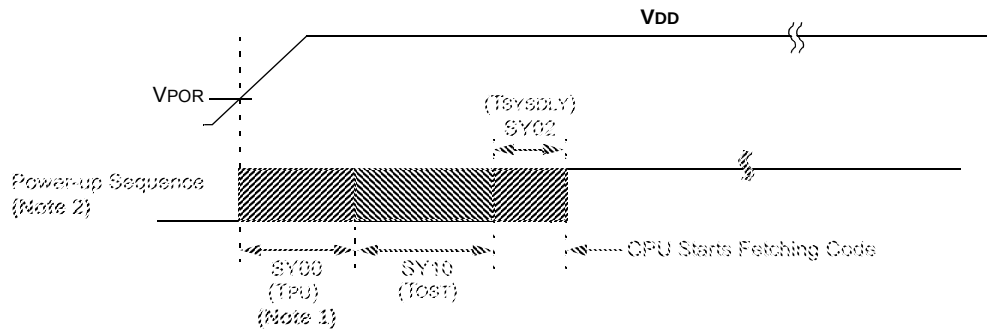
*Internal Voltage Regulator Enabled*

*Clock Sources = {FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC}*



*Internal Voltage Regulator Enabled*

*Clock Sources = {HS, HSPLL, XT, XTPLL and Sosc}*



**Note 1:** The power-up period will be extended if the power-up sequence completes before the device exits from BOR ( $V_{DD} < V_{DDMIN}$ ).

**2:** Includes interval voltage regulator stabilization delay.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## 32.0 50 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX/5XX 64/100-pin Family electrical characteristics for devices operating at 50 MHz.

The specifications for 50 MHz are identical to those shown in **Section 31.0 “40 MHz Electrical Characteristics”**, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter “M”, which denotes 50 MHz operation. For example, parameter DC29a in **Section 31.0 “40 MHz Electrical Characteristics”**, is the up to 40 MHz operation equivalent for MDC29a.

Absolute maximum ratings for the PIC32MX1XX/2XX/5XX 64/100-pin Family 50 MHz devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

### Absolute Maximum Ratings

(See Note 1)

|                                                                                            |                           |
|--------------------------------------------------------------------------------------------|---------------------------|
| Ambient temperature under bias .....                                                       | -40°C to +85°C            |
| Storage temperature .....                                                                  | -65°C to +150°C           |
| Voltage on VDD with respect to VSS .....                                                   | -0.3V to +4.0V            |
| Voltage on any pin that is not 5V tolerant, with respect to VSS ( <b>Note 3</b> ) .....    | -0.3V to (VDD + 0.3V)     |
| Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.3V ( <b>Note 3</b> ) ..... | -0.3V to +5.5V            |
| Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V ( <b>Note 3</b> ) ..... | -0.3V to +3.6V            |
| Voltage on D+ or D- pin with respect to VUSB3V3 .....                                      | -0.3V to (VUSB3V3 + 0.3V) |
| Voltage on VBUS with respect to VSS .....                                                  | -0.3V to +5.5V            |
| Maximum current out of VSS pin(s) .....                                                    | 300 mA                    |
| Maximum current into VDD pin(s) ( <b>Note 2</b> ) .....                                    | 300 mA                    |
| Maximum output current sunk by any I/O pin .....                                           | 15 mA                     |
| Maximum output current sourced by any I/O pin .....                                        | 15 mA                     |
| Maximum current sunk by all ports .....                                                    | 200 mA                    |
| Maximum current sourced by all ports ( <b>Note 2</b> ) .....                               | 200 mA                    |

**Note 1:** Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

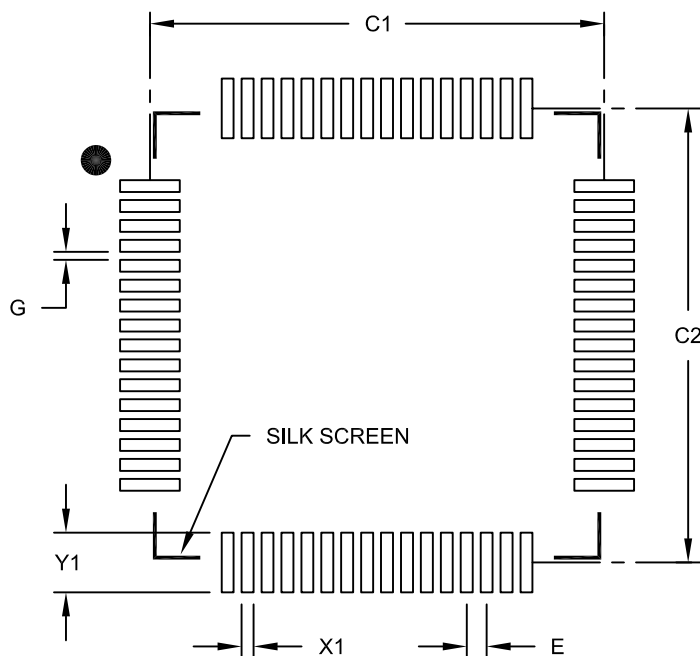
**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 32-2).

**3:** See the “**Device Pin Tables**” section for the 5V tolerant pins.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits         | Units | MILLIMETERS |          |      |
|--------------------------|-------|-------------|----------|------|
|                          |       | MIN         | NOM      | MAX  |
| Contact Pitch            | E     |             | 0.50 BSC |      |
| Contact Pad Spacing      | C1    |             | 11.40    |      |
| Contact Pad Spacing      | C2    |             | 11.40    |      |
| Contact Pad Width (X64)  | X1    |             |          | 0.30 |
| Contact Pad Length (X64) | Y1    |             |          | 1.50 |
| Distance Between Pads    | G     | 0.20        |          |      |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## INDEX

### A

|                                                 |          |
|-------------------------------------------------|----------|
| AC Characteristics .....                        | 321, 356 |
| 10-Bit Conversion Rate Parameters .....         | 343      |
| ADC Specifications .....                        | 341      |
| Analog-to-Digital Conversion Requirements ..... | 344      |
| EJTAG Timing Requirements .....                 | 352      |
| Internal FRC Accuracy .....                     | 323      |
| Internal RC Accuracy .....                      | 323      |
| OTG Electrical Specifications .....             | 350      |
| Parallel Master Port Read Requirements .....    | 349      |
| Parallel Master Port Write .....                | 350      |
| Parallel Master Port Write Requirements .....   | 350      |
| Parallel Slave Port Requirements .....          | 348      |
| PLL Clock Timing .....                          | 323      |
| Analog-to-Digital Converter (ADC) .....         | 231      |

### B

|                                                      |     |
|------------------------------------------------------|-----|
| Block Diagrams .....                                 |     |
| ADC Module .....                                     | 231 |
| Comparator I/O Operating Modes .....                 | 271 |
| Comparator Voltage Reference .....                   | 275 |
| Connections for On-Chip Voltage Regulator .....      | 302 |
| CPU .....                                            | 35  |
| CTMU Configurations .....                            |     |
| Time Measurement .....                               | 279 |
| DMA .....                                            | 85  |
| Input Capture .....                                  | 173 |
| Inter-Integrated Circuit (I <sup>2</sup> C) .....    | 192 |
| Interrupt Controller .....                           | 53  |
| JTAG Programming, Debugging and Trace Ports .....    | 302 |
| Output Compare Module .....                          | 177 |
| PIC32 CAN Module .....                               | 243 |
| PMP Pinout and Connections to External Devices ..... | 207 |
| Reset System .....                                   | 69  |
| RTCC .....                                           | 221 |
| SPI Module .....                                     | 181 |
| Timer1 .....                                         | 159 |
| Timer2/3/4/5 (16-Bit) .....                          | 163 |
| Typical Multiplexed Port Structure .....             | 129 |
| UART .....                                           | 199 |
| WDT and Power-up Timer .....                         | 169 |
| Brown-out Reset (BOR) .....                          |     |
| and On-Chip Voltage Regulator .....                  | 302 |

### C

|                                              |          |
|----------------------------------------------|----------|
| C Compilers .....                            |          |
| MPLAB C18 .....                              | 306      |
| Charge Time Measurement Unit. See CTMU. .... |          |
| Clock Diagram .....                          | 74       |
| Comparator .....                             |          |
| Specifications .....                         | 319, 320 |
| Comparator Module .....                      | 271      |
| Comparator Voltage Reference (CVref) .....   | 275      |
| Configuration Bit .....                      | 291      |
| Configuring Analog Port Pins .....           | 130      |
| Controller Area Network (CAN) .....          | 243      |
| CPU .....                                    |          |
| Architecture Overview .....                  | 36       |
| Coprocessor 0 Registers .....                | 37       |
| Core Exception Types .....                   | 38       |
| EJTAG Debug Support .....                    | 38       |
| Power Management .....                       | 38       |
| CPU Module .....                             | 25, 35   |

### CTMU

|                                            |     |
|--------------------------------------------|-----|
| Registers .....                            | 281 |
| Customer Change Notification Service ..... | 377 |
| Customer Notification Service .....        | 377 |
| Customer Support .....                     | 377 |

### D

|                                              |     |
|----------------------------------------------|-----|
| DC and AC Characteristics .....              |     |
| Graphs and Tables .....                      | 359 |
| DC Characteristics .....                     | 310 |
| I/O Pin Input Specifications .....           | 315 |
| I/O Pin Output Specifications .....          | 316 |
| Idle Current (I <sub>IDLE</sub> ) .....      | 313 |
| Power-Down Current (I <sub>PD</sub> ) .....  | 314 |
| Program Memory .....                         | 318 |
| Temperature and Voltage Specifications ..... | 311 |
| DC Characteristics (50 MHz) .....            | 354 |
| Idle Current (I <sub>IDLE</sub> ) .....      | 355 |
| Power-Down Current (I <sub>PD</sub> ) .....  | 355 |
| Development Support .....                    | 305 |
| Direct Memory Access (DMA) Controller .....  | 85  |

### E

|                                           |     |
|-------------------------------------------|-----|
| Electrical Characteristics .....          | 309 |
| 50 MHz .....                              | 353 |
| Errata .....                              | 9   |
| External Clock .....                      |     |
| Timer1 Timing Requirements .....          | 327 |
| Timer2, 3, 4, 5 Timing Requirements ..... | 328 |
| Timing Requirements .....                 | 322 |
| External Clock (50 MHz) .....             |     |
| Timing Requirements .....                 | 356 |

### F

|                            |    |
|----------------------------|----|
| Flash Program Memory ..... | 63 |
| RTSP Operation .....       | 63 |

### H

|                                 |         |
|---------------------------------|---------|
| High Voltage Detect (HVD) ..... | 71, 302 |
|---------------------------------|---------|

### I

|                                                   |     |
|---------------------------------------------------|-----|
| I/O Ports .....                                   | 129 |
| Parallel I/O (PIO) .....                          | 130 |
| Write/Read Timing .....                           | 130 |
| Input Change Notification .....                   | 130 |
| Instruction Set .....                             | 303 |
| Inter-Integrated Circuit (I <sup>2</sup> C) ..... | 191 |
| Internal Voltage Reference Specifications .....   | 320 |
| Internet Address .....                            | 377 |
| Interrupt Controller .....                        | 53  |
| IRG, Vector and Bit Location .....                | 54  |

### M

|                                                         |     |
|---------------------------------------------------------|-----|
| Memory Maps .....                                       |     |
| Devices with 128 KB of Program Memory .....             | 41  |
| Devices with 256 KB of Program Memory .....             | 42  |
| Devices with 512 KB of Program Memory .....             | 43  |
| Devices with 64 KB of Program Memory .....              | 40  |
| Memory Organization .....                               | 39  |
| Layout .....                                            | 39  |
| Microchip Internet Web Site .....                       | 377 |
| MPASM Assembler .....                                   | 306 |
| MPLAB ASM30 Assembler, Linker, Librarian .....          | 306 |
| MPLAB Integrated Development Environment Software ..... | 305 |

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

---

## THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at [www.microchip.com](http://www.microchip.com). This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

## CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at [www.microchip.com](http://www.microchip.com). Under "Support", click on "Customer Change Notification" and follow the registration instructions.

## CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

**Technical support is available through the web site at: <http://microchip.com/support>**