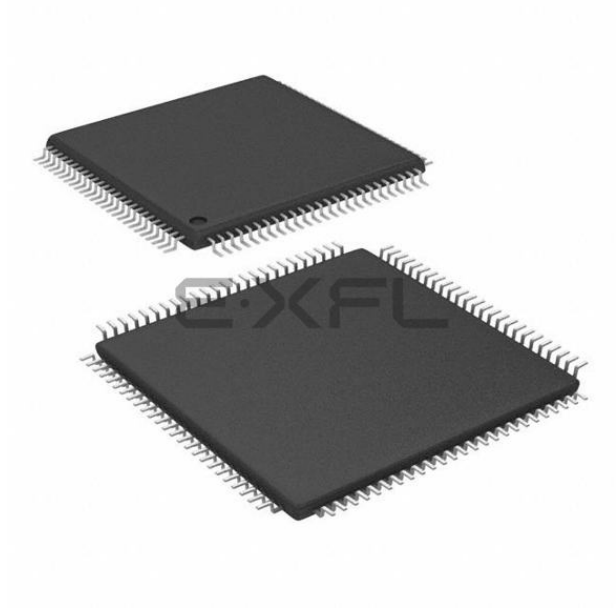

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CANbus, I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx530f128l-i-pf

TABLE 5: PIN NAMES FOR 100-PIN USB DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MX230F128L
PIC32MX530F128L
PIC32MX250F256L
PIC32MX550F256L
PIC32MX270F512L
PIC32MX570F512L

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN28/RG15	36	VSS
2	VDD	37	VDD
3	AN22/RPE5/PMD5/RE5	38	TCK/CTED2/RA1
4	AN23/PMD6/RE6	39	AN34/RPF13/SCK3/RF13
5	AN27/PMD7/RE7	40	AN35/RPF12/RF12
6	AN29/RPC1/RC1	41	AN12/PMA11/RB12
7	AN30/RPC2/RC2	42	AN13/PMA10/RB13
8	AN31/RPC3/RC3	43	AN14/RPB14/CTED5/PMA1/RB14
9	RPC4/CTED7/RC4	44	AN15/RPB15/OCFB/CTED6/PMA0/RB15
10	AN16/C1IND/RPG6/SCK2/PMA5/RG6	45	VSS
11	AN17/C1INC/RPG7/PMA4/RG7	46	VDD
12	AN18/C2IND/RPG8/PMA3/RG8	47	AN36/RPD14/RD14
13	$\overline{\text{MCLR}}$	48	AN37/RPD15/SCK4/RD15
14	AN19/C2INC/RPG9/PMA2/RG9	49	RPF4/PMA9/RF4
15	VSS	50	RPF5/PMA8/RF5
16	VDD	51	USBID/RPF3/RF3
17	TMS/CTED1/RA0	52	AN38/RPF2/RF2
18	AN32/RPE8/RE8	53	AN39/RPF8/RF8
19	AN33/RPE9/RE9	54	VBUS
20	AN5/C1INA/RPB5/VBUSON/RB5	55	VUSB3V3
21	AN4/C1INB/RB4	56	D-
22	PGED3/AN3/C2INA/RPB3/RB3	57	D+
23	PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2	58	SCL2/RA2
24	PGEC1/AN1/RPB1/CTED12/RB1	59	SDA2/RA3
25	PGED1/AN0/RPB0/RB0	60	TDI/CTED9/RA4
26	PGEC2/AN6/RPB6/RB6	61	TDO/RA5
27	PGED2/AN7/RPB7/CTED3/RB7	62	VDD
28	VREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	VSS
31	AVSS	66	RPA14/SCL1/RA14
32	AN8/RPB8/CTED10/RB8	67	RPA15/SDA1/RA15
33	AN9/RPB9/CTED4/RB9	68	RPD8/RTCC/RD8
34	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	69	RPD9/RD9
35	AN11/PMA12/RB11	70	RPD10/SCK1/PMA15/RD10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin microcontrollers provide 4 GB of unified virtual memory address space. All memory regions, including program, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX/5XX 64/100-pin devices to execute from data memory.

The key features include:

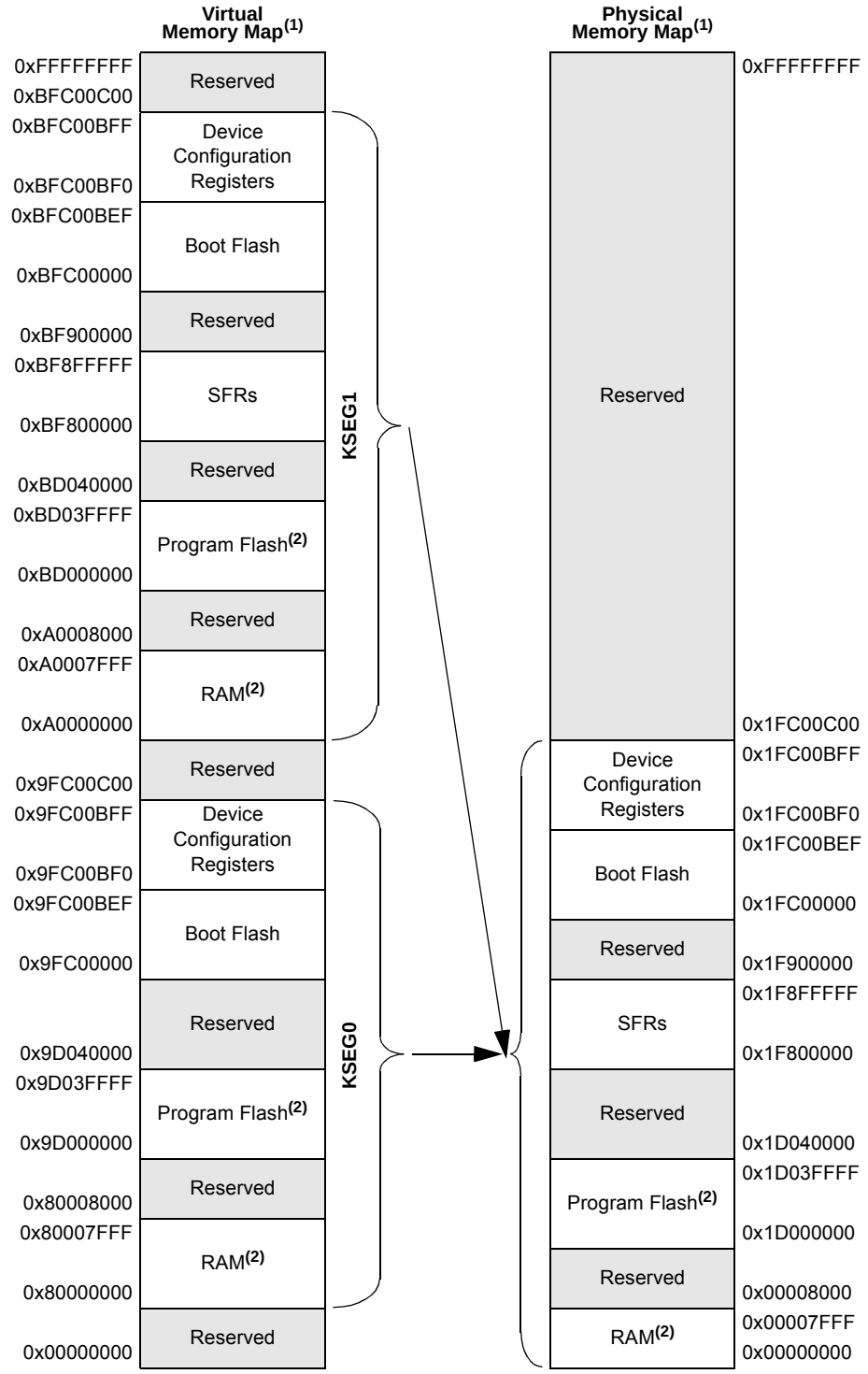
- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/ KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit

4.1 Memory Layout

PIC32MX1XX/2XX/5XX 64/100-pin microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX/5XX 64/ 100-pin devices are illustrated in Figure 4-1 through Figure 4-4.

FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 256 KB OF PROGRAM MEMORY + 32 KB RAM



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

5.1 Interrupts Control Registers

TABLE 5-2: INTERRUPT REGISTER MAP

Virtual Address (BF88_#)	Register Name(3)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	FCEIF	RTCCIF	FSCMIF	AD1IF	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
		15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	U3RXIF	U3EIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	SPI2RXIF	SPI2EIF	PMPEIF	PMPIF	CNGIF	CNFIF	CNEIF	0000
		15:0	CNDIF	CNCIF	CNBIF	CNAIF	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1TXIF	SPI1RXIF	SPI1EIF	USBIF(2)	CMP2IF	CMP1IF	0000
1050	IFS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SPI4TXIF(1)	SPI4RXIF(1)	SPI4EIF(1)	SPI3TXIF	0000
		15:0	SPI3RXIF	SPI3EIF	CANIF	CMP3IF	DMA3IF	DMA2IF	DMA1IF	DMA0IF	CTMUIF	U5TXIF(1)	U5RXIF(1)	U5EIF(1)	U4TXIF	U4RXIF	U4EIF	U3TXIF	0000
1060	IEC0	31:16	FCEIE	RTCCIE	FSCMIE	AD1IE	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
		15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	U3RXIE	U3EIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2TXIE	SPI2RXIE	SPI2EIE	PMPEIE	PMPIE	CNGIE	CNFIE	CNEIE	0000
		15:0	CNDIE	CNCIE	CNBIE	CNAIE	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1TXIE	SPI1RXIE	SPI1EIE	USBIE(2)	CMP2IE	CMP1IE	0000
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE	CTMUIE	U5TXIE(1)	U5RXIE(1)	U5EIE(1)	U4TXIE	U4RXIE	U4EIE	U3TXIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This bit is only available on 100-pin devices.

2: This bit is only implemented on devices with a USB module.

3: With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

4: This register does not have associated CLR, SET, and INV registers.

5: This bit is only implemented on devices with a CAN module.

8.1 Control Registers

TABLE 8-1: OSCILLATOR CONFIGURATION REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F000	OSCCON	31:16	—	—	PLLODIV<2:0>			FRCDIV<2:0>			—	SOSCRDY	PBDIVRDY	PBDIV<1:0>		PLLMULT<2:0>			x1xx(2)
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	ULOCK	SLOCK	SLPEN	CF	UFRCEN(3)	SOSCEN	OSWEN	xxxx(2)
F010	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000
F020	REFOCON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
F030	REFOTRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

3: This bit is only available on devices with a USB module.

REGISTER 10-21: U1EP0-U1EP15: USB ENDPOINT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPD:** Low-Speed Direct Connection Enable bit (Host mode and U1EP0 only)
1 = Direct connection to a low-speed device enabled
0 = Direct connection to a low-speed device disabled; hub required with PRE_PID

bit 6 **RETRYDIS:** Retry Disable bit (Host mode and U1EP0 only)
1 = Retry NAKed transactions disabled
0 = Retry NAKed transactions enabled; retry done in hardware

bit 5 **Unimplemented:** Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit
If EPTXEN = 1 and EPRXEN = 1:
1 = Disable Endpoint n from Control transfers; only TX and RX transfers allowed
0 = Enable Endpoint n for Control (SETUP) transfers; TX and RX transfers also allowed
Otherwise, this bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit
1 = Endpoint n receive enabled
0 = Endpoint n receive disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit
1 = Endpoint n transmit enabled
0 = Endpoint n transmit disabled

bit 1 **EPSTALL:** Endpoint Stall Status bit
1 = Endpoint n was stalled
0 = Endpoint n was not stalled

bit 0 **EPHSHK:** Endpoint Handshake Enable bit
1 = Endpoint Handshake enabled
0 = Endpoint Handshake disabled (typically used for isochronous endpoints)

NOTES:

TABLE 19-1: UART1 THROUGH UART5 REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6440	U3BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
6600	U4MODE(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6610	U4STA(1)	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	FFFF
6620	U4TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6630	U4RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6640	U4BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
6800	U5MODE(1,2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6810	U5STA(1,2)	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	FFFF
6820	U5TXREG(1,2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6830	U5RXREG(1,2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6840	U5BRG(1,2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

2: This register is only available on 100-pin devices.

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/PMWR port enabled
0 = PMRD/PMWR port disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits(2)
11 = Reserved
10 = PMCS1 and PMCS2 function as Chip Select
01 = PMCS1 functions as address bit 14; PMCS2 functions as Chip Select
00 = PMCS1 and PMCS2 function as address bits 14 and 15, respectively

bit 5 **ALP:** Address Latch Polarity bit(2)
1 = Active-high (PMALL and PMALH)
0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

bit 4 **CS2P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS2)
0 = Active-low ($\overline{\text{PMCS2}}$)

bit 3 **CS1P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS1)
0 = Active-low ($\overline{\text{PMCS1}}$)

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Write strobe active-high (PMWR)
0 = Write strobe active-low ($\overline{\text{PMWR}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Read Strobe active-high (PMRD)
0 = Read Strobe active-low ($\overline{\text{PMRD}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

21.1 Control Registers

TABLE 21-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>										0000
		15:0	ON	—	SIDL	—	—	—	—	—	RTSECSEL	RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0210	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>				ARPT<7:0>								0000
0220	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0230	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>				xxxx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx00
0240	ALRMTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0250	ALRMDATE	31:16	—	—	—	—	—	—	—	—	MONTH10<3:0>				MONTH01<3:0>				00xx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits(3)

11111111 =Alarm will trigger 256 times

•

•

•

00000000 =Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note:	This register is reset only on a Power-on Reset (POR).

REGISTER 22-4: AD1CHS: ADC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NB	—	CH0SB<5:0>					
23:16	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NA	—	CH0SA<5:0>					
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **CH0NB:** Negative Input Select bit for Sample B
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL

bit 30 **Unimplemented:** Read as '0'

bit 29-24 **CH0SB<5:0>:** Positive Input Select bits for Sample B
For 64-pin devices:
011110 = Channel 0 positive input is Open(1)
011101 = Channel 0 positive input is CTMU temperature sensor (CTMUT)(2)
011100 = Channel 0 positive input is IVREF(3)
011011 = Channel 0 positive input is AN27
•
•
•
000001 = Channel 0 positive input is AN1
000000 = Channel 0 positive input is AN0
For 100-pin devices:
110010 = Channel 0 positive input is Open(1)
110001 = Channel 0 positive input is CTMU temperature sensor (CTMUT)(2)
110000 = Channel 0 positive input is IVREF(3)
101111 = Channel 0 positive input is AN47
•
•
•
0000001 = Channel 0 positive input is AN1
0000000 = Channel 0 positive input is AN0

bit 23 **CH0NA:** Negative Input Select bit for Sample A Multiplexer Setting(3)
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL

bit 22 **Unimplemented:** Read as '0'

Note 1: This selection is only used with CTMU capacitive and time measurement.
2: See **Section 26.0 "Charge Time Measurement Unit (CTMU)"** for more information.
3: Internal precision 1.2V reference. See **Section 24.0 "Comparator"** for more information.

REGISTER 23-10: C1FLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)

bit 20-16 **FSEL2<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 15 **FLTEN1:** Filter 1 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL1<1:0>:** Filter 1 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL1<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN0:** Filter 0 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL0<1:0>:** Filter 0 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL0<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

27.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

Note 1: Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a POSC of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.

2: Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from POSC to LPRC just prior to entering Sleep in order to save power. No oscillator start-up delay would be applied when exiting Idle. However, when switching back to POSC, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

27.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The peripheral bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

REGISTER 28-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	—	—	—	—	—	FPLLODIV<2:0>		
15:8	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	UPLLEN(1)	—	—	—	—	UPLLIDIV<2:0>(1)		
7:0	r-1	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P
	—	FPLLMUL<2:0>			—	FPLLIDIV<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLLODIV<2:0>:** Default PLL Output Divisor bits
- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit(1)
- 1 = Disable and bypass USB PLL
- 0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLLIDIV<2:0>:** USB PLL Input Divider bits(1)
- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits
- 111 = 24x multiplier
- 110 = 21x multiplier
- 101 = 20x multiplier
- 100 = 19x multiplier
- 011 = 18x multiplier
- 010 = 17x multiplier
- 001 = 16x multiplier
- 000 = 15x multiplier

bit 3 **Reserved:** Write '1'

Note 1: This bit is available on PIC32MX2XX/5XX devices only.

31.1 DC Characteristics

TABLE 31-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)(1)	Temp. Range (in °C)	Max. Frequency
			PIC32MX1XX/2XX/5XX 64/100-pin Family
DC5	VBOR-3.6V	-40°C to +105°C	40 MHz

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for BOR values.

TABLE 31-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
V-temp Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+105	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – S IOH) I/O Pin Power Dissipation: I/O = S (({VDD – VOH} x IOH) + S (VOL x IOL))	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 31-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 64-pin QFN	θJA	28	—	°C/W	**1**
Package Thermal Resistance, 64-pin TQFP, 10 mm x 10 mm	θJA	55	—	°C/W	**1**
Package Thermal Resistance, 100-pin TQFP, 12 mm x 12 mm	θJA	52	—	°C/W	**1**
Package Thermal Resistance, 100-pin TQFP, 14 mm x 14 mm	θJA	50	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 31-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Parameter No.	**Typical(2)**	**Max.**	**Units**	**Conditions**		
Idle Current (IIDLE): Core Off, Clock on Base Current (Notes 1, 4)						
DC30a	1.5	5	mA	4 MHz **(Note 3)**		
DC31a	3	8	mA	10 MHz		
DC32a	5	12	mA	20 MHz **(Note 3)**		
DC33a	6.5	15	mA	30 MHz **(Note 3)**		
DC34a	8	20	mA	40 MHz		
DC37a	75	100	µA	-40°C	3.3V	LPRC (31 kHz) **(Note 3)**
DC37b	180	250	µA	+25°C		
DC37c	280	380	µA	+85°C		

Note 1: The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

4: IIDLE electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

TABLE 31-34: ADC MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions (see Note 5): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
ADC Accuracy – Measurements with Internal VREF+/VREF-							
AD20d	Nr	Resolution	10 data bits			bits	**(Note 3)**
AD21d	INL	Integral Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)**
AD22d	DNL	Differential Non-linearity	> -1	—	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Notes 2,3)**
AD23d	GERR	Gain Error	> -4	—	< 4	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)**
AD24d	EOFF	Offset Error	> -2	—	< 2	Lsb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)**
AD25d	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance							
AD32b	SINAD	Signal to Noise and Distortion	55	58.5	—	dB	**(Notes 3,4)**
AD34b	ENOB	Effective Number of bits	9.0	9.5	—	bits	**(Notes 3,4)**

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 31-36: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period(2)	65	—	—	ns	See Table 31-35
Conversion Rate							
AD55	TCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate (Sampling Speed)	—	—	1000	ksps	AVDD = 3.0V to 3.6V
			—	—	400	ksps	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	1 TAD	—	—	—	TSAMP must be ≥ 132 ns
Timing Parameters							
AD60	TPCS	Conversion Start from Sample Trigger(3)	—	1.0 TAD	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD	—	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1)(3)	—	0.5 TAD	—	—	—
AD63	TDPU	Time to Stabilize Analog Stage from ADC Off to ADC On(3)	—	—	2	μs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: Characterized by design but not tested.

4: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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