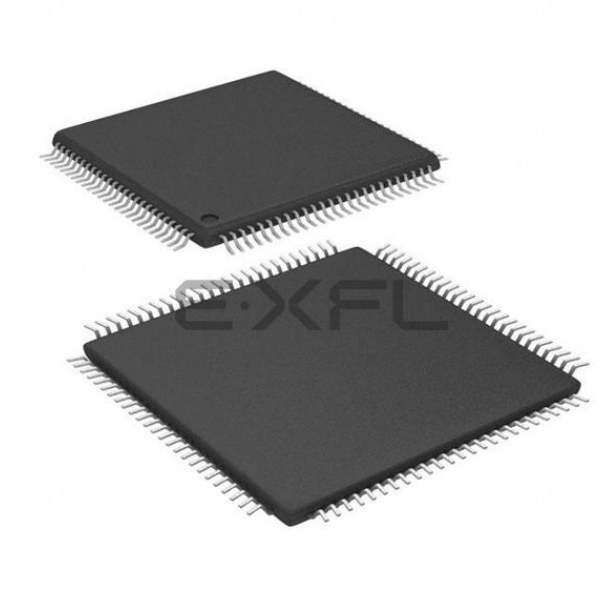

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CANbus, I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx530f128l-i-pt

TABLE 4: PIN NAMES FOR 100-PIN GENERAL PURPOSE DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MX130F128L
PIC32MX150F256L
PIC32MX170F512L

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN28/RG15	36	VSS
2	VDD	37	VDD
3	AN22/RPE5/PMD5/RE5	38	TCK/CTED2/RA1
4	AN23/PMD6/RE6	39	AN34/RPF13/SCK3/RF13
5	AN27/PMD7/RE7	40	AN35/RPF12/RF12
6	AN29/RPC1/RC1	41	AN12/PMA11/RB12
7	AN30/RPC2/RC2	42	AN13/PMA10/RB13
8	AN31/RPC3/RC3	43	AN14/RPB14/CTED5/PMA1/RB14
9	RPC4/CTED7/RC4	44	AN15/RPB15/OCFB/CTED6/PMA0/RB15
10	AN16/C1IND/RPG6/SCK2/PMA5/RG6	45	VSS
11	AN17/C1INC/RPG7/PMA4/RG7	46	VDD
12	AN18/C2IND/RPG8/PMA3/RG8	47	AN36/RPD14/RD14
13	$\overline{\text{MCLR}}$	48	AN37/RPD15/SCK4/RD15
14	AN19/C2INC/RPG9/PMA2/RG9	49	RPF4/PMA9/RF4
15	VSS	50	RPF5/PMA8/RF5
16	VDD	51	RPF3/RF3
17	TMS/CTED1/RA0	52	AN38/RPF2/RF2
18	AN32/RPE8/RE8	53	AN39/RPF8/RF8
19	AN33/RPE9/RE9	54	RPF7/RF7
20	AN5/C1INA/RPB5/RB5	55	RPF6/SCK1/INT0/RF6
21	AN4/C1INB/RB4	56	SDA1/RG3
22	PGED3/AN3/C2INA/RPB3/RB3	57	SCL1/RG2
23	PGEC3/AN2/CTCMP/C2INB/RPB2/CTED13/RB2	58	SCL2/RA2
24	PGEC1/AN1/RPB1/CTED12/RB1	59	SDA2/RA3
25	PGED1/AN0/RPB0/RB0	60	TDI/CTED9/RA4
26	PGEC2/AN6/RPB6/RB6	61	TDO/RA5
27	PGED2/AN7/RPB7/CTED3/RB7	62	VDD
28	VREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	VSS
31	AVSS	66	RPA14/RA14
32	AN8/RPB8/CTED10/RB8	67	RPA15/RA15
33	AN9/RPB9/CTED4/RB9	68	RPD8/RTCC/RD8
34	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	69	RPD9/RD9
35	AN11/PMA12/RB11	70	RPD10/PMA15/RD10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP			
PMA2	8	14	O	TTL/ST	Parallel Master Port data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMA3	6	12	O	TTL/ST	
PMA4	5	11	O	TTL/ST	
PMA5	4	10	O	TTL/ST	
PMA6	16	29	O	TTL/ST	
PMA7	22	28	O	TTL/ST	
PMA8	32	50	O	TTL/ST	
PMA9	31	49	O	TTL/ST	
PMA10	28	42	O	TTL/ST	
PMA11	27	41	O	TTL/ST	
PMA12	24	35	O	TTL/ST	
PMA13	23	34	O	TTL/ST	
PMA14	45	71	O	TTL/ST	
PMA15	44	70	O	TTL/ST	
PMCS1	45	71	O	TTL/ST	Parallel Master Port data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMCS2	44	70	O	TTL/ST	
PMD0	60	93	I/O	TTL/ST	
PMD1	61	94	I/O	TTL/ST	
PMD2	62	98	I/O	TTL/ST	
PMD3	63	99	I/O	TTL/ST	
PMD4	64	100	I/O	TTL/ST	
PMD5	1	3	I/O	TTL/ST	
PMD6	2	4	I/O	TTL/ST	
PMD7	3	5	I/O	TTL/ST	
PMD8	—	90	I/O	TTL/ST	
PMD9	—	89	I/O	TTL/ST	
PMD10	—	88	I/O	TTL/ST	
PMD11	—	87	I/O	TTL/ST	
PMD12	—	79	I/O	TTL/ST	
PMD13	—	80	I/O	TTL/ST	
PMD14	—	83	I/O	TTL/ST	
PMD15	—	84	I/O	TTL/ST	
PMRD	53	82	O	—	Parallel Master Port Read Strobe
PMWR	52	81	O	—	Parallel Master Port Write Strobe
V_{BUS} **(2)**	34	54	I	Analog	USB Bus Power Monitor

Legend: CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

2.10 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-8, Figure 2-9, and Figure 2-10.

FIGURE 2-8: CAPACITIVE TOUCH SENSING WITH GRAPHICS APPLICATION

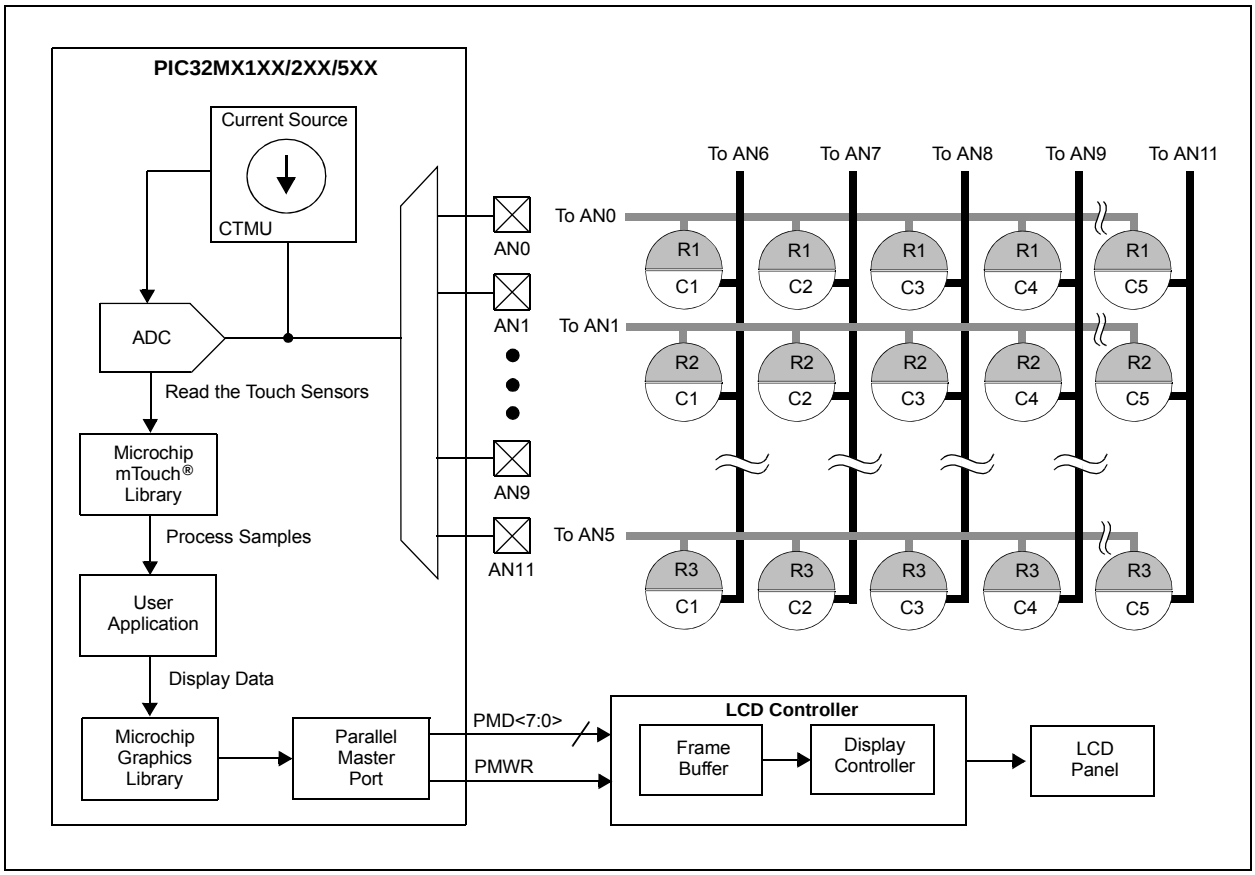


FIGURE 2-9: AUDIO PLAYBACK APPLICATION

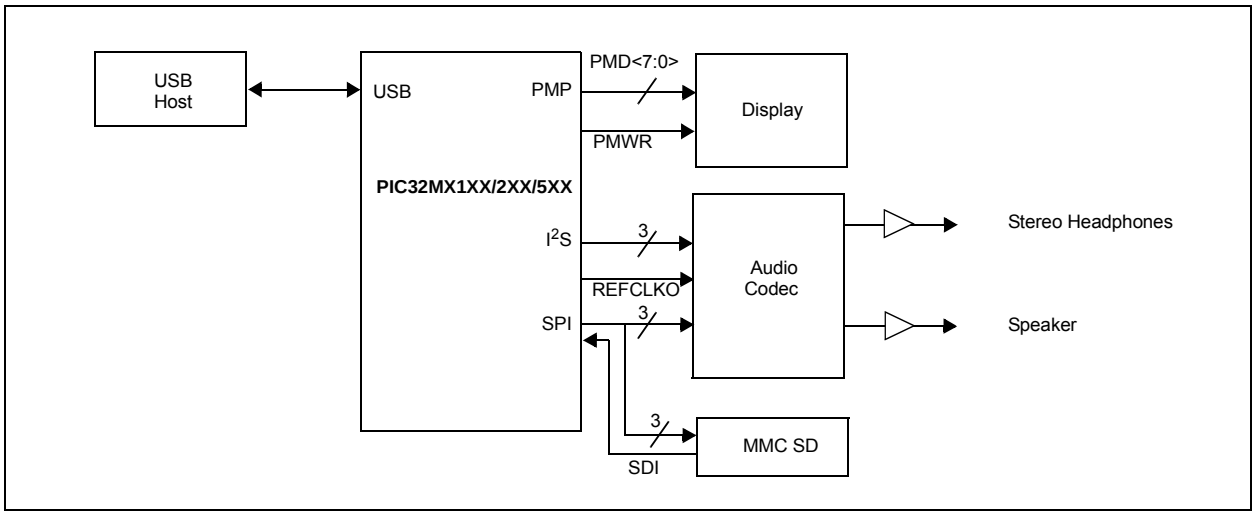
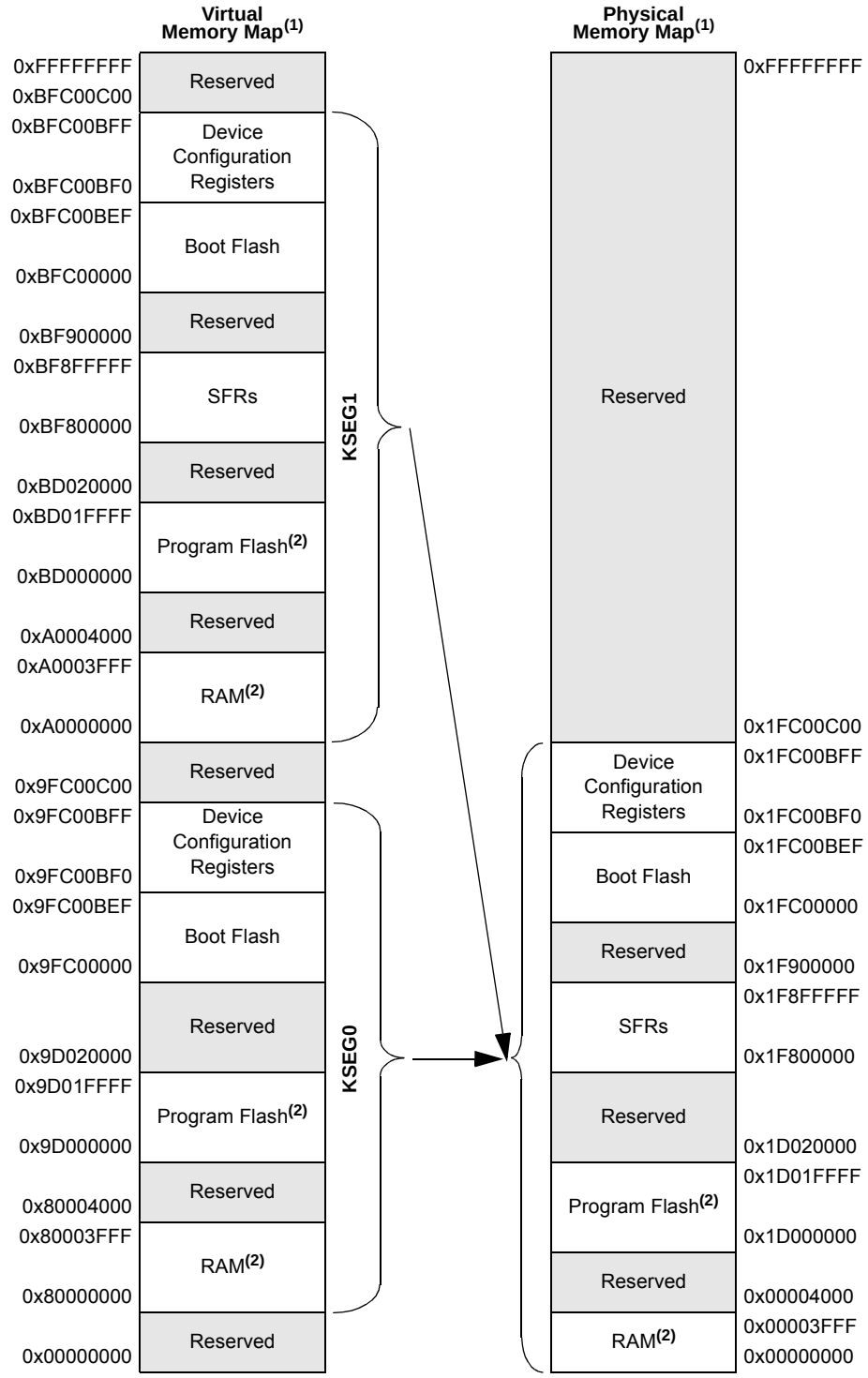


FIGURE 4-2: MEMORY MAP FOR DEVICES WITH 128 KB OF PROGRAM MEMORY + 16 KB RAM



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
Interrupt Controller	0xBF88	0x1000
Bus Matrix		0x2000
DMA		0x3000
USB		0x5000
PORTA-PORTG		0x6000
CAN1		0xB000
Watchdog Timer	0xBF80	0x0000
RTCC		0x0200
Timer1-Timer5		0x0600
IC1-IC5		0x2000
OC1-OC5		0x3000
I2C1-I2C2		0x5000
SPI1-SPI4		0x5800
UART1-UART5		0x6000
PMP		0x7000
ADC1		0x9000
DAC		0x9800
Comparator 1, 2, 3		0xA000
Oscillator		0xF000
Device and Revision ID		0xF200
Flash Controller		0xF400
PPS		0xFA00
Configuration	0xBFC0	0x0BF0

REGISTER 6-1: NVMCON: PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R-0	R-0	R-0	U-0	U-0	U-0
	WR	WREN(1)	WRERR(2)	LVDERR(2)	LVDSTAT(2)	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	NVMOP<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit
This bit is writable when WREN = 1 and the unlock sequence is followed.
1 = Initiate a Flash operation. Hardware clears this bit when the operation completes
0 = Flash operation complete or inactive

bit 14 **WREN:** Write Enable bit(1)
1 = Enable writes to WR bit and enables LVD circuit
0 = Disable writes to WR bit and disables LVD circuit
This is the only bit in this register reset by a device Reset.

bit 13 **WRERR:** Write Error bit(2)
This bit is read-only and is automatically set by hardware.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit (LVD circuit must be enabled)(2)
This bit is read-only and is automatically set by hardware.
1 = Low-voltage detected (possible data corruption, if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11 **LVDSTAT:** Low-Voltage Detect Status bit (LVD circuit must be enabled)(2)
This bit is read-only and is automatically set, and cleared, by hardware.
1 = Low-voltage event active
0 = Low-voltage event NOT active

bit 10-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation bits
These bits are writable when WREN = 0.
1111 =Reserved
•
•
•
0111 = Reserved
0110 =No operation
0101 =Program Flash (PFM) erase operation: erases PFM, if all pages are not write-protected
0100 =Page erase operation: erases page selected by NVMADDR, if it is not write-protected
0011 =Row program operation: programs row selected by NVMADDR, if it is not write-protected
0010 =No operation
0001 =Word program operation: programs word selected by NVMADDR, if it is not write-protected
0000 = No operation

Note 1: This bit is cleared by any reset (i.e., POR, BOR, WDT, $\overline{\text{MCLR}}$, SWR).

2: This bit is only cleared by setting NVMOP = 0000, and initiating a Flash WR operation or a POR. Any other kind of reset (i.e., BOR, WDT, $\overline{\text{MCLR}}$) does not clear this bit.

10.0 USB ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS60001126) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, full-speed device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 10-1.

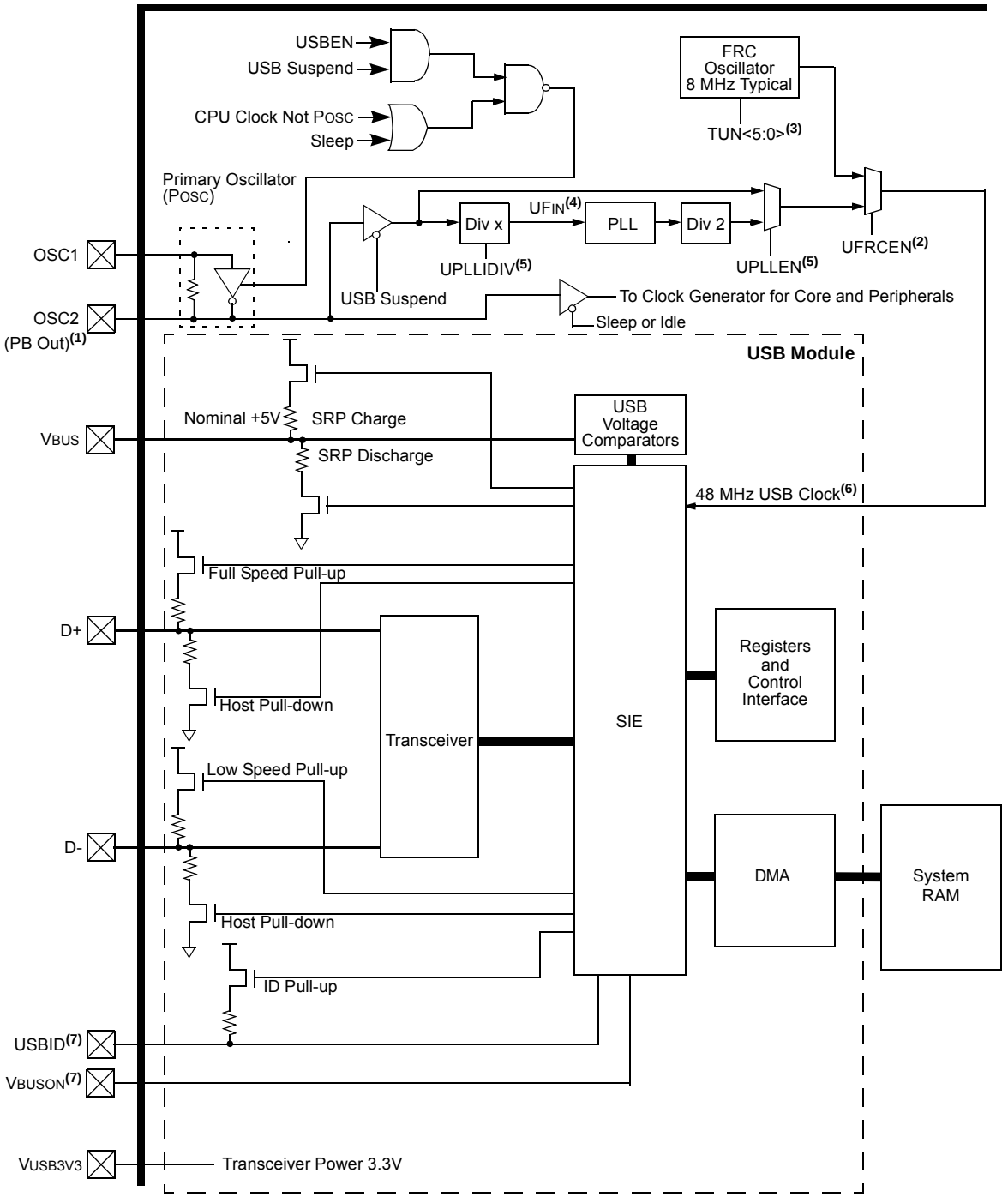
The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The PIC32 USB module includes the following features:

- USB Full-speed support for host and device
- Low-speed host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

Note: The implementation and use of the USB specifications, and other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

FIGURE 10-1: PIC32MX1XX/2XX/5XX USB INTERFACE DIAGRAM



Note 1: PB clock is only available on this pin for select EC modes.
2: This bit field is contained in the OSCCON register.
3: This bit field is contained in the OSCTRM register.
4: USB PLL UFIN requirements: 4 MHz.
5: This bit field is contained in the DEVCFG2 register.
6: A 48 MHz clock is required for proper USB operation.
7: Pins can be used as GPIO when the USB module is disabled or if the USB is enabled but DEVCFG3<31:30> = '0b00.

10.1 Control Registers

TABLE 10-1: USB REGISTER MAP

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5040	U1OTGIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
5050	U1OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
5060	U1OTGSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
5070	U1OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND(4)	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR	0000
5200	U1IR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF	0000
																		DETACHIF	0000
5210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000
																		DETACHIE	0000
5220	U1EIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	0000
																	EOFEF		0000
5230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE	0000
																	EOFEE		0000
5240	U1STAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0>				DIR	PPBI	—	—	0000
5250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE	SE0	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN	0000
													TOKBUSY					SOFEN	0000
5260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
5270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<15:9>							—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

REGISTER 10-2: U1OTGIE: USB OTG INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit
1 = ID interrupt enabled
0 = ID interrupt disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit
1 = 1 millisecond timer interrupt enabled
0 = 1 millisecond timer interrupt disabled

bit 5 **LSTATEIE:** Line State Interrupt Enable bit
1 = Line state interrupt enabled
0 = Line state interrupt disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit
1 = ACTIVITY interrupt enabled
0 = ACTIVITY interrupt disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit
1 = Session valid interrupt enabled
0 = Session valid interrupt disabled

bit 2 **SESENDIE:** B-Session End Interrupt Enable bit
1 = B-session end interrupt enabled
0 = B-session end interrupt disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-VBUS Valid Interrupt Enable bit
1 = A-VBUS valid interrupt enabled
0 = A-VBUS valid interrupt disabled

REGISTER 10-5: U1PWRC: USB POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	UACTPND	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
- 1 = USB bus activity has been detected; but an interrupt is pending, it has not been generated yet
- 0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit
- 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
- 0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit(1)
- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled

Note: When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit
- 1 = USB module is placed in Suspend mode (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit
- 1 = USB module is turned on
- 0 = USB module is disabled (Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

TABLE 11-1: INPUT PIN SELECTION (CONTINUED)

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT1	INT1R	INT1R<3:0>	0000 = RPD1 0001 = RPG9 0010 = RPB14 0011 = RPD0 0100 = RPD8 0101 = RPB6 0110 = RPD5 0111 = RPB2 1000 = RPF3(4) 1001 = RPF13(3) 1010 = Reserved 1011 = RPF2(1) 1100 = RPC2(3) 1101 = RPE8(3) 1110 = Reserved 1111 = Reserved
T3CK	T3CKR	T3CKR<3:0>	
IC1	IC1R	IC1R<3:0>	
$\overline{\text{U3CTS}}$	U3CTSR	U3CTSR<3:0>	
U4RX	U4RXR	U4RXR<3:0>	
U5RX	U5RXR	U5RXR<3:0>	
$\overline{\text{SS2}}$	SS2R	SS2R<3:0>	
OCFA	OCFAR	OCFAR<3:0>	

Note 1: This selection is not available on 64-pin USB devices.

2: This selection is only available on 100-pin General Purpose devices.

3: This selection is not available on 64-pin devices.

4: This selection is not available when USBID functionality is used on USB devices.

5: This selection is not available on devices without a CAN module.

6: This selection is not available on USB devices.

7: This selection is not available when VBUSON functionality is used on USB devices.

TABLE 11-2: OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD2	RPD2R	RPD2R<3:0>	0000 = No Connect 0001 = U3TX 0010 = U4RTS 0011 = Reserved 0100 = Reserved 0101 = Reserved 0110 = SDO2 0111 = Reserved 1000 = Reserved 1001 = Reserved 1010 = Reserved 1011 = OC3 1100 = C1TX(5) 1101 = C2OUT 1110 = SDO3 1111 = SDO4(3)
RPG8	RPG8R	RPG8R<3:0>	
RPF4	RPF4R	RPF4R<3:0>	
RPD10	RPD10R	RPD10R<3:0>	
RPF1	RPF1R	RPF1R<3:0>	
RPB9	RPB9R	RPB9R<3:0>	
RPB10	RPB10R	RPB10R<3:0>	
RPC14	RPC14R	RPC14R<3:0>	
RPB5(7)	RPB5R	RPB5R<3:0>	
RPC1(3)	RPC1R	RPC1R<3:0>	
RPD14(3)	RPD14R	RPD14R<3:0>	
RPG1(3)	RPG1R	RPG1R<3:0>	
RPA14(3)	RPA14R	RPA14R<3:0>	
RPD3	RPD3R	RPD3R<3:0>	0000 = No Connect 0001 = U2TX 0010 = Reserved 0011 = U1TX 0100 = U5RTS(3) 0101 = Reserved 0110 = SDO2 0111 = Reserved 1000 = SDO1 1001 = Reserved 1010 = Reserved 1011 = OC4 1100 = Reserved 1101 = C3OUT 1110 = SDO3 1111 = SDO4(3)
RPG7	RPG7R	RPG7R<3:0>	
RPF5	RPF5R	RPF5R<3:0>	
RPD11	RPD11R	RPD11R<3:0>	
RPF0	RPF0R	RPF0R<3:0>	
RPB1	RPB1R	RPB1R<3:0>	
RPE5	RPE5R	RPE5R<3:0>	
RPC13	RPC13R	RPC13R<3:0>	
RPB3	RPB3R	RPB3R<3:0>	
RPF3(4)	RPF3R	RPF3R<3:0>	
RPC4(3)	RPC4R	RPC4R<3:0>	
RPD15(3)	RPD15R	RPD15R<3:0>	
RPG0(3)	RPG0R	RPG0R<3:0>	
RPA15(3)	RPA15R	RPA15R<3:0>	

Note 1: This selection is not available on 64-pin USB devices.

2: This selection is only available on 100-pin General Purpose devices.

3: This selection is not available on 64-pin devices.

4: This selection is not available when USBID functionality is used on USB devices.

5: This selection is not available on devices without a CAN module.

6: This selection is not available on USB devices.

7: This selection is not available when VBUSON functionality is used on USB devices.

TABLE 11-7: PORTD REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSELD15	ANSELD14	ANSELD13	ANSELD12	—	—	—	—	ANSELD7	ANSELD6	—	—	ANSELD3	ANSELD2	ANSELD1	—	F0CE
6310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
5320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
6330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
6340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
6350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	CNPUD8	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
6360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	CNPDD8	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
6370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIED15	CNIED14	CNIED13	CNIED12	CNIED11	CNIED10	CNIED9	CNIED8	CNIED7	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	0000
6390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNS TATD15	CN STATD14	CN STATD13	CN STATD12	CN STATD11	CN STATD10	CN STATD9	CN STATD8	CN STATD7	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

NOTES:

REGISTER 20-10: PMRDIN: PARALLEL PORT READ INPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RDATAIN<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RDATAIN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RDATAIN<15:0>:** Port Read Input Data bits

Note:	This register is only used when the DUALBUF bit (PMCON<17>) is set to '1' and exclusively for reads. If the DUALBUF bit is '0', the PMDIN register (Register 20-5) is used for reads instead of PMRDIN.

REGISTER 23-17: C1FIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXNEMPTYIE
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	TXNFULLIF(1)	TXHALFIF	TXEMPTYIF(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R-0	R-0	R-0
	—	—	—	—	RXOVFLIF	RXFULLIF(1)	RXHALFIF(1)	RXNEMPTYIF(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit
1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is not full
0 = FIFO is full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

Note 1: This bit is read-only and reflects the status of the FIFO.

28.3 On-Chip Voltage Regulator

All PIC32MX1XX/2XX/5XX 64/100-pin devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX1XX/2XX/5XX 64/100-pin family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 28-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 31.1 "DC Characteristics"**.

Note:	It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.

28.3.1 HIGH VOLTAGE DETECT (HVD)

The HVD module monitors the core voltage at the VCAP pin. If a voltage above the required level is detected on VCAP, the I/O pins are disabled and the device is held in Reset as long as the HVD condition persists. See parameter HV10 (VHVD) in Table 31-11 in **Section 31.1 "DC Characteristics"** for more information.

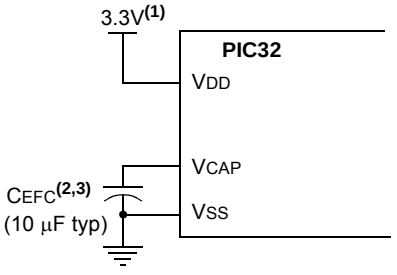
28.3.2 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

28.3.3 ON-CHIP REGULATOR AND BOR

PIC32MX1XX/2XX/5XX 64/100-pin devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 31.1 "DC Characteristics"**.

FIGURE 28-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



Note 1: These are typical operating voltages. Refer to **Section 31.1 "DC Characteristics"** for the full operating ranges of VDD.
2: It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.
3: The typical voltage on the VCAP pin is 1.8V.

28.4 Programming and Diagnostics

PIC32MX1XX/2XX/5XX 64/100-pin devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules that provide a range of functions to the application developer.

FIGURE 28-2: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS

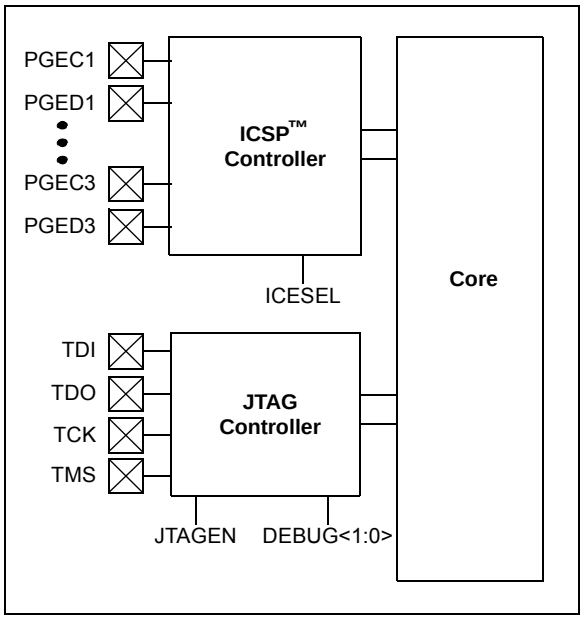


TABLE 31-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage (Note 2)**	2.3	—	3.6	V	—
DC12	VDR	**RAM Data Retention Voltage (Note 1)**	1.75	—	—	V	—
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	1.75	—	2.1	V	—
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.00005	—	0.115	V/μs	—

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for BOR values.

FIGURE 31-20: PARALLEL SLAVE PORT TIMING