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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx530f128lt-50i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 4: PIN NAMES FOR 100-PIN GENERAL PURPOSE DEVICES (CONTINUED)

10	0-PIN TQFP (TOP VIEW)		
	PIC32MX130F128L PIC32MX150F256L PIC32MX170F512L		
			100
Din #	Full Bin Name	Din #	Full Bin Name
FIII #		FIII #	
/1	RPD11/PMA14/RD11	86	VDD
/./		07	
72	RPD0/RD0	87	AN44/C3INA/RPF0/PMD11/RF0
73	RPD0/RD0 SOSCI/RPC13/RC13	87 88	AN44/C3INA/RPF0/PMD11/RF0 AN45/RPF1/PMD10/RF1
72 73 74	RPD0/RD0 SOSCI/RPC13/RC13 SOSCO/RPC14/T1CK/RC14	87 88 89	AN44/C3INA/RPF0/PMD11/RF0 AN45/RPF1/PMD10/RF1 RPG1/PMD9/RG1
72 73 74 75	RPD0/RD0 SOSCI/RPC13/RC13 SOSCO/RPC14/T1CK/RC14 Vss	87 88 89 90	AN44/C3INA/RPF0/PMD11/RF0 AN45/RPF1/PMD10/RF1 RPG1/PMD9/RG1 RPG0/PMD8/RG0
72 73 74 75 76 77	RPD0/RD0 SOSCI/RPC13/RC13 SOSCO/RPC14/T1CK/RC14 Vss AN24/RPD1/RD1 AN25/RPD2/RD2	87 88 89 90 91	AN44/C3INA/RPF0/PMD11/RF0 AN45/RPF1/PMD10/RF1 RPG1/PMD9/RG1 RPG0/PMD8/RG0 RA6 CTED8/DA7
72 73 74 75 76 77 78	RPD0/RD0 SOSCI/RPC13/RC13 SOSCO/RPC14/T1CK/RC14 Vss AN24/RPD1/RD1 AN25/RPD2/RD2 AN26/C3IND/RPD3/RD3	87 88 89 90 91 92 93	AN44/C3INA/RPF0/PMD11/RF0 AN45/RPF1/PMD10/RF1 RPG1/PMD9/RG1 RPG0/PMD8/RG0 RA6 CTED8/RA7 AN46/PMD0/PE0
72 73 74 75 76 77 78 79	RPD0/RD0 SOSCI/RPC13/RC13 SOSCO/RPC14/T1CK/RC14 Vss AN24/RPD1/RD1 AN25/RPD2/RD2 AN26/C3IND/RPD3/RD3 AN40/RPD12/RD12	87 88 89 90 91 92 93 94	AN44/C3INA/RPF0/PMD11/RF0 AN45/RPF1/PMD10/RF1 RPG1/PMD9/RG1 RPG0/PMD8/RG0 RA6 CTED8/RA7 AN46/PMD0/RE0 AN47/PMD1/RE1
72 73 74 75 76 77 78 79 80	RPD0/RD0 SOSCI/RPC13/RC13 SOSCO/RPC14/T1CK/RC14 Vss AN24/RPD1/RD1 AN25/RPD2/RD2 AN26/C3IND/RPD3/RD3 AN40/RPD12/PMD12/RD12 AN41/PMD13/RD13	87 88 89 90 91 92 93 94 95	AN44/C3INA/RPF0/PMD11/RF0 AN45/RPF1/PMD10/RF1 RPG1/PMD9/RG1 RPG0/PMD8/RG0 RA6 CTED8/RA7 AN46/PMD0/RE0 AN47/PMD1/RE1 RG14
72 73 74 75 76 77 78 79 80 81	RPD0/RD0 SOSCI/RPC13/RC13 SOSCO/RPC14/T1CK/RC14 Vss AN24/RPD1/RD1 AN25/RPD2/RD2 AN26/C3IND/RPD3/RD3 AN40/RPD12/PMD12/RD12 AN41/PMD13/RD13 RPD4/PMWR/RD4	87 88 89 90 91 92 93 94 95 96	AN44/C3INA/RPF0/PMD11/RF0 AN45/RPF1/PMD10/RF1 RPG1/PMD9/RG1 RPG0/PMD8/RG0 RA6 CTED8/RA7 AN46/PMD0/RE0 AN47/PMD1/RE1 RG14 RG12
72 73 74 75 76 77 78 79 80 81 82	RPD0/RD0 SOSCI/RPC13/RC13 SOSCO/RPC14/T1CK/RC14 Vss AN24/RPD1/RD1 AN25/RPD2/RD2 AN26/C3IND/RPD3/RD3 AN40/RPD12/PMD12/RD12 AN41/PMD13/RD13 RPD4/PMWR/RD4 RPD5/PMRD/RD5	87 88 89 90 91 92 93 94 95 96 97	AN44/C3INA/RPF0/PMD11/RF0 AN45/RPF1/PMD10/RF1 RPG1/PMD9/RG1 RPG0/PMD8/RG0 RA6 CTED8/RA7 AN46/PMD0/RE0 AN47/PMD1/RE1 RG14 RG12 RG13
73 74 75 76 77 78 79 80 81 82 83	RPD0/RD0 SOSCI/RPC13/RC13 SOSCO/RPC14/T1CK/RC14 Vss AN24/RPD1/RD1 AN25/RPD2/RD2 AN26/C3IND/RPD3/RD3 AN40/RPD12/PMD12/RD12 AN41/PMD13/RD13 RPD4/PMWR/RD4 RPD5/PMRD/RD5 AN42/C3INC/PMD14/RD6	87 88 89 90 91 92 93 94 95 96 97 98	AN44/C3INA/RPF0/PMD11/RF0 AN45/RPF1/PMD10/RF1 RPG1/PMD9/RG1 RPG0/PMD8/RG0 RA6 CTED8/RA7 AN46/PMD0/RE0 AN47/PMD1/RE1 RG14 RG12 RG13 AN20/PMD2/RE2
72 73 74 75 76 77 78 79 80 81 82 83 84	RPD0/RD0 SOSCI/RPC13/RC13 SOSCO/RPC14/T1CK/RC14 Vss AN24/RPD1/RD1 AN25/RPD2/RD2 AN26/C3IND/RPD3/RD3 AN40/RPD12/PMD12/RD12 AN41/PMD13/RD13 RPD4/PMWR/RD4 RPD5/PMRD/RD5 AN42/C3INC/PMD14/RD6 AN43/C3INB/PMD15/RD7	87 88 89 90 91 92 93 94 95 96 97 98 99	AN44/C3INA/RPF0/PMD11/RF0 AN45/RPF1/PMD10/RF1 RPG1/PMD9/RG1 RPG0/PMD8/RG0 RA6 CTED8/RA7 AN46/PMD0/RE0 AN47/PMD1/RE1 RG14 RG12 RG13 AN20/PMD2/RE2 RPE3/CTPLS/PMD3/RE3

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See Section 11.0 "I/O Ports" for more information.

3: Shaded pins are 5V tolerant.

Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note:	To acc	ess the docume	ents listed	below,
	browse	e to the docume	ntation se	ction of
	the	Microchip	web	site
	(www.r	nicrochip.com).		

- Section 1. "Introduction" (DS60001127)
- Section 2. "CPU" (DS60001113)
- Section 3. "Memory Organization" (DS60001115)
- Section 5. "Flash Program Memory" (DS60001121)
- Section 6. "Oscillator Configuration" (DS60001112)
- Section 7. "Resets" (DS60001118)
- Section 8. "Interrupt Controller" (DS60001108)
- Section 9. "Watchdog Timer and Power-up Timer" (DS60001114)
- Section 10. "Power-Saving Features" (DS60001130)
- Section 12. "I/O Ports" (DS60001120)
- Section 13. "Parallel Master Port (PMP)" (DS60001128)
- Section 14. "Timers" (DS60001105)
- Section 15. "Input Capture" (DS60001122)
- Section 16. "Output Compare" (DS60001111)
- Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104)
- Section 19. "Comparator" (DS60001110)
- Section 20. "Comparator Voltage Reference (CVREF)" (DS60001109)
- Section 21. "Universal Asynchronous Receiver Transmitter (UART)" (DS60001107)
- Section 23. "Serial Peripheral Interface (SPI)" (DS60001106)
- Section 24. "Inter-Integrated Circuit (I²C)" (DS60001116)
- · Section 27. "USB On-The-Go (OTG)" (DS60001126)
- Section 29. "Real-Time Clock and Calendar (RTCC)" (DS60001125)
- Section 31. "Direct Memory Access (DMA) Controller" (DS60001117)
- Section 32. "Configuration" (DS60001124)
- Section 33. "Programming and Diagnostics" (DS60001129)
- Section 34. "Controller Area Network (CAN)" (DS60001123)
- Section 37. "Charge Time Measurement Unit (CTMU)" (DS60001167)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS9	IFS8
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	IFS7	IFS6	IFS5	IFS4	IFS3	IFS2	IFS1	IFS0

REGISTER 5-4: IFSx: INTERRUPT FLAG STATUS REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 IFS31-IFS0: Interrupt Flag Status bits

- 1 = Interrupt request has occurred
- 0 = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 5-1 for the exact bit definitions.

REGISTER 5-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	IEC7	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 IEC31-IEC0: Interrupt Enable bits

- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 5-1 for the exact bit definitions.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
00.40	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	_	_			TUN<	5:0> ⁽¹⁾		

Legend:	y = Value set from Configuration bits on POR				
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-6 Unimplemented: Read as '0'

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized, nor tested.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 3-0 ROSEL<3:0>: Reference Clock Source Select bits⁽¹⁾

- 1111 = Reserved; do not use
- 1001 = Reserved; do not use 1000 = REFCLKI 0111 = System PLL output 0110 = USB PLL output 0101 = Sosc 0100 = LPRC 0011 = FRC 0010 = POSC 0001 = PBCLK 0000 = SYSCLK
- **Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.
 - 2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
 - 3: While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
31:24	—	—	BYTO<1:0>		WBO ⁽¹⁾	—	—	BITO
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	—	—	—		PLEN<4:0>			
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP ⁽¹⁾	CRCTYP	—	— — CRCCH<2:0>			

REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER

Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

- bit 29-28 BYTO<1:0>: CRC Byte Order Selection bits
 - 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
 - 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
 - 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
 - 00 = No swapping (i.e., source byte order)
- bit 27 **WBO:** CRC Write Byte Order Selection bit⁽¹⁾
 - 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
 - 0 = Source data is written to the destination unaltered
- bit 26-25 Unimplemented: Read as '0'
- bit 24 BITO: CRC Bit Order Selection bit⁽¹

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

<u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode):

- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 Unimplemented: Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits⁽¹⁾

<u>When CRCTYP (DCRCCON<15>) = 1</u> (CRC module is in IP Header mode): These bits are unused.

<u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode): Denotes the length of the polynomial -1.

- bit 7 CRCEN: CRC Enable bit
 - 1 = CRC module is enabled and channel transfers are routed through the CRC module
 - 0 = CRC module is disabled and channel transfers proceed normally
- Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	_	_	—		_	_
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	_	—	—	—	_	—	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-24	Unimplemented: Read as '0'
bit 23	CHSDIE: Channel Source Done Interrupt Enable bit
	1 = Interrupt is enabled0 = Interrupt is disabled
bit 22	CHSHIE: Channel Source Half Empty Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 21	CHDDIE: Channel Destination Done Interrupt Enable bit
	1 = Interrupt is enabled 0 = Interrupt is disabled
bit 20	CHDHIE: Channel Destination Half Full Interrupt Enable bit
	1 = Interrupt is enabled0 = Interrupt is disabled
bit 19	CHBCIE: Channel Block Transfer Complete Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 18	CHCCIE: Channel Cell Transfer Complete Interrupt Enable bit
	1 = Interrupt is enabled 0 = Interrupt is disabled
bit 17	CHTAIE: Channel Transfer Abort Interrupt Enable bit
	1 = Interrupt is enabled0 = Interrupt is disabled
bit 16	CHERIE: Channel Address Error Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 15-8	Unimplemented: Read as '0'
DIT /	CHSDIF: Channel Source Done Interrupt Flag bit
	0 = No interrupt is pending
bit 6	CHSHIF: Channel Source Half Empty Interrupt Flag bit
	1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)0 = No interrupt is pending
bit 5	CHDDIF: Channel Destination Done Interrupt Flag bit
	1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)0 = No interrupt is pending
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TABLE 10-1: USB REGISTER MAP (CONTINUED)

ess		6		Bits															
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
5300		31:16	_	_	—	—	—	—	_	-	-	-	—	—	—		—	_	0000
5550	UTEI 9	15:0	_	_	_	_	_	_	—	_	_	_	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5340		31:16	_	_	—	—	—	—	_	_		_	_		_	_	_		0000
5570	UTEI TU	15:0	_	_	_	_	_	_	_	-	_	_	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53R0		31:16			_	_	_	_	_				_	—	_			—	0000
5560	UIEFII	15:0			_	_	_	_	_				_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5300		31:16			_	_	_	_	_				_	—	_			—	0000
5500	UTLP 12	15:0			_	_	_	_	_				_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5300		31:16			_	_	_	_	_				_	—	_			—	0000
3300	UILF 15	15:0			_	_	_	_	_				_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5050		31:16	_	_	_	_	_	_		_	_	_	_	—	_	_	_	—	0000
53E0	UTEP14	15:0	_	_					_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5250		31:16	_	_	_		_	_	_	_	_	_	_	_	—	—	_	—	0000
5350	UIEPIS	15:0	_	_					_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER (CONTINUED)

- bit 1 CRC5EF: CRC5 Host Error Flag bit⁽⁴⁾
 - 1 = Token packet rejected due to CRC5 error
 - 0 = Token packet accepted
 - EOFEF: EOF Error Flag bit^(3,5)
 - 1 = EOF error condition detected
 - 0 = No EOF error condition
- bit 0 PIDEF: PID Check Failure Flag bit
 - 1 = PID check failed
 - 0 = PID check passed
- **Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.
 - **2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.
 - **3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.
 - 4: Device mode.
 - 5: Host mode.

REGISTER 10-10: U1STAT: USB STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—		—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—		—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—		—	—	—	—	—
7.0	R-x	R-x	R-x R-x		R-x	R-x	U-0	U-0
7:0		ENDP.	T<3:0>		DIR	PPBI	_	_

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits (Represents the number of the BDT, updated by the last USB transfer.)
 - 1111 = Endpoint 15 1110 = Endpoint 14 . . 0001 = Endpoint 1 0000 = Endpoint 0
- bit 3 **DIR:** Last BD Direction Indicator bit
 - 1 = Last transaction was a transmit transfer (TX)
 - 0 = Last transaction was a receive transfer (RX)
- bit 2 **PPBI:** Ping-Pong BD Pointer Indicator bit
 - 1 = The last transaction was to the ODD BD bank
 - 0 = The last transaction was to the EVEN BD bank
- bit 1-0 Unimplemented: Read as '0'

Note: The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. U1STAT value is only valid when the TRNIF bit (U1IR<3>) is active. Clearing the TRNIF bit advances the FIFO. Data in register is invalid when the TRNIF bit = 0.

TABLE 11-14: PORTF REGISTER MAP FOR PIC32MX230F128H, PIC32MX530F128H, PIC32MX250F256H, PIC32MX550F256H, PIC32MX270F512H, AND PIC32MX570F512H DEVICES ONLY

ess		6								Bi	its								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6510	TRISF	31:16	_		—	—	—	—		_	_	—	—	—	—	_	—	—	0000
		15:0	_	_	—	—	_	—	—	_	_		TRISF5	TRISF4	TRISF3	_	TRISF1	TRISF0	003B
6520	PORTF	31:16	—	—	—	_	—	—	—	—	—	—	—	—	—	—	—		0000
		15:0	—	—	—	—	—	—	—	_		—	RF5	RF4	RF3	—	RF1	RF0	XXXX
6530	LATE	31:16	—	—	—	—	—	—	_	—	_		_	_	—	—	_		0000
	2	15:0	—	_	—	—	-	—	—	-	—	—	LATF5	LATF4	LATF3	-	LATF1	LATF0	xxxx
6540	ODCE	31:16	—	_	_	—	_	_		_	_				—	_		—	0000
0010	0001	15:0	—	—	—	—	—	—	—	_	_	—	ODCF5	ODCF4	ODCF3	—	ODCF1	ODCF0	0000
6550	CNPLIE	31:16	—	_	—	—		—	—	_	_	—	—	—	—	_	—	—	0000
0000		15:0	—		—	—	_	—		_	_		CNPUF5	CNPUF4	CNPUF3		CNPUF1	CNPUF0	0000
6560		31:16	—	—	—	—	—	—	_	—	—		_	_	—	—	_	-	0000
0000		15:0	_	_	—	—	-	—	—	-	_	—	CNPDF5	CNPDF4	CNPDF3	_	CNPDF1	CNPDF0	0000
6570		31:16	—	-	—	—	_	—	—	_	_	_	_	_	—	-	—	-	0000
0370	CINCOIN	15:0	ON	-	SIDL	—	_	—	—	_	_	_	_	_	—	-	—	-	0000
6580		31:16	_		_	—		_	_			_	_	_	_		_	—	0000
0500	CINEINF	15:0		—	—	—	—	_	—	—	—	_	CNIEF5	CNIEF4	CNIEF3	—	CNIEF1	CNIEF0	0000
		31:16	—	_		_	—	_	—	—	—	_	—	—	—	—	—	—	0000
6590	CNSTATF	15:0	_	_	—	—	_	_	_	_	_	—	CN STATF5	CN STATF4	CN STATF3	_	CN STATF1	CN STATF0	0000

Legend: x = Unknown value on Reset; -- = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

14.0 WATCHDOG TIMER (WDT)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 9. "Watchdog, Deadman, and Power-up Timers" (DS60001114) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The Watchdog Timer (WDT), when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- · Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle



FIGURE 14-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM

NOTES:

REGISTER 15-1: ICXCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)('x' = 1 THROUGH 5)

- bit 2-0 ICM<2:0>: Input Capture Mode Select bits
 - 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
 - 110 = Simple Capture Event mode every edge, specified edge first and every edge thereafter
 - 101 = Prescaled Capture Event mode every sixteenth rising edge
 - 100 = Prescaled Capture Event mode every fourth rising edge
 - 011 = Simple Capture Event mode every rising edge
 - 010 = Simple Capture Event mode every falling edge
 - 001 = Edge Detect mode every edge (rising and falling)
 - 000 = Input Capture module is disabled
- **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 4 DISSDI: Disable SDI bit
 - 1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
 - 0 = SDI pin is controlled by the SPI module
- bit 3-2 STXISEL<1:0>: SPI Transmit Buffer Empty Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
 - 10 = Interrupt is generated when the buffer is empty by one-half or more
 - 01 = Interrupt is generated when the buffer is completely empty
 - 00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete
- bit 1-0 SRXISEL<1:0>: SPI Receive Buffer Full Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is full
 - 10 = Interrupt is generated when the buffer is full by one-half or more
 - 01 = Interrupt is generated when the buffer is not empty
 - 00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)
- **Note 1:** When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - **2:** This bit can only be written when the ON bit = 0.
 - **3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
 - 4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

19.2 Timing Diagrams

Figure 19-2 and Figure 19-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 19-2: UART RECEPTION



FIGURE 19-3: TRANSMISSION (8-BIT OR 9-BIT DATA)



20.0 PARALLEL MASTER PORT (PMP)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 13. "Parallel Master Port (PMP)" (DS60001128) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The PMP is a parallel 8-bit or 16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable. The following are the key features of the PMP module:

- 8-bit,16-bit interface
- · Up to 16 programmable address lines
- · Up to two Chip Select lines
- Programmable strobe options:
 - Individual read and write strobes, or
 - Read/write strobe with enable strobe
- Selectable polarity
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support:
 - Legacy addressable
 - Address support
- · Read and Write 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Freeze option for in-circuit debugging

Note: On 64-pin devices, data pins PMD<15:8> are not available in 16-bit Master modes.



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REGISTER	23-10: C1FLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)
bit 20-16	FSEL2<4:0>: FIFO Selection bits
	11111 = Reserved
	•
	10000 = Reserved
	01111 = Message matching filter is stored in FIFO buffer 15
	•
	•
hit 15	ELTEN4: Filter 4 Enchle bit
DIC 15	FLIENT: Filler I Effable bit
	0 = Filter is disabled
bit 14-13	MSEL1<1:0>: Filter 1 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
bit 12 8	ESEL 1 - Acceptance Mask 0 selected
DIL 12-0	11111 = Reserved
	•
	•
	10000 = Reserved
	01111 = Message matching filter is stored in FIFO buffer 15
	•
	•
	00000 = Message matching filter is stored in FIFO buffer 0
bit 7	FLTEN0: Filter 0 Enable bit
	1 = Filter is enabled
bit 6-5	MSEL 0-1:0>: Filter 0 Mack Select hits
bit 0-0	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 4-0	FSEL0<4:0>: FIFO Selection bits
	11111 = Reserved
	•
	•
	01111 = Message matching filter is stored in FIFO buffer 15
	•
	00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

27.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to enabled or disabled peripherals:

- Control register lock sequence
- · Configuration bit select lock

27.4.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes.

To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 6.** "**Oscillator**" (DS60001112) in the "*PIC32 Family Reference Manual*" for details.

27.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If PMDLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.