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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	MIPS32 ® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx550f256h-50i-mr

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 1-1:	PINOUT I/O DESCRIPTIONS ((CONTINUED)	

	Pin N	umber						
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	Pin Type	Buffer Type	Description			
RTCC	42	68	0	—	Real-Time Clock Alarm Output			
CVREFOUT	23	34	0	Analog	Comparator Voltage Reference (Output)			
C1INA	11	20	Ι	Analog				
C1INB	12	21	Ι	Analog	Comportor 1 Innuto			
C1INC	5	11	I	Analog				
C1IND	4	10	I	Analog				
C2INA	13	22	I	Analog				
C2INB	14	23	I	Analog	Comportor 2 Innuito			
C2INC	8	14	I	Analog				
C2IND	6	12	I	Analog	1			
C3INA	58	87	I	Analog				
C3INB	55	84	I	Analog	Comportor 2 Innuito			
C3INC	54	83	I	Analog				
C3IND	51	78	I	Analog				
C10UT	PPS	PPS	0	_	Comparator 1 Output			
C2OUT	PPS	PPS	0	_	Comparator 2 Output			
C3OUT	PPS	PPS	0	_	Comparator 3 Output			
PMALL	30	44	0	TTL/ST	Parallel Master Port Address Latch Enable Low Byte			
PMALH	29	43	0	TTL/ST	Parallel Master Port Address Latch Enable High Byte			
PMA0	30	44	0	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)			
PMA1	29	43	0	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)			
Legend:	CMOS = CN	IOS compati	ible inpu	ut or output	Analog = Analog input I = Input O = Output			

Legend: CMOS = CMOS compatible input or output Analog = Analog input I = Input ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

3.2 Architecture Overview

The MIPS32[®] M4K[®] processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e[®] Support
- · Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32[®] M4K[®] processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation.

The execution unit includes:

- · 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- · Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32[®] M4K[®] processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1:MIPS32[®] M4K[®] PROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/
DIVIDE UNIT LATENCIES AND REPEAT RATES

Op code	Operand Size (mul rt) (div rs)	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU,	16 bits	1	1
MSUB/MSUBU	32 bits	2	2
MUL	16 bits	2	1
	32 bits	3	2
DIV/DIVU	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

5.1 Interrupts Control Registers

TABLE 5-2: INTERRUPT REGISTER MAP

ess											Bits								
Virtual Addr (BF88_#)	Register Name ⁽³⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1000		31:16	_	—	—	_	—	—	_	—	—	_	—	—	—	_	—	_	0000
1000		15:0	—	—	—	MVEC	—		TPC<2:0>		—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT ⁽⁴⁾	31:16	_	_	—	_		—	—	—	—	—	—	—	—	_	—	—	0000
		15:0	—	—	—	—	—	S	SRIPL<2:0	>	—	—			VEC<	5:0>			0000
1020	IPTMR	31:16 15:0	IPTMR<31:0>						0000										
4000	1500	31:16	FCEIF	RTCCIF	FSCMIF	AD1IF	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
1030	IF50	15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INTOIF	CS1IF	CS0IF	CTIF	0000
1040	IEQ1	31:16	U3RXIF	U3EIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	SPI2RXIF	SPI2EIF	PMPEIF	PMPIF	CNGIF	CNFIF	CNEIF	0000
1040	IFST	15:0	CNDIF	CNCIF	CNBIF	CNAIF	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1TXIF	SPI1RXIF	SPI1EIF	USBIF ⁽²⁾	CMP2IF	CMP1IF	0000
1050 JES2 31		31:16	—	—	—		—	_	_	—	-	—	-	_	SPI4TXIF ⁽¹⁾	SPI4RXIF ⁽¹⁾	SPI4EIF ⁽¹⁾	SPI3TXIF	0000
1000	11 02	15:0	SPI3RXIF	SPI3EIF	CANIF	CMP3IF	DMA3IF	DMA2IF	DMA1IF	DMA0IF	CTMUIF	U5TXIF ⁽¹⁾	U5RXIF ⁽¹⁾	U5EIF ⁽¹⁾	U4TXIF	U4RXIF	U4EIF	U3TXIF	0000
1060	IEC0	31:16	FCEIE	RTCCIE	FSCMIE	AD1IE	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
	.200	15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INTOIE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	U3RXIE	U3EIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2TXIE	SPI2RXIE	SPI2EIE	PMPEIE	PMPIE	CNGIE	CNFIE	CNEIE	0000
		15:0	CNDIE	CNCIE	CNBIE	CNAIE	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1TXIE	SPI1RXIE	SPI1EIE	USBIE ⁽²⁾	CMP2IE	CMP1IE	0000
1080	IEC2	31:16	—		—		—	—	—	—	—	— (1)	—	—	—		—	—	0000
		15:0		_	_	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE	CTMUIE	U5TXIE(')	U5RXIE()	U5EIE()	U4TXIE	U4RXIE	U4EIE	U3TXIE	0000
1090	IPC0	31:16	_		_	IN	10IP<2:0>		INTOIS	5<1:0>		_			CS1IP<2:0>	>	CS1IS	5<1:0>	0000
		15:0	_				SUIP<2:0>		CSUIS	5<1:0>		_	_	-	CTIP<2:0>		CTIS	<1:0>	0000
10A0	IPC1	15:0	_		_	IN	11IP<2:0>			5<1:0>	_	_	_		UCTIP<2:02	>		<1:0>	0000
		15.0					TOID -0.05			2-1-0-					00000-000		00016	<1.0~	0000
10B0	IPC2	31.10		<u> </u>		IN	INT2IP<2:0> INT2IS<1:0> — —			_			2		5<1.U>	0000			
		15:0	_		_	ICZIP<2:0> ICZIS<1:0> IZIP<2:0> IZIS<				<1:0>	0000								
10C0	IPC3	15.0				INT SIF <2.02 INT SIS <1:02				UC313	<1.0>	0000							
		31.16					T4IP<2:0>			S<1.02					OC4IP<2:02	>	00/19	S<1:0>	0000
10D0	IPC4	15.0	_			10	4IP<2:0>		IC4IS	<1:0>	_	_	_		T4IP<2:0>		T4IS	<1:0>	0000
L		10.0					-2.0		10-10								1410	1.04	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This bit is only available on 100-pin devices.

2: This bit is only implemented on devices with a USB module.

3: With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

4: This register does not have associated CLR, SET, and INV registers.

5: This bit is only implemented on devices with a CAN module.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31.24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	—	—	—		IP3<2:0>	IS3<	:1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<	:1:0>
15.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	—	—	—		IP1<2:0>		IS1<	:1:0>
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	_	_	_		IP0<2:0>		IS0<	:1:0>

REGISTER 5-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 Unimplemented: Read as '0'

000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits

- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0
- bit 23-21 Unimplemented: Read as '0'

bit 20-18 IP2<2:0>: Interrupt Priority bits

```
111 = Interrupt priority is 7
```

```
•
•
• • • •
```

- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1 000 = Interrupt is disabled
- bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits
 - 11 = Interrupt subpriority is 3
 - 10 = Interrupt subpriority is 2
 - 01 = Interrupt subpriority is 1
 - 00 = Interrupt subpriority is 0
- bit 15-13 Unimplemented: Read as '0'
- bit 12-10 IP1<2:0>: Interrupt Priority bits

111 = Interrupt priority is 7

- 010 = Interrupt priority is 2 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

Note: This register represents a generic definition of the IPCx register. Refer to Table 5-1 for the exact bit definitions.

7.0 RESETS

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7.** "**Resets**" (DS60001118) in the "*PIC32 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com/PIC32). The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- MCLR: Master Clear Reset pin
- · SWR: Software Reset
- WDTR: Watchdog Timer Reset
- · BOR: Brown-out Reset
- CMR: Configuration Mismatch Reset
- HVDR: High Voltage Detect Reset

A simplified block diagram of the Reset module is illustrated in Figure 7-1.



FIGURE 7-1: SYSTEM RESET BLOCK DIAGRAM

9.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 31. "Direct Memory Access (DMA) Controller" (DS60001117) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32 Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32 (such as Peripheral Bus (PBUS) devices: SPI, UART, PMP, etc.) or memory itself.

The following are some of the key features of the DMA controller module:

- Four identical channels, each featuring:
 - Auto-increment source and destination address registers
 - Source and destination pointers
 - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
 - Transfer granularity, down to byte level
 - Bytes need not be word-aligned at source and destination

- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
 - Manual (software) or automatic (interrupt) DMA requests
 - One-Shot or Auto-Repeat Block Transfer modes
 - Channel-to-channel chaining
- · Flexible DMA requests:
 - A DMA request can be selected from any of the peripheral interrupt sources
 - Each channel can select any (appropriate) observable interrupt as its DMA request source
 - A DMA transfer abort can be selected from any of the peripheral interrupt sources
 - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
 - DMA channel block transfer complete
 - Source empty or half empty
 - Destination full or half full
 - DMA transfer aborted due to an external event
 - Invalid DMA address generated
- DMA debug support features:
 - Most recent address accessed by a DMA channel
 - Most recent DMA channel to transfer data
- · CRC Generation module:
 - CRC module can be assigned to any of the available channels
 - CRC module is highly configurable



FIGURE 9-1: DMA BLOCK DIAGRAM

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	—	—	—	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	—	—	—	—	—	—	—	—		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	CHSSIZ<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0				CHSSIZ	<7:0>					

REGISTER 9-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSSIZ<15:0>: Channel Source Size bits

1111111111111111 = 65,535 byte source size

REGISTER 9-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	—	—	—	—	—	—	—	—		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:10	—	—	—	—	—	—	—	—		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	CHDSIZ<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				CHDSIZ	<u>/</u> <7:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
	—	—	—	—	—	—	—	—			
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	_	—	—	—			
45.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
15:8	CHSPTR<15:8>										
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
7:0		CHSPTR<7:0>									

REGISTER 9-14: DCHxSPTR: DMA CHANNEL 'x' SOURCE POINTER REGISTER

Legend:

0			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSPTR<15:0>: Channel Source Pointer bits

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 9-15: DCHxDPTR: DMA CHANNEL 'x' DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24		—	—	—	—	—	—	_
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10		—	—	—	—	—	—	_
15.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
10.0				CHDPTR	<15:8>			
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7:0				CHDPTF	R<7:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16	Unimplemented: Read as '0'
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bit 15-0 CHDPTR<15:0>: Channel Destination Pointer bits

1111111111111111 = Points to byte 65,535 of the destination

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—		—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	_	_	_		_	—	_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	-	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

REGISTER 10-4: U1OTGCON: USB OTG CONTROL REGISTER

Legend:

bit

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

7	DPF	PUL	UP	: D+	Pull-Up	Enable	bit	
	-	D .						

1 = D+ data line pull-up resistor is enabled
 0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit

- to **DMPOLOP:** D- Pull-Op Enable bit
 - 1 = D- data line pull-up resistor is enabled
 0 = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit

1 = D+ data line pull-down resistor is enabled
 0 = D+ data line pull-down resistor is disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit

- 1 = D- data line pull-down resistor is enabled
- 0 = D- data line pull-down resistor is disabled
- bit 3 **VBUSON:** VBUS Power-on bit
 - 1 = VBUS line is powered
 - 0 = VBUS line is not powered
- bit 2 **OTGEN:** OTG Functionality Enable bit
 - 1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control
 - 0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 VBUSCHG: VBUS Charge Enable bit

- 1 = VBUS line is charged through a pull-up resistor
- 0 = VBUS line is not charged through a resistor
- bit 0 VBUSDIS: VBUS Discharge Enable bit
 - 1 = VBUS line is discharged through a pull-down resistor
 - 0 = VBUS line is not discharged through a resistor

13.0 TIMER2/3, TIMER4/5

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a freerunning interval timer for various timing applications and counting external events. The following modes are supported:

- · Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- Synchronous external 16-bit timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

- · Synchronous internal 32-bit timer
- Synchronous internal 32-bit gated timer
- · Synchronous external 32-bit timer
- Note: In this chapter, references to registers, TxCON, TMRx and PRx, use 'x' to represent Timer2 through 5 in 16-bit modes. In 32-bit modes, 'x' represents Timer2 or 4; 'y' represents Timer3 or 5.

13.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 and Timer3 only)
- ADC event trigger (Timer3 in 16-bit mode, Timer2/ 3 in 32-bit mode)
- Fast bit manipulation using CLR, SET and INV registers

FIGURE 13-1: TIMER2, 3, 4, 5 BLOCK DIAGRAM (16-BIT)



14.0 WATCHDOG TIMER (WDT)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 9. "Watchdog, Deadman, and Power-up Timers" (DS60001114) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The Watchdog Timer (WDT), when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- · Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle



FIGURE 14-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM

NOTES:

18.0 INTER-INTEGRATED CIRCUIT (I²C)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 24. "Inter-Integrated Circuit (I²C)" (DS60001116) in the "*PIC32 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com/PIC32). The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard. Figure 18-1 illustrates the I^2C module block diagram.

Each I^2C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I²C module offers the following key features:

- I²C interface supporting both master and slave operation
- I²C Slave mode supports 7-bit and 10-bit addressing
- I²C Master mode supports 7-bit and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	-	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	_	—	—	—	—	—
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	PTEN<1	5:14> ⁽¹⁾			PTEN	<13:8>		
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0			PTEN	<7:2>			PTEN<	<1:0> ⁽²⁾

REGISTER 20-6: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

Legend:

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Write '0'; ignore read

- bit 15-14 **PTEN<15:14>:** PMCSx Address Port Enable bits
 - 1 = PMA15 and PMA14 function as either PMA<15:14> or PMCS2 and PMCS1⁽¹⁾
 - 0 = PMA15 and PMA14 function as port I/O
- bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
 - 1 = PMA<13:2> function as PMP address lines
 - 0 = PMA<13:2> function as port I/O
- bit 1-0 **PTEN<1:0>:** PMALH/PMALL Address Port Enable bits
 - 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL⁽²⁾
 - 0 = PMA1 and PMA0 pads function as port I/O
- Note 1: The use of these pins as PMA15/PMA14 or CS2/CS1 is selected by the CSF<1:0> bits (PMCON<7:6>).
 - 2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by the ADRMUX<1:0> bits in the PMCON register.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
31.24	—	—	—	—	—	—	CAL<9):8>
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10				CAL<	:7:0>			
15.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
10.0	ON ^(1,2)	—	SIDL	—	—	—	—	-
7.0	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0
7.0	RTSECSEL ⁽³⁾	RTCCLKON	_	—	RTCWREN ⁽⁴⁾	RTCSYNC	HALFSEC ⁽⁵⁾	RTCOE

REGISTER 21-1: RTCCON: RTC CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 Unimplemented: Read as '0'

bit 25-16 CAL<9:0>: RTC Drift Calibration bits, which contain a signed 10-bit integer value 0111111111 = Maximum positive adjustment, adds 511 RTC clock pulses every one minute 000000001 = Minimum positive adjustment, adds 1 RTC clock pulse every one minute 000000000 = No adjustment 1111111111 = Minimum negative adjustment, subtracts 1 RTC clock pulse every one minute 100000000 = Maximum negative adjustment, subtracts 512 clock pulses every one minute ON: RTCC On bit^(1,2) bit 15 1 = RTCC module is enabled 0 = RTCC module is disabled bit 14 Unimplemented: Read as '0' bit 13 SIDL: Stop in Idle Mode bit 1 = Disables the PBCLK to the RTCC when CPU enters in Idle mode 0 = Continue normal operation in Idle mode Unimplemented: Read as '0' bit 12-8 bit 7 RTSECSEL: RTCC Seconds Clock Output Select bit⁽³⁾ 1 = RTCC Seconds Clock is selected for the RTCC pin 0 = RTCC Alarm Pulse is selected for the RTCC pin bit 6 RTCCLKON: RTCC Clock Enable Status bit 1 = RTCC Clock is actively running 0 = RTCC Clock is not running bit 5-4 Unimplemented: Read as '0' **Note 1:** The ON bit is only writable when RTCWREN = 1. 2: When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit. 3: Requires RTCOE = 1 (RTCCON<0>) for the output to be active. 4: The RTCWREN bit can be set only when the write sequence is enabled. 5: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>). Note: This register is reset only on a Power-on Reset (POR).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	31:24 FLTEN11 MSEL11<1:0>			F	SEL11<4:0>			
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	FLTEN10	MSEL1	0<1:0>		F	SEL10<4:0>		
15:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTEN9		MSEL	9<1:0>		F	SEL9<4:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	FLTEN8	MSEL	8<1:0>		F	SEL8<4:0>		

REGISTER 23-12: C1FLTCON2: CAN FILTER CONTROL REGISTER 2

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	FLTEN11: Filter 11 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 30-29	MSEL11<1:0>: Filter 11 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected
bit 28-24	FSEL11<4:0>: FIFO Selection bits
	11111 = Reserved
	•
	•
	• 10000 - Reserved
	01111 = Message matching filter is stored in EIEO buffer 15
	•
	•
	00000 = Message matching filter is stored in FIFO buffer 0
bit 23	FLTEN10: Filter 10 Enable bit
	1 = Filter is enabled
	0 = Filter is disabled
bit 22-21	MSEL10<1:0>: Filter 10 Mask Select bits
	11 = Acceptance Mask 3 selected
	10 = Acceptance Mask 2 selected
	01 = Acceptance Mask 1 selected
	00 = Acceptance Mask 0 selected

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	R-x	R-x									
31.24	C1FIFOUAn<31:24>										
00.40	R-x	R-x									
23.10	C1FIFOUAn<23:16>										
15.0	R-x	R-x									
15.0	C1FIFOUAn<15:8>										
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-0 ⁽¹⁾	R-0 ⁽¹⁾			
				C1FIFOL	JAn<7:0>						

REGISTER 23-18: C1FIFOUAn: CAN FIFO USER ADDRESS REGISTER 'n' ('n' = 0 THROUGH 15)

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 C1FIFOUAn<31:0>: CAN FIFO User Address bits

TXEN = 1: (FIFO configured as a transmit buffer)

A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0: (FIFO configured as a receive buffer)

A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This bit will always read '0', which forces byte-alignment of messages.

Note: This register is not guaranteed to read correctly in Configuration mode, and should only be accessed when the module is not in Configuration mode.

REGISTER 23-19: C1FIFOCIn: CAN MODULE MESSAGE INDEX REGISTER 'n' ('n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
51.24	—	—	—	—	—	—	_	—			
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—	—	_	—			
15.9	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
15:8	—	—	—	—	—	—	_	—			
7:0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0			
	_	_	_	C1FIFOCIn<4:0>							

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-5 Unimplemented: Read as '0'

bit 4-0 C1FIFOCIn<4:0>: CAN Side FIFO Message Index bits

TXEN = 1: (FIFO configured as a transmit buffer)

A read of this register will return an index to the message that the FIFO will next attempt to transmit.

TXEN = 0: (FIFO configured as a receive buffer)

A read of this register will return an index to the message that the FIFO will use to save the next message.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24	—	—	—	—	—	-		—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	_	—	—	—	_				
15.0	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	
10.0	—	—	SIDL	—	—	—	—	—	
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	
	_	_	_	_	_	C3OUT	C2OUT	C10UT	

REGISTER 24-2: CMSTAT: COMPARATOR STATUS REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 Unimplemented: Read as '0'

bit 13 **SIDL:** Stop in IDLE Control bit

1 = All Comparator modules are disabled in IDLE mode

0 = All Comparator modules continue to operate in the IDLE mode

bit 12-3 Unimplemented: Read as '0'

- bit 2 C3OUT: Comparator Output bit
 - 1 = Output of Comparator 3 is a '1'
 - 0 = Output of Comparator 3 is a '0'

bit 1 C2OUT: Comparator Output bit

- 1 = Output of Comparator 2 is a '1'
- 0 = Output of Comparator 2 is a '0'

bit 0 **C1OUT:** Comparator Output bit

- 1 = Output of Comparator 1 is a '1'
- 0 = Output of Comparator 1 is a '0'

26.1 Control Registers

TABLE 26-1: CTMU REGISTER MAP

ess		•		Bits															
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
1200		31:16	EDG1MOD	EDG1POL		EDG15	SEL<3:0>		EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL		EDG28	SEL<3:0>		_	_	0000
A200	CTWOCON	15:0	ON	_	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG			ITRIM	<5:0>			IRNG	<1:0>	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

TABLE 31-34:	ADC MODULE SPECIFICATIONS (CONTINUED)
--------------	---------------------------------------

	AC CHAR	ACTERISTICS	Standard C (unless oth Operating to	Pperating C nerwise stat emperature	onditions (set ted) -40°C ≤ TA -40°C ≤ TA	ee Note ≤ +85° ≤ +105	e 5): 2.5V to 3.6V C for Industrial °C for V-temp
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
ADC Ac	curacy – N	leasurements with Inter	nal VREF+/V	REF-			
AD20d	Nr	Resolution		10 data bits	3	bits	(Note 3)
AD21d	INL	Integral Non-linearity	> -1	_	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)
AD22d	DNL	Differential Non-linearity	> -1	_	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Notes 2,3)
AD23d	Gerr	Gain Error	> -4	_	< 4	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)
AD24d	Eoff	Offset Error	> -2	_	< 2	Lsb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)
AD25d		Monotonicity	—	—		_	Guaranteed
Dynami	ic Performa	ance	·				·
AD32b	SINAD	Signal to Noise and Distortion	55	55 58.5 -		dB	(Notes 3,4)
AD34b	ENOB	Effective Number of bits	9.0	9.5	_	bits	(Notes 3,4)

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.