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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx550f256h-i-mr

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP			
RTCC	42	68	O	—	Real-Time Clock Alarm Output
CVREFOUT	23	34	O	Analog	Comparator Voltage Reference (Output)
C1INA	11	20	I	Analog	Comparator 1 Inputs
C1INB	12	21	I	Analog	
C1INC	5	11	I	Analog	
C1IND	4	10	I	Analog	
C2INA	13	22	I	Analog	Comparator 2 Inputs
C2INB	14	23	I	Analog	
C2INC	8	14	I	Analog	
C2IND	6	12	I	Analog	
C3INA	58	87	I	Analog	Comparator 3 Inputs
C3INB	55	84	I	Analog	
C3INC	54	83	I	Analog	
C3IND	51	78	I	Analog	
C1OUT	PPS	PPS	O	—	Comparator 1 Output
C2OUT	PPS	PPS	O	—	Comparator 2 Output
C3OUT	PPS	PPS	O	—	Comparator 3 Output
PMALL	30	44	O	TTL/ST	Parallel Master Port Address Latch Enable Low Byte
PMALH	29	43	O	TTL/ST	Parallel Master Port Address Latch Enable High Byte
PMA0	30	44	O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)
PMA1	29	43	O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)

Legend: CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

- Note 1:** This pin is only available on devices without a USB module.
2: This pin is only available on devices with a USB module.
3: This pin is not available on 64-pin devices with a USB module.
4: This pin is only available on 100-pin devices without a USB module.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32® architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e®, is also available by accessing the CP0 registers, listed in Table 3-2.

TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers.
8	BadVAddr ⁽¹⁾	Reports the address for the most recent address-related exception.
9	Count ⁽¹⁾	Processor cycle count.
10	Reserved	Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core.
11	Compare ⁽¹⁾	Timer interrupt control.
12	Status ⁽¹⁾	Processor status and control.
12	IntCtl ⁽¹⁾	Interrupt system status and control.
13	Cause ⁽¹⁾	Cause of last general exception.
14	EPC ⁽¹⁾	Program counter at last exception.
15	PRId	Processor identification and revision.
15	EBASE	Exception vector base register.
16	Config	Configuration register.
16	Config1	Configuration register 1.
16	Config2	Configuration register 2.
16	Config3	Configuration register 3.
17-22	Reserved	Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core.
23	Debug ⁽²⁾	Debug control and exception status.
24	DEPC ⁽²⁾	Program counter at last debug exception.
25-29	Reserved	Reserved in the PIC32MX1XX/2XX/5XX 64/100-pin family core.
30	ErrorEPC ⁽¹⁾	Program counter at last error.
31	DESAVE ⁽²⁾	Debug handler scratchpad register.

Note 1: Registers used in exception processing.

2: Registers used during debug.

7.1 Control Registers

TABLE 7-1: RESET SFR SUMMARY

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F600	RCON	31:16	—	—	HVDR	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CMR	VREGS	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	xxxx ⁽¹⁾
F610	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000

Legend: — = unimplemented, read as '0'. Address offset values are shown in hexadecimal.

Note 1: The Reset value is dependent on the DEVCFGx Configuration bits and the type of reset.

TABLE 9-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3060	DCH0CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	—	0000
3070	DCH0ECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FFF8
3080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3090	DCH0SSA	31:16	CHSSA<31:0>																0000
		15:0	CHSSA<31:0>																0000
30A0	DCH0DSA	31:16	CHDSA<31:0>																0000
		15:0	CHDSA<31:0>																0000
30B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
30C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
30D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
30E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
30F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3120	DCH1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	—	0000
3130	DCH1ECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FFF8
3140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3150	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0	CHSSA<31:0>																0000
3160	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0	CHDSA<31:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.

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REGISTER 9-16: DCHxCSIZ: DMA CHANNEL 'x' CELL-SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>:** Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event

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0000000000000010 = 2 bytes transferred on an event

0000000000000001 = 1 byte transferred on an event

0000000000000000 = 65,536 bytes transferred on an event

REGISTER 9-17: DCHxCPTR: DMA CHANNEL 'x' CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<7:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event

.

.

.

0000000000000001 = 1 byte has been transferred since the last event

0000000000000000 = 0 bytes have been transferred since the last event

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

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REGISTER 10-4: U1OTGCON: USB OTG CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **DPPULUP:** D+ Pull-Up Enable bit

1 = D+ data line pull-up resistor is enabled

0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit

1 = D- data line pull-up resistor is enabled

0 = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit

1 = D+ data line pull-down resistor is enabled

0 = D+ data line pull-down resistor is disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit

1 = D- data line pull-down resistor is enabled

0 = D- data line pull-down resistor is disabled

bit 3 **VBUSON:** VBUS Power-on bit

1 = VBUS line is powered

0 = VBUS line is not powered

bit 2 **OTGEN:** OTG Functionality Enable bit

1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control

0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 **VBUSCHG:** VBUS Charge Enable bit

1 = VBUS line is charged through a pull-up resistor

0 = VBUS line is not charged through a resistor

bit 0 **VBUSDIS:** VBUS Discharge Enable bit

1 = VBUS line is discharged through a pull-down resistor

0 = VBUS line is not discharged through a resistor

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 10-6: U1IR: USB INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R-0	R/WC-0, HS
	STALLIF	ATTACHIF ⁽¹⁾	RESUMEIF ⁽²⁾	IDLEIF	TRNIF ⁽³⁾	SOFIF	UERRIF ⁽⁴⁾	URSTIF ⁽⁵⁾
								DETACHIF ⁽⁶⁾

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit

1 = In Host mode, a STALL handshake was received during the handshake phase of the transaction

In Device mode, a STALL handshake was transmitted during the handshake phase of the transaction

0 = STALL handshake has not been sent

bit 6 **ATTACHIF:** Peripheral Attach Interrupt bit⁽¹⁾

1 = Peripheral attachment was detected by the USB module

0 = Peripheral attachment was not detected

bit 5 **RESUMEIF:** Resume Interrupt bit⁽²⁾

1 = K-State is observed on the D+ or D- pin for 2.5 μ s

0 = K-State is not observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit

1 = Idle condition detected (constant Idle state of 3 ms or more)

0 = No Idle condition detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit⁽³⁾

1 = Processing of current token is complete; a read of the U1STAT register will provide endpoint information

0 = Processing of current token not complete

bit 2 **SOFIF:** SOF Token Interrupt bit

1 = SOF token received by the peripheral or the SOF threshold reached by the host

0 = SOF token was not received nor threshold reached

bit 1 **UERRIF:** USB Error Condition Interrupt bit⁽⁴⁾

1 = Unmasked error condition has occurred

0 = Unmasked error condition has not occurred

bit 0 **URSTIF:** USB Reset Interrupt bit (Device mode)⁽⁵⁾

1 = Valid USB Reset has occurred

0 = No USB Reset has occurred

bit 0 **DETACHIF:** USB Detach Interrupt bit (Host mode)⁽⁶⁾

1 = Peripheral detachment was detected by the USB module

0 = Peripheral detachment was not detected

Note 1: This bit is valid only if the HOSTEN bit is set (see Register 10-11), there is no activity on the USB for 2.5 μ s, and the current bus state is not SE0.

2: When not in Suspend mode, this interrupt should be disabled.

3: Clearing this bit will cause the STAT FIFO to advance.

4: Only error conditions enabled through the U1EIE register will set this bit.

5: Device mode.

6: Host mode.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 10-10: U1STAT: USB STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	U-0	U-0
	ENDPT<3:0>				DIR	PPBI	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits
(Represents the number of the BDT, updated by the last USB transfer.)

1111 = Endpoint 15

1110 = Endpoint 14

.

.

.

0001 = Endpoint 1

0000 = Endpoint 0

bit 3 **DIR:** Last BD Direction Indicator bit

1 = Last transaction was a transmit transfer (TX)

0 = Last transaction was a receive transfer (RX)

bit 2 **PPBI:** Ping-Pong BD Pointer Indicator bit

1 = The last transaction was to the ODD BD bank

0 = The last transaction was to the EVEN BD bank

bit 1-0 **Unimplemented:** Read as '0'

Note: The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. U1STAT value is only valid when the TRNIF bit (U1IR<3>) is active. Clearing the TRNIF bit advances the FIFO. Data in register is invalid when the TRNIF bit = 0.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 10-11: U1CON: USB CONTROL REGISTER (CONTINUED)

- bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
 1 = Reset all Even/Odd buffer pointers to the EVEN BD banks
 0 = Even/Odd buffer pointers not being Reset
- bit 0 **USBEN:** USB Module Enable bit⁽⁴⁾
 1 = USB module and supporting circuitry enabled
 0 = USB module and supporting circuitry disabled
- SOFEN:** SOF Enable bit⁽⁵⁾
 1 = SOF token sent every 1 ms
 0 = SOF token disabled

- Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).
- 2:** All host control logic is reset any time that the value of this bit is toggled.
- 3:** Software must set the RESUME bit for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.
- 4:** Device mode.
- 5:** Host mode.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 15-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER ('x' = 1 THROUGH 5)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON ⁽¹⁾	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit

-n = Bit Value at POR: ('0', '1', x = unknown)

P = Programmable bit r = Reserved bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit⁽¹⁾

1 = Module enabled

0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit

1 = Halt in CPU Idle mode

0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)

1 = Capture rising edge first

0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit

1 = 32-bit timer resource capture

0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')

0 = Timer3 is the counter source for capture

1 = Timer2 is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits

11 = Interrupt on every fourth capture event

10 = Interrupt on every third capture event

01 = Interrupt on every second capture event

00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)

1 = Input capture overflow occurred

0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)

1 = Input capture buffer is not empty; at least one more capture value can be read

0 = Input capture buffer is empty

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

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REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER (CONTINUED)

- bit 3 **SPITBE:** SPI Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB is empty
0 = Transmit buffer, SPIxTXB is not empty
Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.
Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **SPITBF:** SPI Transmit Buffer Full Status bit
1 = Transmit not yet started, SPITXB is full
0 = Transmit buffer is not full
Standard Buffer Mode:
Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB.
Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR.
Enhanced Buffer Mode:
Set when CWPTR + 1 = SRPTR; cleared otherwise
- bit 0 **SPIRBF:** SPI Receive Buffer Full Status bit
1 = Receive buffer, SPIxRXB is full
0 = Receive buffer, SPIxRXB is not full
Standard Buffer Mode:
Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB.
Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer Mode:
Set when SWPTR + 1 = CRPTR; cleared otherwise

18.0 INTER-INTEGRATED CIRCUIT (I²C)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. “Inter-Integrated Circuit (I²C)”** (DS60001116) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard. Figure 18-1 illustrates the I²C module block diagram.

Each I²C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I²C module offers the following key features:

- I²C interface supporting both master and slave operation
- I²C Slave mode supports 7-bit and 10-bit addressing
- I²C Master mode supports 7-bit and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking

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REGISTER 18-1: I2CxCON: I²C ‘x’ CONTROL REGISTER (‘x’ = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ON ⁽¹⁾	U-0 —	R/W-0 SIDL	R/W-1, HC SCLREL	R/W-0 STRICT	R/W-0 A10M	R/W-0 DISSLW	R/W-0 SMEN
7:0	R/W-0 GCEN	R/W-0 STREN	R/W-0 ACKDT	R/W-0, HC ACKEN	R/W-0, HC RCEN	R/W-0, HC PEN	R/W-0, HC RSEN	R/W-0, HC SEN

Legend:	HC = Cleared in Hardware
R = Readable bit	W = Writable bit
-n = Value at POR	‘1’ = Bit is set
	‘0’ = Bit is cleared
	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** I²C Enable bit⁽¹⁾

- 1 = Enables the I²C module and configures the SDA and SCL pins as serial port pins
- 0 = Disables the I²C module; all I²C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Mode bit

- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)

- 1 = Release SCLx clock
- 0 = Hold SCLx clock low (clock stretch)

If STREN = 1:

Bit is R/W (i.e., software can write ‘0’ to initiate stretch and write ‘1’ to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:

Bit is R/S (i.e., software can only write ‘1’ to release clock). Hardware clear at beginning of slave transmission.

bit 11 **STRICT:** Strict I²C Reserved Address Rule Enable bit

- 1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
- 0 = Strict I²C Reserved Address Rule not enabled

bit 10 **A10M:** 10-bit Slave Address bit

- 1 = I2CxADD is a 10-bit slave address
- 0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit

- 1 = Slew rate control disabled
- 0 = Slew rate control enabled

bit 8 **SMEN:** SMBus Input Levels bit

- 1 = Enable I/O pin thresholds compliant with SMBus specification
- 0 = Disable SMBus input thresholds

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

19.1 Control Registers

TABLE 19-1: UART1 THROUGH UART5 REGISTER MAP

Virtual Address (BF80-#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	U1MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6010	U1STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	FFFF
6020	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6030	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6040	U1BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
6200	U2MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6210	U2STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	FFFF
6220	U2TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6230	U2RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6240	U2BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
6400	U3MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
6410	U3STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	FFFF
6420	U3TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6430	U3RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.
- 2: This register is only available on 100-pin devices.

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REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN ^(1,2)	CHIME ⁽²⁾	PIV ⁽²⁾	ALRMSYNC ⁽³⁾	AMASK<3:0> ⁽³⁾			
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARPT<7:0> ⁽³⁾							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit^(1,2)

1 = Alarm is enabled

0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit⁽²⁾

1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF

0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit⁽²⁾

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.

When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit⁽³⁾

1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read.

The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain

0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits⁽³⁾

0000 = Every half-second

0001 = Every second

0010 = Every 10 seconds

0011 = Every minute

0100 = Every 10 minutes

0101 = Every hour

0110 = Once a day

0111 = Once a week

1000 = Once a month

1001 = Once a year (except when configured for February 29, once every four years)

1010 = Reserved; do not use

1011 = Reserved; do not use

11xx = Reserved; do not use

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

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REGISTER 21-5: ALRMTIME: ALARM TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **HR10<3:0>**: Binary Coded Decimal value of hours bits, 10s place digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>**: Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>**: Binary Coded Decimal value of minutes bits, 10s place digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>**: Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>**: Binary Coded Decimal value of seconds bits, 10s place digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>**: Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 **Unimplemented**: Read as '0'

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REGISTER 23-4: C1VEC: CAN INTERRUPT CODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	FILHIT<4:0>				
7:0	U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
	—	ICODE<6:0> ⁽¹⁾						

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>**: Filter Hit Number bit

11111 = Reserved

•
•
•

10000 = Reserved

01111 = Filter 15

•
•
•

00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>**: Interrupt Flag Code bits⁽¹⁾

1111111 = Reserved

•
•
•

1001001 = Reserved

1001000 = Invalid message received (IVRIF)

1000111 = CAN module mode change (MODIF)

1000110 = CAN timestamp timer (CTMRIF)

1000101 = Bus bandwidth error (SERRIF)

1000100 = Address error interrupt (SERRIF)

1000011 = Receive FIFO overflow interrupt (RBOVIF)

1000010 = Wake-up interrupt (WAKIF)

1000001 = Error Interrupt (CERRIF)

1000000 = No interrupt

0111111 = Reserved

•
•
•

0010000 = Reserved

0001111 = FIFO15 Interrupt (C1FSTAT<15> set)

•
•
•

0000000 = FIFO0 Interrupt (C1FSTAT<0> set)

Note 1: These bits are only updated for enabled interrupts.

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28.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. “Watchdog Timer and Power-up Timer”** (DS60001114), **Section 32. “Configuration”** (DS60001124) and **Section 33. “Programming and Diagnostics”** (DS60001129) in the *“PIC32 Family Reference Manual”*, which are available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX1XX/2XX/5XX 64/100-pin devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible device configuration
- Watchdog Timer (WDT)
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)

28.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- CFGCON: Configuration Control Register

In addition, the DEVID register (Register 28-6) provides device and revision information.

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TABLE 31-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	— —	40 40	MHz MHz	EC (Note 4) ECPLL (Note 3)
OS11		Oscillator Crystal Frequency	3	—	10	MHz	XT (Note 4)
OS12			4	—	10	MHz	XTPLL (Notes 3,4)
OS13			10	—	25	MHz	HS (Note 5)
OS14			10	—	25	MHz	HSPLL (Notes 3,4)
OS15			32	32.768	100	kHz	Sosc (Note 4)
OS20	Tosc	Tosc = 1/Fosc = Tcy (Note 2)	—	—	—	—	See parameter OS10 for Fosc value
OS30	TosL, TosH	External Clock In (OSC1) High or Low Time	0.45 x Tosc	—	—	ns	EC (Note 4)
OS31	TosR, TosF	External Clock In (OSC1) Rise or Fall Time	—	—	0.05 x Tosc	ns	EC (Note 4)
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and Sosc Clock Oscillator modes)	—	1024	—	Tosc	(Note 4)
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	(Note 4)
OS42	GM	External Oscillator Transconductance (Primary Oscillator only)	—	12	—	mA/V	VDD = 3.3V, TA = +25°C (Note 4)

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

- 2:** Instruction cycle period (Tcy) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKI pin.
- 3:** PLL input requirements: 4 MHz ≤ F_{PLLIN} ≤ 5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.
- 4:** This parameter is characterized, but not tested in manufacturing.

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TABLE 31-36: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period ⁽²⁾	65	—	—	ns	See Table 31-35
Conversion Rate							
AD55	TCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate (Sampling Speed)	—	—	1000	ksps	AVDD = 3.0V to 3.6V
			—	—	400	ksps	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	1 TAD	—	—	—	TSAMP must be ≥ 132 ns
Timing Parameters							
AD60	TPCS	Conversion Start from Sample Trigger ⁽³⁾	—	1.0 TAD	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD	—	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1) ⁽³⁾	—	0.5 TAD	—	—	—
AD63	TDPU	Time to Stabilize Analog Stage from ADC Off to ADC On ⁽³⁾	—	—	2	μs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: Characterized by design but not tested.

4: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.