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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx570f512ht-v-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

	Pin N	umber			
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	Pin Type	Buffer Type	Description
AN0	16	25	I	Analog	
AN1	15	24	Ι	Analog	
AN2	14	23	Ι	Analog	
AN3	13	22	I	Analog	
AN4	12	21	I	Analog	
AN5	11	20	Ι	Analog	
AN6	17	26	I	Analog	
AN7	18	27	I	Analog	
AN8	21	32	Ι	Analog	
AN9	22	33	Ι	Analog	
AN10	23	34	Ι	Analog	
AN11	24	35	I	Analog	
AN12	27	41	Ι	Analog	
AN13	28	42	I	Analog	
AN14	29	43	I	Analog	
AN15	30	44	I	Analog	
AN16	4	10	I	Analog	
AN17	5	11	I	Analog	
AN18	6	12	I	Analog	
AN19	8	14	Ι	Analog	
AN20	62	98	I	Analog	
AN21	64	100	I	Analog	
AN22	1	3	Ι	Analog	
AN23	2	4	Ι	Analog	
AN24	49	76	Ι	Analog	
AN25	50	77	Ι	Analog	
AN26	51	78	Ι	Analog	
AN27	3	5	Ι	Analog	
AN28	—	1	Ι	Analog	
AN29	—	6	Ι	Analog	
AN30	—	7	Ι	Analog	
AN31		8	Ι	Analog	
AN32		18	Ι	Analog	
AN33	_	19	I	Analog	
AN34	_	39	I	Analog	
AN35	_	40	I	Analog	
Legend:	CMOS = CN	IOS compat	ible inpu	it or output	Analog = Analog input I = Input O = Output

TABLE 1-1:PINOUT I/O DESCRIPTIONS

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

	Pin N	umber								
_	64		Pin	Buffer						
Pin Name	QFN/ TQFP	100-pin TQFP	Туре	Туре	Description					
RC1	_	6	I/O	ST						
RC2	_	7	I/O	ST						
RC3	_	8	I/O	ST						
RC4	_	9	I/O	ST						
RC12	39	63	I/O	ST	PORIC is a didirectional I/O port					
RC13	47	73	I/O	ST						
RC14	48	74	I/O	ST						
RC15	40	64	I/O	ST						
RD0	46	72	I/O	ST						
RD1	49	76	I/O	ST						
RD2	50	77	I/O	ST						
RD3	51	78	I/O	ST						
RD4	52	81	I/O	ST						
RD5	53	82	I/O	ST						
RD6	54	83	I/O	ST						
RD7	55	84	I/O	ST						
RD8	42	68	I/O	ST	PORTD is a bidirectional I/O port					
RD9	43	69	I/O	ST						
RD10	44	70	I/O	ST						
RD11	45	71	I/O	ST						
RD12	_	79	I/O	ST						
RD13	_	80	I/O	ST						
RD14	_	47	I/O	ST						
RD15	_	48	I/O	ST						
RE0	60	93	I/O	ST						
RE1	61	94	I/O	ST						
RE2	62	98	I/O	ST						
RE3	63	99	I/O	ST						
RE4	64	100	I/O	ST	DORTE is a hidiractional I/O part					
RE5	1	3	I/O	ST						
RE6	2	4	I/O	ST	_					
RE7	3	5	I/O	ST	\neg					
RE8	_	18	I/O	ST						
RE9		19	I/O	ST						
Legend:	CMOS = CN	IOS compat	ible inpu	it or output	Analog = Analog input I = Input O = Output					
	ST = Schmit	tt Trigger inp	out with (CMOS leve	Is TTL = TTL input buffer P = Power					
Note 1:	This pin is o	nly available	on dev	ices withou	t a USB module.					

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices with a USB module.

4: This pin is only available on 100-pin devices without a USB module.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial ProgrammingTM (ICSPTM) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input voltage low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB[®] ICD 3 or MPLAB REAL ICE[™].

For more information on MPLAB ICD 3 and MPLAB REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB[®] ICD 3"* (poster) DS50001765
- "MPLAB[®] ICD 3 Design Advisory" DS50001764
- *"MPLAB[®] REAL ICE™ In-Circuit Debugger User's Guide"* DS50001616
- *"Using MPLAB[®] REAL ICE™ Emulator"* (poster) DS50001749

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer or debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input voltage low (VIL) requirements

2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR





FIGURE 4-4: MEMORY MAP FOR DEVICES WITH 512 KB OF PROGRAM MEMORY + 64 KB RAM

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documentation for information).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24 23:16	ROTRIM<8:1>										
00.40	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:10	ROTRIM<0>	—	—	—	—	—	—	—			
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
15:8	—	—	—	—	—	—	—	—			
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
7:0	_	_	—	_	_	_	_	_			

REGISTER 8-4: REFOTRIM: REFERENCE OSCILLATOR TRIM REGISTER

Legend:	y = Value set from Configuration bits on POR						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-23 ROTRIM<8:0>: Reference Oscillator Trim bits

Note: While the ON bit (REFOCON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 10-10: U1STAT: USB STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24 23:16	—	—		—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—		—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—		—	—	—	—	—
7.0	R-x	R-x	R-x	R-x	R-x	R-x	U-0	U-0
Range 31:24 23:16 15:8 7:0		ENDP.	T<3:0>		DIR	PPBI	_	_

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits (Represents the number of the BDT, updated by the last USB transfer.)
 - 1111 = Endpoint 15 1110 = Endpoint 14 . . 0001 = Endpoint 1 0000 = Endpoint 0
- bit 3 **DIR:** Last BD Direction Indicator bit
 - 1 = Last transaction was a transmit transfer (TX)
 - 0 = Last transaction was a receive transfer (RX)
- bit 2 **PPBI:** Ping-Pong BD Pointer Indicator bit
 - 1 = The last transaction was to the ODD BD bank
 - 0 = The last transaction was to the EVEN BD bank
- bit 1-0 Unimplemented: Read as '0'

Note: The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. U1STAT value is only valid when the TRNIF bit (U1IR<3>) is active. Clearing the TRNIF bit advances the FIFO. Data in register is invalid when the TRNIF bit = 0.

TABLE 11-2: OUTPUT PIN SELECTION (CONTINUED)

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD9	RPD9R	RPD9R<3:0>	0000 = No Connect
RPG6	RPG6R	RPG6R<3:0>	0001 = U3RTS
RPB8	RPB8R	RPB8R<3:0>	0010 = U4TX
RPB15	RPB15R	RPB15R<3:0>	0011 = REFCLKO
RPD4	RPD4R	RPD4R<3:0>	0101 = Reserved
RPB0	RPB0R	RPB0R<3:0>	0110 = Reserved
RPE3	RPE3R	RPE3R<3:0>	0111 = SS1
RPB7	RPB7R	RPB7R<3:0>	1000 = SDO1
RPB2	RPB2R	RPB2R<3:0>	1001 = Reserved
RPF12 ⁽³⁾	RPF12R	RPF12R<3:0>	1010 = Reserved
RPD12 ⁽³⁾	RPD12R	RPD12R<3:0>	1011 = 005 1100 = Reserved
RPF8 ⁽³⁾	RPF8R	RPF8R<3:0>	1101 = C1OUT
RPC3 ⁽³⁾	RPC3R	RPC3R<3:0>	1110 = SS3
RPE9 ⁽³⁾	RPE9R	RPE9R<3:0>	1111 = SS4⁽³⁾
RPD1	RPD1R	RPD1R<3:0>	0000 = <u>No Connect</u>
RPG9	RPG9R	RPG9R<3:0>	0001 = U2RTS
RPB14	RPB14R	RPB14R<3:0>	10010 = Reserved $10011 = \overline{\text{U1RTS}}$
RPD0	RPD0R	RPD0R<3:0>	$0100 = U5TX^{(3)}$
RPD8	RPD8R	RPD8R<3:0>	0101 = Reserved
RPB6	RPB6R	RPB6R<3:0>	0110 = SS2
RPD5	RPD5R	RPD5R<3:0>	1000 = SDO1
RPF3 ⁽¹⁾	RPF3R	RPF3R<3:0>	1001 = Reserved
RPF6 ⁽²⁾	RPF6R	RPF6R<3:0>	1010 = Reserved
RPF13 ⁽³⁾	RPF13R	RPF13R<3:0>	1011 = OC2
RPC2 ⁽³⁾	RPC2R	RPC2R<3:0>	1100 = OC1 1101 = Reserved
RPE8 ⁽³⁾	RPE8R	RPE8R<3:0>	1110 = Reserved
RPF2 ⁽¹⁾	RPF2R	RPF2R<3:0>	1111 = Reserved

Note 1: This selection is not available on 64-pin USB devices.

2: This selection is only available on 100-pin General Purpose devices.

3: This selection is not available on 64-pin devices.

4: This selection is not available when USBID functionality is used on USB devices.

5: This selection is not available on devices without a CAN module.

6: This selection is not available on USB devices.

7: This selection is not available when VBUSON functionality is used on USB devices.

-																			
ess										Bi	ts								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6510	TRISF	31:16	_	—	—	—	—	—	—	—		_		—	—	_	—	_	0000
		15:0	_	_	_	_	_	_	_	_	_	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	007F
6520	PORTE	31:16	—		—		—	_		—	—	_		_		—	—		0000
		15:0	—	_	—	_	—	_	_	—	_	RF6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6530		31:16	—	_	—	_	_	—	_	—	_	—	_	_		_	_	—	0000
0000	LAII	15:0	—	_	—	_	—	_	_	_	_	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6540	ODCE	31:16		-	-	-	—	-	-			—		-	—	-	-	—	0000
0540	ODCF	15:0		_	_	_	_	_	_	—	_	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000
0550		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6550	CNPUF	15:0	_		_		_	-		—		CNPUF6	CNPUF5	CNPUF4	CNPUF3	CNPUF2	CNPUF1	CNPUF0	0000
0500		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0000	CNPDF	15:0	_	_	_	_	_	_	_	_	_	CNPDF6	CNPDF5	CNPDF4	CNPDF3	CNPDF2	CNPDF1	CNPDF0	0000
6570		31:16	—	_	_	_	_	_	_	—	_	_	_	_	_	_	_	_	0000
0570	CINCOINF	15:0	ON	_	SIDL	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0500		31:16	_	_	_	_	_	_	_	_	_	_	_	_		_	_	—	0000
6580	CNENF	15:0	_	_	_	_	—	_	_	_	_	CNIEF6	CNIEF5	CNIEF4	CNIEF3	CNIEF2	CNIEF1	CNIEF0	0000
		31:16	_	_	_	_	—	_	_	_	_	_	_	_	—	_	_	_	0000
6590	CNSTATF	15:0	_	_	_	_	_		_			CN STATF6	CN STATF5	CN STATF4	CN STATF3	CN STATF2	CN STATF1	CN STATF0	0000

TABLE 11-13: PORTF REGISTER MAP FOR PIC32MX120F064H, PIC32MX130F128H, PIC32MX150F256H, AND PIC32MX170F512H DEVICES ONLY

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET, and INV Registers" for more information.

REGISTER 13-1: TxCON: TYPE B TIMER 'x' CONTROL REGISTER (CONTINUED)('x' = 2 THROUGH 5)

- bit 3 **T32:** 32-Bit Timer Mode Select bit⁽²⁾ 1 = Odd numbered and even numbered timers form a 32-bit timer 0 = Odd numbered and even numbered timers form a separate 16-bit timer
- bit 2 Unimplemented: Read as '0'
- bit 1 **TCS:** Timer Clock Source Select bit⁽³⁾
 - 1 = External clock from TxCK pin
 - 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit is available only on even numbered timers (Timer2 and Timer4).
 - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3 and Timer5). All timer functions are set through the even numbered timers.
 - 4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	-	—
00.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	_	—
15.0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7.0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7:0	AUDEN ⁽¹⁾			—	AUDMONO ^(1,2)		AUDMOD)<1:0>(1,2)

REGISTER 17-2: SPIxCON2: SPI CONTROL REGISTER 2

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

)'
)

- bit 15 SPISGNEXT: Sign Extend Read Data from the RX FIFO bit
 - 1 = Data from RX FIFO is sign extended
 - 0 = Data from RX FIFO is not sign extened

bit 14-13 Unimplemented: Read as '0'

- bit 12 FRMERREN: Enable Interrupt Events via FRMERR bit 1 = Frame Error overflow generates error events 0 = Frame Error does not generate error events bit 11 SPIROVEN: Enable Interrupt Events via SPIROV bit 1 = Receive overflow generates error events 0 = Receive overflow does not generate error events bit 10 SPITUREN: Enable Interrupt Events via SPITUR bit 1 = Transmit Underrun Generates Error Events 0 = Transmit Underrun Does Not Generates Error Events bit 9 IGNROV: Ignore Receive Overflow bit (for Audio Data Transmissions) 1 = A ROV is not a critical error; during ROV data in the fifo is not overwritten by receive data 0 = A ROV is a critical error which stop SPI operation bit 8 IGNTUR: Ignore Transmit Underrun bit (for Audio Data Transmissions) 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty 0 = A TUR is a critical error which stop SPI operation AUDEN: Enable Audio CODEC Support bit⁽¹⁾ bit 7 1 = Audio protocol enabled 0 = Audio protocol disabled bit 6-5 Unimplemented: Read as '0' AUDMONO: Transmit Audio Data Format bit^(1,2) bit 3 1 = Audio data is mono (Each data word is transmitted on both left and right channels) 0 = Audio data is stereo bit 2 Unimplemented: Read as '0' AUDMOD<1:0>: Audio Protocol Mode bit^(1,2) bit 1-0 11 = PCM/DSP mode 10 = Right Justified mode 01 = Left Justified mode $00 = I^2 S \mod I$
- **Note 1:** This bit can only be written when the ON bit = 0.
 - **2:** This bit is only valid for AUDEN = 1.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22:16	R/W-0, HC	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
23.10	RDSTART	—	—	—	—	—	DUALBUF	—
15.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	ON ⁽¹⁾	—	SIDL	ADRMU	JX<1:0>	PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
7.0	CSF<	1:0> (2)	ALP ⁽²⁾	CS2P ⁽²⁾	CS1P ⁽²⁾	—	WRSP	RDSP

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER

Legend:	HC = Hardware cleared			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-24 Unimplemented: Read as '0'

- bit 23 RDSTART: Start a Read on the PMP Bus bit⁽³⁾
 - 1 = Start a read cycle on the PMP bus
 - 0 = No effect

This bit is cleared by hardware at the end of the read cycle when the BUSY bit (PMMODE<15>) = 0.

bit 22-18 Unimplemented: Read as '0'

bit 17 **DUALBUF:** Parallel Master Port Dual Read/Write Buffer Enable bit

- This bit is only valid in Master mode.
- PMP uses separate registers for reads and writes Reads: PMRADDR and PMRDIN Writes: PMRWADDR and PMDOUT
- 0 = PMP uses legacy registers for reads and writes Reads/Writes: PMADDR and PMRDIN
- bit 16 Unimplemented: Read as '0'
- bit 15 **ON:** Parallel Master Port Enable bit⁽¹⁾
 - 1 = PMP enabled
 - 0 = PMP disabled, no off-chip access performed
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit

bit 10

- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

bit 12-11 ADRMUX<1:0>: Address/Data Multiplexing Selection bits

- 11 = Lower 8 bits of address are multiplexed on PMD<15:0> pins
- 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
- 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>
- 00 = Address and data appear on separate pins
- PMPTTL: PMP Module TTL Input Buffer Select bit
 - 1 = PMP module uses TTL input buffers
 - 0 = PMP module uses Schmitt Trigger input buffer
- bit 9 PTWREN: Write Enable Strobe Port Enable bit
 - 1 = PMWR/PMENB port enabled
 - 0 = PMWR/PMENB port disabled
 - **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.
 - **2:** These bits have no effect when their corresponding pins are used as address lines.

REGISTER 20-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

- bit 5-2 WAITM<3:0>: Data Read/Write Strobe Wait States bits⁽¹⁾
 - 1111 = Wait of 16 Трв •
 - • 0001 = Wait of 2 Трв
 - 0000 = Wait of 1 TPB (default)

bit 1-0 WAITE<1:0>: Data Hold After Read/Write Strobe Wait States bits⁽¹⁾

- 11 = Wait of 4 TPB 10 = Wait of 3 TPB 01 = Wait of 2 TPB
- 00 = Wait of 1 Трв (default)

For Read operations: 11 = Wait of 3 TPB 10 = Wait of 2 TPB 01 = Wait of 1 TPB 00 = Wait of 0 TPB (default)

- **Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.
 - 2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.
 - **3:** These pins are active when MODE16 = 1 (16-bit mode).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	DATAOUT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				DATAOU	Γ<7:0>			

REGISTER 20-4: PMDOUT: PARALLEL PORT OUTPUT DATA REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 DATAOUT<15:0>: Port Data Output bits

This register is used for Read operations in the Enhanced Parallel Slave mode and Write operations for Dual Buffer Master mode.

In Dual Buffer Master mode, the DUALBUF bit (PMPCON<17>) = 1, a write to the MSB triggers the transaction on the PMP port. When MODE16 = 1, MSB = DATAOUT<15:8>. When MODE16 = 0, MSB = DATAOUT<7:0>.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	_	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	_	—	_	—	—		_
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	DATAIN<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAIN<7:0>							

REGISTER 20-5: PMDIN: PARALLEL PORT INPUT DATA REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 DATAIN<15:0>: Port Data Input bits

This register is used for both Parallel Master Port mode and Enhanced Parallel Slave mode. In Parallel Master mode, a write to the MSB triggers the write transaction on the PMP port. Similarly, a read to the MSB triggers the read transaction on the PMP port. When MODE16 = 1, MSB = DATAIN<15:8>. When MODE16 = 0, MSB = DATAIN<7:0>.

Note: This register is not used in Dual Buffer Master mode (i.e., DUALBUF bit (PMPCON<17>) = 1).

Note: In Master mode, a read will return the last value written to the register. In Slave mode, a read will return indeterminate results.

'0' = Bit is cleared

x = Bit is unknown

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
31:24		HR10	<3:0>			HR01	<3:0>	
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
23:10	MIN10<3:0>				MIN01<3:0>			
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15:8		SEC10	<3:0>		SEC01<3:0>			
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	—	_	—	—	_	_	_	—
Legend:								
R = Readable bit W = Writable bit U		U = Unimple	emented bit, re	ead as '0'				

REGISTER 21-5: ALRMTIME: ALARM TIME VALUE REGISTER

bit 31-28 HR10<3:0>: Binary Coded Decimal value of hours bits, 10s place digits; contains a value from 0 to 2
bit 27-24 HR01<3:0>: Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9
bit 23-20 MIN10<3:0>: Binary Coded Decimal value of minutes bits, 10s place digits; contains a value from 0 to 5
bit 19-16 MIN01<3:0>: Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9
bit 15-12 SEC10<3:0>: Binary Coded Decimal value of seconds bits, 10s place digits; contains a value from 0 to 5
bit 11-8 SEC01<3:0>: Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9
bit 7-0 Unimplemented: Read as '0'

'1' = Bit is set

-n = Value at POR

22.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104) in the "PIC32 Family Reference Manual", which is available the Microchip from web site (www.microchip.com/PIC32).

The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- · Up to 1 Msps conversion speed
- Up to 48 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- · Automatic Channel Scan mode
- Selectable conversion trigger source
- · 16-word conversion result buffer
- · Selectable buffer fill modes
- · Eight conversion result format options
- · Operation during CPU Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 22-1. The 10-bit ADC has up to 28 analog input pins, designated AN0-AN27. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.



4: This selection is only used with CTMU capacitive and time measurement.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 22-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ADRC	—	—			SAMC<4:0>(1)		
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
7:0				ADCS<	7:0> ⁽²⁾			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ADRC: ADC Conversion Clock Source bit
 - 1 = Clock derived from FRC
 - 0 = Clock derived from Peripheral Bus Clock (PBCLK)
- bit 14-13 Unimplemented: Read as '0'
- - 00000001 =TPB 2 (ADCS<7:0> + 1) = 4 TPB = TAD 00000000 =TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD
- **Note 1:** This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.
 - 2: This bit is not used if the ADRC bit (AD1CON3<15>) = 1.

PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

REGISTER 23-13: C1FLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED) bit 20-16 FSEL14<4:0>: FIFO Selection bits 11111 = Reserved 10000 = Reserved 01111 = Message matching filter is stored in FIFO buffer 15 00000 = Message matching filter is stored in FIFO buffer 0 FLTEN13: Filter 13 Enable bit bit 15 1 = Filter is enabled 0 = Filter is disabled bit 14-13 MSEL13<1:0>: Filter 13 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected bit 12-8 FSEL13<4:0>: FIFO Selection bits 11111 = Reserved 10000 = Reserved 01111 = Message matching filter is stored in FIFO buffer 15 00000 = Message matching filter is stored in FIFO buffer 0 bit 7 FLTEN12: Filter 12 Enable bit 1 = Filter is enabled 0 = Filter is disabled bit 6-5 MSEL12<1:0>: Filter 12 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected FSEL12<4:0>: FIFO Selection bits bit 4-0 11111 = Reserved 10000 = Reserved 01111 = Message matching filter is stored in FIFO buffer 15 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
51.24				SID<	10:3>			
00.40	R/W-x	R/W-x	R/W-x	U-0	R/W-0	U-0	R/W-x	R/W-x
23.10		SID<2:0>		—	EXID	—	EID<1	17:16>
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
10.0				EID<	15:8>			
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
7.0				EID<	<7:0>			

REGISTER 23-14: C1RXFn: CAN ACCEPTANCE FILTER 'n' REGISTER ('n' = 0 THROUGH 15)

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 SID<10:0>: Standard Identifier bits

- 1 = Message address bit SIDx must be '1' to match filter
- 0 = Message address bit SIDx must be '0' to match filter
- bit 20 Unimplemented: Read as '0'
- bit 19 **EXID:** Extended Identifier Enable bits
 - 1 = Match only messages with extended identifier addresses
 - 0 = Match only messages with standard identifier addresses
- bit 18 Unimplemented: Read as '0'
- bit 17-0 EID<17:0>: Extended Identifier bits
 - 1 = Message address bit EIDx must be '1' to match filter
 - 0 = Message address bit EIDx must be '0' to match filter

Note: This register can only be modified when the filter is disabled (FLTENn = 0).

29.0 INSTRUCTION SET

The PIC32MX1XX/2XX/5XX 64/100-pin family instruction set complies with the MIPS32[®] Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- · Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note: Refer to *"MIPS32[®] Architecture for Programmers Volume II: The MIPS32[®] Instruction Set"* at www.imgtec.com for more information.

Note the following details of the code protection feature on Microchip devices:

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