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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx570f512lt-50i-pf">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx570f512lt-50i-pf</a>

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP			
INT0	35 <sup>(1)</sup> , 46 <sup>(2)</sup>	55 <sup>(1)</sup> , 72 <sup>(2)</sup>	I	ST	External Interrupt 0
INT1	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	I	ST	External Interrupt 4
RA0	—	17	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	I/O	ST	
RA2	—	58	I/O	ST	
RA3	—	59	I/O	ST	
RA4	—	60	I/O	ST	
RA5	—	61	I/O	ST	
RA6	—	91	I/O	ST	
RA7	—	92	I/O	ST	
RA9	—	28	I/O	ST	
RA10	—	29	I/O	ST	
RA14	—	66	I/O	ST	
RA15	—	67	I/O	ST	
RB0	16	25	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	I/O	ST	
RB2	14	23	I/O	ST	
RB3	13	22	I/O	ST	
RB4	12	21	I/O	ST	
RB5	11	20	I/O	ST	
RB6	17	26	I/O	ST	
RB7	18	27	I/O	ST	
RB8	21	32	I/O	ST	
RB9	22	33	I/O	ST	
RB10	23	34	I/O	ST	
RB11	24	35	I/O	ST	
RB12	27	41	I/O	ST	
RB13	28	42	I/O	ST	
RB14	29	43	I/O	ST	
RB15	30	44	I/O	ST	

**Legend:** CMOS = CMOS compatible input or output    Analog = Analog input    I = Input    O = Output  
ST = Schmitt Trigger input with CMOS levels    TTL = TTL input buffer    P = Power

- Note 1:** This pin is only available on devices without a USB module.  
**2:** This pin is only available on devices with a USB module.  
**3:** This pin is not available on 64-pin devices with a USB module.  
**4:** This pin is only available on 100-pin devices without a USB module.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP			
RF0	58	87	I/O	ST	PORTF is a bidirectional I/O port
RF1	59	88	I/O	ST	
RF2	34 <sup>(3)</sup>	52	I/O	ST	
RF3	33	51	I/O	ST	
RF4	31	49	I/O	ST	
RF5	32	50	I/O	ST	
RF6	35 <sup>(1)</sup>	55 <sup>(1)</sup>	I/O	ST	
RF7	—	54 <sup>(4)</sup>	I/O	ST	
RF8	—	53	I/O	ST	
RF12	—	40	I/O	ST	
RF13	—	39	I/O	ST	
RG0	—	90	I/O	ST	PORTG is a bidirectional I/O port
RG1	—	89	I/O	ST	
RG2	37 <sup>(1)</sup>	57 <sup>(1)</sup>	I/O	ST	
RG3	36 <sup>(1)</sup>	56 <sup>(1)</sup>	I/O	ST	
RG6	4	10	I/O	ST	
RG7	5	11	I/O	ST	
RG8	6	12	I/O	ST	
RG9	8	14	I/O	ST	
RG12	—	96	I/O	ST	
RG13	—	97	I/O	ST	
RG14	—	95	I/O	ST	
RG15	—	1	I/O	ST	
T1CK	48	74	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	I	ST	Timer5 External Clock Input
U1CTS	PPS	PPS	I	ST	UART1 Clear to Send
U1RTS	PPS	PPS	O	—	UART1 Ready to Send
U1RX	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	O	—	UART1 Transmit
U2CTS	PPS	PPS	I	ST	UART2 Clear to Send
U2RTS	PPS	PPS	O	—	UART2 Ready to Send
U2RX	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	O	—	UART2 Transmit

**Legend:** CMOS = CMOS compatible input or output    Analog = Analog input    I = Input    O = Output  
ST = Schmitt Trigger input with CMOS levels    TTL = TTL input buffer    P = Power

- Note 1:** This pin is only available on devices without a USB module.  
**2:** This pin is only available on devices with a USB module.  
**3:** This pin is not available on 64-pin devices with a USB module.  
**4:** This pin is only available on 100-pin devices without a USB module.

**TABLE 5-2: INTERRUPT REGISTER MAP (CONTINUED)**

Virtual Address (BF88_#)	Register Name <sup>(3)</sup>	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
10E0	IPC5	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>			—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>			—	—	—	T5IP<2:0>			T5IS<1:0>		0000
10F0	IPC6	31:16	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>			—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000
		15:0	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>			—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000
1100	IPC7	31:16	—	—	—	U1IP<2:0>			U1IS<1:0>			—	—	—	SPI1IP<2:0>			SPI1IS<1:0>		0000
		15:0	—	—	—	USBIP<2:0> <sup>(2)</sup>			USBIS<1:0> <sup>(2)</sup>			—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
1110	IPC8	31:16	—	—	—	SPI2IP<2:0>			SPI2IS<1:0>			—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
		15:0	—	—	—	CNIP<2:0>			CNIS<1:0>			—	—	—	I2C1IP<2:0>			I2C1IS<1:0>		0000
1120	IPC9	31:16	—	—	—	U4IP<2:0>			U4IS<1:0>			—	—	—	U3IP<2:0>			U3IS<1:0>		0000
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>			—	—	—	U2IP<2:0>			U2IS<1:0>		0000
1130	IPC10	31:16	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>			—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
		15:0	—	—	—	CTMUIP<2:0>			CTMUIS<1:0>			—	—	—	U5IP<2:0>			U5IS<1:0>		0000
1140	IPC11	31:16	—	—	—	CANIP<2:0> <sup>(5)</sup>			CANIS<1:0> <sup>(5)</sup>			—	—	—	CMP3IP<2:0>			CMP3IS<1:0>		0000
		15:0	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>			—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
1150	IPC12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	SPI4P<2:0> <sup>(1)</sup>			SPI4S<1:0> <sup>(1)</sup>			—	—	—	SPI3P<2:0>			SPI3S<1:0>		0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: This bit is only available on 100-pin devices.
  - 2: This bit is only implemented on devices with a USB module.
  - 3: With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.
  - 4: This register does not have associated CLR, SET, and INV registers.
  - 5: This bit is only implemented on devices with a CAN module.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## 6.0 FLASH PROGRAM MEMORY

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. “Flash Program Memory”** (DS60001121) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

PIC32MX1XX/2XX/5XX 64/100-pin devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. “Flash Program Memory”** (DS60001121) in the *“PIC32 Family Reference Manual”*.

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the *“PIC32 Flash Programming Specification”* (DS60001145), which can be downloaded from the Microchip web site.

**Note:** On PIC32MX1XX/2XX/5XX 64/100-pin devices, the Flash page size is 1 KB and the row size is 128 bytes (256 IW and 32 IW, respectively).

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

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NOTES:

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**REGISTER 9-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0> <sup>(1)</sup>							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0> <sup>(1)</sup>							
7:0	S-0 CFORCE	S-0 CABORT	R/W-0 PATEN	R/W-0 SIRQEN	R/W-0 AIRQEN	U-0 —	U-0 —	U-0 —

<b>Legend:</b>	S = Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>**: Channel Transfer Abort IRQ bits<sup>(1)</sup>

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag

•  
•  
•

00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag

00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>**: Channel Transfer Start IRQ bits<sup>(1)</sup>

11111111 = Interrupt 255 will initiate a DMA transfer

•  
•  
•

00000001 = Interrupt 1 will initiate a DMA transfer

00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE**: DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'

0 = This bit always reads '0'

bit 6 **CABORT**: DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'

0 = This bit always reads '0'

bit 5 **PATEN**: Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match

0 = Pattern match is disabled

bit 4 **SIRQEN**: Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs

0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN**: Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs

0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

**Note 1:** See Table 5-1: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**REGISTER 9-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSSIZ<15:0>**: Channel Source Size bits

1111111111111111 = 65,535 byte source size

.

.

.

0000000000000010 = 2 byte source size

0000000000000001 = 1 byte source size

0000000000000000 = 65,536 byte source size

**REGISTER 9-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDSIZ<15:0>**: Channel Destination Size bits

1111111111111111 = 65,535 byte destination size

.

.

.

0000000000000010 = 2 byte destination size

0000000000000001 = 1 byte destination size

0000000000000000 = 65,536 byte destination size



# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## REGISTER 10-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	UTEYE	—	—	USBSIDL	USBSIDL	—	—	UASUSPND

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye-Pattern Test Enable bit

1 = Eye-Pattern Test enabled

0 = Eye-Pattern Test disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 3 **LSDEV:** Low-Speed Device Enable bit

1 = USB module operates in Low-Speed Device mode only

0 = USB module operates in OTG, Host, or Full-Speed Device mode

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit

1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 10-5.

0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock

## 11.4 Control Registers

TABLE 11-3: PORTA REGISTER MAP 100-PIN DEVICES ONLY

Virtual Address (BF88_#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	ANSELA10	ANSELA9	—	—	—	—	—	—	—	—	—	0060
6010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISA15	TRISA14	—	—	—	TRISA10	TRISA9	—	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	C6FF
6020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RA15	RA14	—	—	—	RA10	RA9	—	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
6030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATA15	LATA14	—	—	—	LATA10	LATA9	—	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
6040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCA15	ODCA14	—	—	—	ODCA10	ODCA9	—	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
6050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUA15	CNPUA14	—	—	—	CNPUA10	CNPUA9	—	CNPUA7	CNPUA6	CNPUA5	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
6060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDA15	CNPDA14	—	—	—	CNPDA10	CNPDA9	—	CNPDA7	CNPDA6	CNPDA5	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
6070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEA15	CNIEA14	—	—	—	CNIEA10	CNIEA9	—	CNIEA7	CNIEA6	CNIEA5	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
6090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATA15	CN STATA14	—	—	—	CN STATA10	CN STATA9	—	CN STATA7	CN STATA6	CN STATA5	CN STATA4	CN STATA3	CN STATA2	CN STATA1	CN STATA0	0000

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET, and INV Registers”** for more information.

**TABLE 19-1: UART1 THROUGH UART5 REGISTER MAP (CONTINUED)**

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6440	U3BRG <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
6600	U4MODE <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>	STSEL	—	—	0000
6610	U4STA <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	—	—	FFFF
6620	U4TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6630	U4RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6640	U4BRG <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
6800	U5MODE <sup>(1,2)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>	STSEL	—	—	0000
6810	U5STA <sup>(1,2)</sup>	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	—	—	FFFF
6820	U5TXREG <sup>(1,2)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
6830	U5RXREG <sup>(1,2)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
6840	U5BRG <sup>(1,2)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.
- 2: This register is only available on 100-pin devices.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## REGISTER 21-5: ALRMTIME: ALARM TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **HR10<3:0>**: Binary Coded Decimal value of hours bits, 10s place digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>**: Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>**: Binary Coded Decimal value of minutes bits, 10s place digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>**: Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>**: Binary Coded Decimal value of seconds bits, 10s place digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>**: Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 **Unimplemented**: Read as '0'

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

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## REGISTER 23-3: C1INT: CAN INTERRUPT REGISTER (CONTINUED)

- bit 14 **WAKIF:** CAN Bus Activity Wake-up Interrupt Flag bit  
1 = A bus wake-up activity interrupt has occurred  
0 = A bus wake-up activity interrupt has not occurred
- bit 13 **CERRIF:** CAN Bus Error Interrupt Flag bit  
1 = A CAN bus error has occurred  
0 = A CAN bus error has not occurred
- bit 12 **SERRIF:** System Error Interrupt Flag bit<sup>(1)</sup>  
1 = A system error occurred (typically an illegal address was presented to the system bus)  
0 = A system error has not occurred
- bit 11 **RBOVIF:** Receive Buffer Overflow Interrupt Flag bit  
1 = A receive buffer overflow has occurred  
0 = A receive buffer overflow has not occurred
- bit 10-4 **Unimplemented:** Read as '0'
- bit 3 **MODIF:** CAN Mode Change Interrupt Flag bit  
1 = A CAN module mode change has occurred (OPMOD<2:0> has changed to reflect REQOP)  
0 = A CAN module mode change has not occurred
- bit 2 **CTMRIF:** CAN Timer Overflow Interrupt Flag bit  
1 = A CAN timer (CANTMR) overflow has occurred  
0 = A CAN timer (CANTMR) overflow has not occurred
- bit 1 **RBIF:** Receive Buffer Interrupt Flag bit  
1 = A receive buffer interrupt is pending  
0 = A receive buffer interrupt is not pending
- bit 0 **TBIF:** Transmit Buffer Interrupt Flag bit  
1 = A transmit buffer interrupt is pending  
0 = A transmit buffer interrupt is not pending

**Note 1:** This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (C1CON<15>).

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**REGISTER 24-1: CMxCON: COMPARATOR CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON <sup>(1)</sup>	COE	CPOL <sup>(2)</sup>	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit<sup>(1)</sup>

1 = Module is enabled. Setting this bit does not affect the other bits in this register

0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 **COE:** Comparator Output Enable bit

1 = Comparator output is driven on the output CxOUT pin

0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit<sup>(2)</sup>

1 = Output is inverted

0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit

1 = Output of the Comparator is a '1'

0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits

11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output

10 = Comparator interrupt is generated on a high-to-low transition of the comparator output

01 = Comparator interrupt is generated on a low-to-high transition of the comparator output

00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit

1 = Comparator non-inverting input is connected to the internal CVREF

0 = Comparator non-inverting input is connected to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator

11 = Comparator inverting input is connected to the IVREF

10 = Comparator inverting input is connected to the CxIND pin

01 = Comparator inverting input is connected to the CxINC pin

00 = Comparator inverting input is connected to the CxINB pin

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## 27.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 27-1 for more information.

**Note:** Disabling a peripheral module while its ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

**TABLE 27-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS**

Peripheral <sup>(1)</sup>	PMDx bit Name <sup>(1)</sup>	Register Name and Bit Location
ADC1	AD1MD	PMD1<0>
CTMU	CTMUMD	PMD1<8>
Comparator Voltage Reference	CVRMD	PMD1<12>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Comparator 3	CMP3MD	PMD2<2>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
UART3	U3MD	PMD5<2>
UART4	U4MD	PMD5<3>
UART5	U5MD	PMD5<4>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
SPI3	SPI3MD	PMD5<10>
SPI4	SPI4MD	PMD5<11>
I2C1	I2C1MD	PMD5<16>
I2C2	I2C2MD	PMD5<17>
USB <sup>(2)</sup>	USBMD	PMD5<24>
CAN	CAN1MD	PMD5<28>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output	REFOMD	PMD6<1>
PMP	PMPMD	PMD6<16>

**Note 1:** Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: “PIC32MX1XX/2XX/5XX 64/100-pin Controller Family Features”** for the list of available peripherals.

**2:** Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## REGISTER 28-6: DEVID: DEVICE AND REVISION ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	VER<3:0> <sup>(1)</sup>				DEVID<27:24> <sup>(1)</sup>			
23:16	R	R	R	R	R	R	R	R
	DEVID<23:16> <sup>(1)</sup>							
15:8	R	R	R	R	R	R	R	R
	DEVID<15:8> <sup>(1)</sup>							
7:0	R	R	R	R	R	R	R	R
	DEVID<7:0> <sup>(1)</sup>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **VER<3:0>**: Revision Identifier bits<sup>(1)</sup>

bit 27-0 **DEVID<27:0>**: Device ID<sup>(1)</sup>

**Note 1:** See the "PIC32 Flash Programming Specification" (DS60001145) for a list of Revision and Device ID values.



# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

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## 30.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page ([www.microchip.com](http://www.microchip.com)) for the complete list of demonstration, development and evaluation kits.

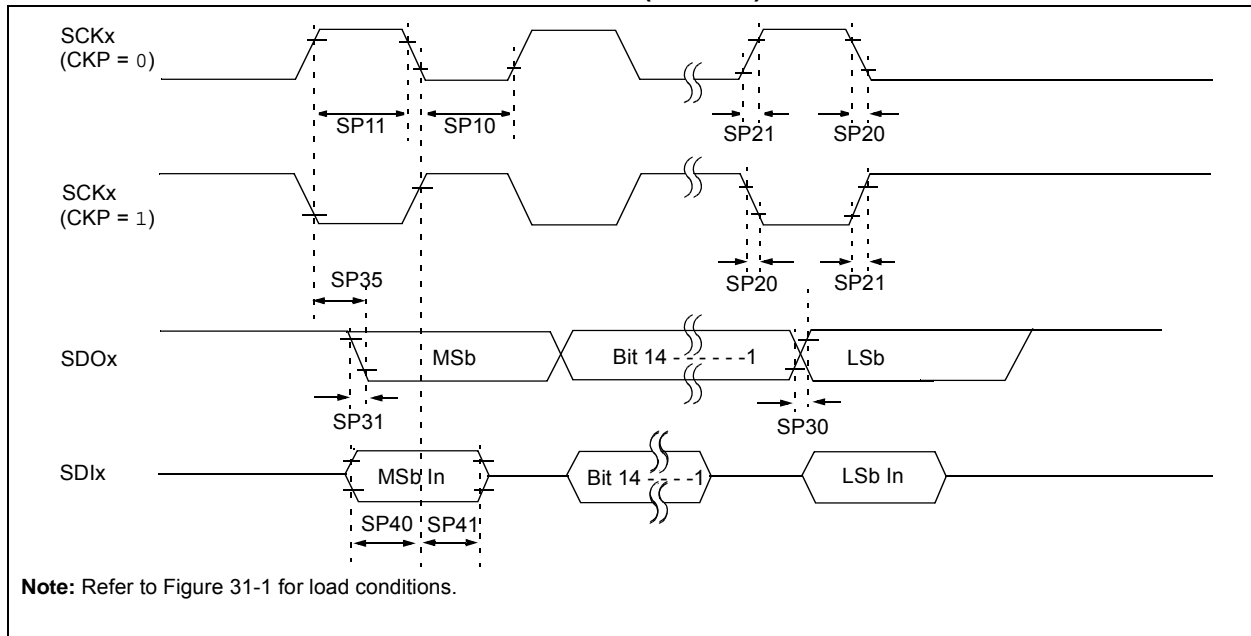
## 30.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**FIGURE 31-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS**



**TABLE 31-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS**

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typical <sup>(2)</sup>	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time (Note 3)	Tsck/2	—	—	ns	—
SP11	Tsch	SCKx Output High Time (Note 3)	Tsck/2	—	—	ns	—
SP20	TscF	SCKx Output Fall Time (Note 4)	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time (Note 4)	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time (Note 4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time (Note 4)	—	—	—	ns	See parameter DO31
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**Note 2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**Note 3:** The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.

**Note 4:** Assumes 50 pF load on all SPIx pins.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

**TABLE 31-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typical <sup>(2)</sup>	Max.	Units	Conditions
SP51	TssH2boZ	$\overline{\text{SS}}_x \uparrow$ to SDOx Output High-Impedance (Note 4)	5	—	25	ns	—
SP52	Tsch2ssH TscL2ssH	$\overline{\text{SS}}_x \uparrow$ after SCKx Edge	Tsck + 20	—	—	ns	—
SP60	TssL2boV	SDOx Data Output Valid after $\overline{\text{SS}}_x$ Edge	—	—	25	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns.

**4:** Assumes 50 pF load on all SPIx pins.

# PIC32MX1XX/2XX/5XX 64/100-PIN FAMILY

## 32.0 50 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX/5XX 64/100-pin Family electrical characteristics for devices operating at 50 MHz.

The specifications for 50 MHz are identical to those shown in **Section 31.0 “40 MHz Electrical Characteristics”**, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter “M”, which denotes 50 MHz operation. For example, parameter DC29a in **Section 31.0 “40 MHz Electrical Characteristics”**, is the up to 40 MHz operation equivalent for MDC29a.

Absolute maximum ratings for the PIC32MX1XX/2XX/5XX 64/100-pin Family 50 MHz devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

### Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias .....	-40°C to +85°C
Storage temperature .....	-65°C to +150°C
Voltage on VDD with respect to VSS .....	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS ( <b>Note 3</b> ) .....	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.3V ( <b>Note 3</b> ) .....	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V ( <b>Note 3</b> ) .....	-0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3 .....	-0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS .....	-0.3V to +5.5V
Maximum current out of VSS pin(s) .....	300 mA
Maximum current into VDD pin(s) ( <b>Note 2</b> ) .....	300 mA
Maximum output current sunk by any I/O pin .....	15 mA
Maximum output current sourced by any I/O pin .....	15 mA
Maximum current sunk by all ports .....	200 mA
Maximum current sourced by all ports ( <b>Note 2</b> ) .....	200 mA

**Note 1:** Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

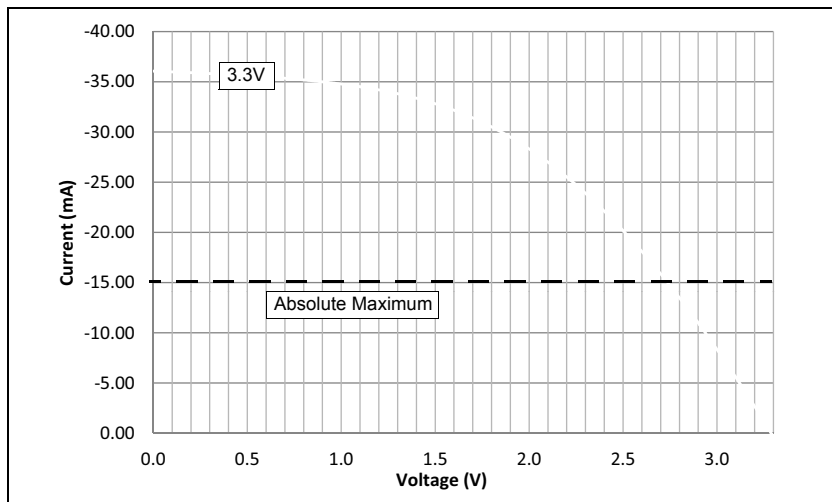
**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 32-2).

**3:** See the “**Device Pin Tables**” section for the 5V tolerant pins.

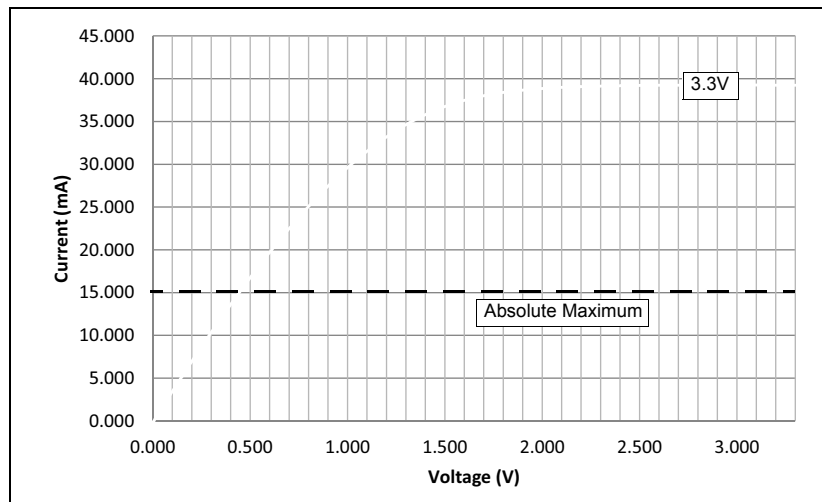
### 33.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

**Note:** The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

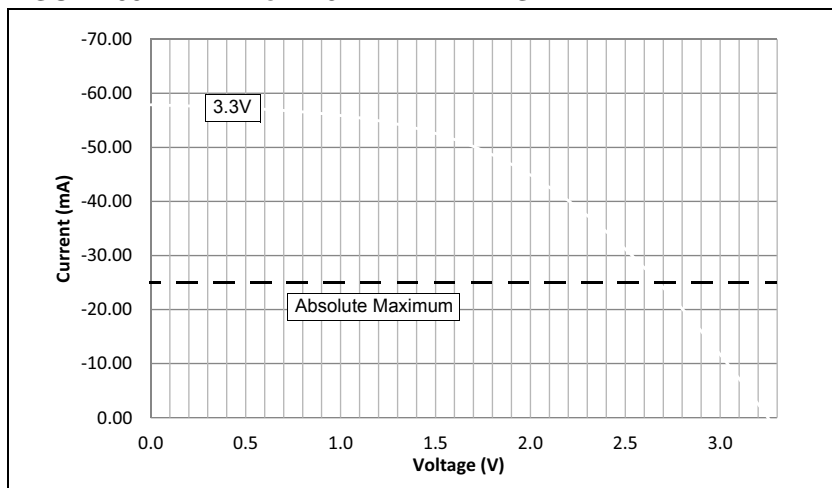
**FIGURE 33-1:  $V_{OH}$  – 4x DRIVER PINS**



**FIGURE 33-3:  $V_{OL}$  – 4x DRIVER PINS**



**FIGURE 33-2:  $V_{OH}$  – 8x DRIVER PINS**



**FIGURE 33-4:  $V_{OL}$  – 8x DRIVER PINS**

