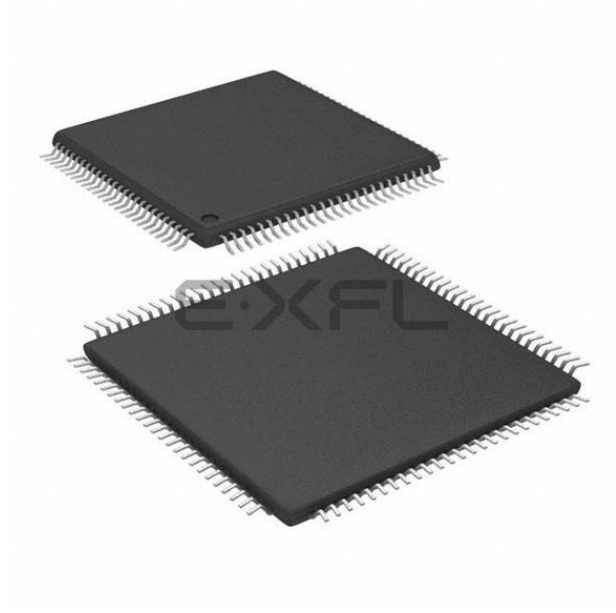
# Microchip Technology - PIC32MX570F512LT-50I/PT Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 81 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 48x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx570f512lt-50i-pt |

**TABLE 1: PIC32MX1XX/2XX/5XX 64/100-PIN CONTROLLER FAMILY FEATURES**

| Device | Pins | Packages(4) | Program Memory (KB)(1) | Data Memory (KB) | Remappable Peripherals | | | | | 10-bit 1 Msps ADC (Channels) | Analog Comparators | USB On-The-Go (OTG) | CAN | CTMU | $I^2C$ | PMP | RTCC | DMA Channels (Programmable/Dedicated) | I/O Pins | JTAG |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Remappable Pins | Timers/Capture/Compare(2) | UART | SPI/$I^2S$ | External Interrupts(3) | | | | | | | | | | | |
| PIC32MX120F064H | 64 | QFN, TQFP | 64+3 | 8 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 53 | Y |
| PIC32MX130F128H | 64 | QFN, TQFP | 128+3 | 16 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 53 | Y |
| PIC32MX130F128L | 100 | TQFP | 128+3 | 16 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 85 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX230F128H | 64 | QFN, TQFP | 128+3 | 16 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 49 | Y |
| PIC32MX230F128L | 100 | TQFP | 128+3 | 16 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX530F128H | 64 | QFN, TQFP | 128+3 | 16 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 49 | Y |
| PIC32MX530F128L | 100 | TQFP | 128+3 | 16 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX150F256H | 64 | QFN, TQFP | 256+3 | 32 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 53 | Y |
| PIC32MX150F256L | 100 | TQFP | 256+3 | 32 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 85 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX250F256H | 64 | QFN, TQFP | 256+3 | 32 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 49 | Y |
| PIC32MX250F256L | 100 | TQFP | 256+3 | 32 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX550F256H | 64 | QFN, TQFP | 256+3 | 32 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 49 | Y |
| PIC32MX550F256L | 100 | TQFP | 256+3 | 32 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX170F512H | 64 | QFN, TQFP | 512+3 | 64 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 53 | Y |
| PIC32MX170F512L | 100 | TQFP | 512+3 | 64 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | N | 0 | Y | 2 | Y | Y | 4/0 | 85 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX270F512H | 64 | QFN, TQFP | 512+3 | 64 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 49 | Y |
| PIC32MX270F512L | 100 | TQFP | 512+3 | 64 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 0 | Y | 2 | Y | Y | 4/2 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |
| PIC32MX570F512H | 64 | QFN, TQFP | 512+3 | 64 | 37 | 5/5/5 | 4 | 3 | 5 | 28 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 49 | Y |
| PIC32MX570F512L | 100 | TQFP | 512+3 | 64 | 54 | 5/5/5 | 5 | 4 | 5 | 48 | 3 | Y | 1 | Y | 2 | Y | Y | 4/4 | 81 | Y |
| | 100 | TFBGA | | | | | | | | | | | | | | | | | | |

**Note 1:** All devices feature 3 KB of Boot Flash memory.
**2:** Four out of five timers are remappable.
**3:** Four out of five external interrupts are remappable.
**4:** Please contact your local Microchip Sales Office for information regarding the availability of devices in the 100-pin TFBGA package.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | | | |
| AN36 | — | 47 | I | Analog | Analog input channels. |
| AN37 | — | 48 | I | Analog | |
| AN38 | — | 52 | I | Analog | |
| AN39 | — | 53 | I | Analog | |
| AN40 | — | 79 | I | Analog | |
| AN41 | — | 80 | I | Analog | |
| AN42 | — | 83 | I | Analog | |
| AN43 | — | 84 | I | Analog | |
| AN44 | — | 87 | I | Analog | |
| AN45 | — | 88 | I | Analog | |
| AN46 | — | 93 | I | Analog | |
| AN47 | — | 94 | I | Analog | |
| CLKI | 39 | 63 | I | ST/CMOS | External clock source input. Always associated with OSC1 pin function. |
| CLKO | 40 | 64 | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with the OSC2 pin function. |
| OSC1 | 39 | 63 | I | ST/CMOS | Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. |
| OSC2 | 40 | 64 | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. |
| SOSCI | 47 | 73 | I | ST/CMOS | 32.768 kHz low-power oscillator crystal input; CMOS otherwise. |
| SOSCO | 48 | 74 | O | — | 32.768 kHz low-power oscillator crystal output. |
| IC1 | PPS | PPS | I | ST | Capture Input 1-5 |
| IC2 | PPS | PPS | I | ST | |
| IC3 | PPS | PPS | I | ST | |
| IC4 | PPS | PPS | I | ST | |
| IC5 | PPS | PPS | I | ST | |
| OC1 | PPS | PPS | O | ST | Output Compare Output 1 |
| OC2 | PPS | PPS | O | ST | Output Compare Output 2 |
| OC3 | PPS | PPS | O | ST | Output Compare Output 3 |
| OC4 | PPS | PPS | O | ST | Output Compare Output 4 |
| OC5 | PPS | PPS | O | ST | Output Compare Output 5 |
| OCFA | PPS | PPS | I | ST | Output Compare Fault A Input |
| OCFB | 30 | 44 | I | ST | Output Compare Fault B Input |

**Legend:** CMOS = CMOS compatible input or output Analog = Analog input I = Input O = Output
ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer P = Power

**Note 1:** This pin is only available on devices without a USB module.

**2:** This pin is only available on devices with a USB module.

**3:** This pin is not available on 64-pin devices with a USB module.

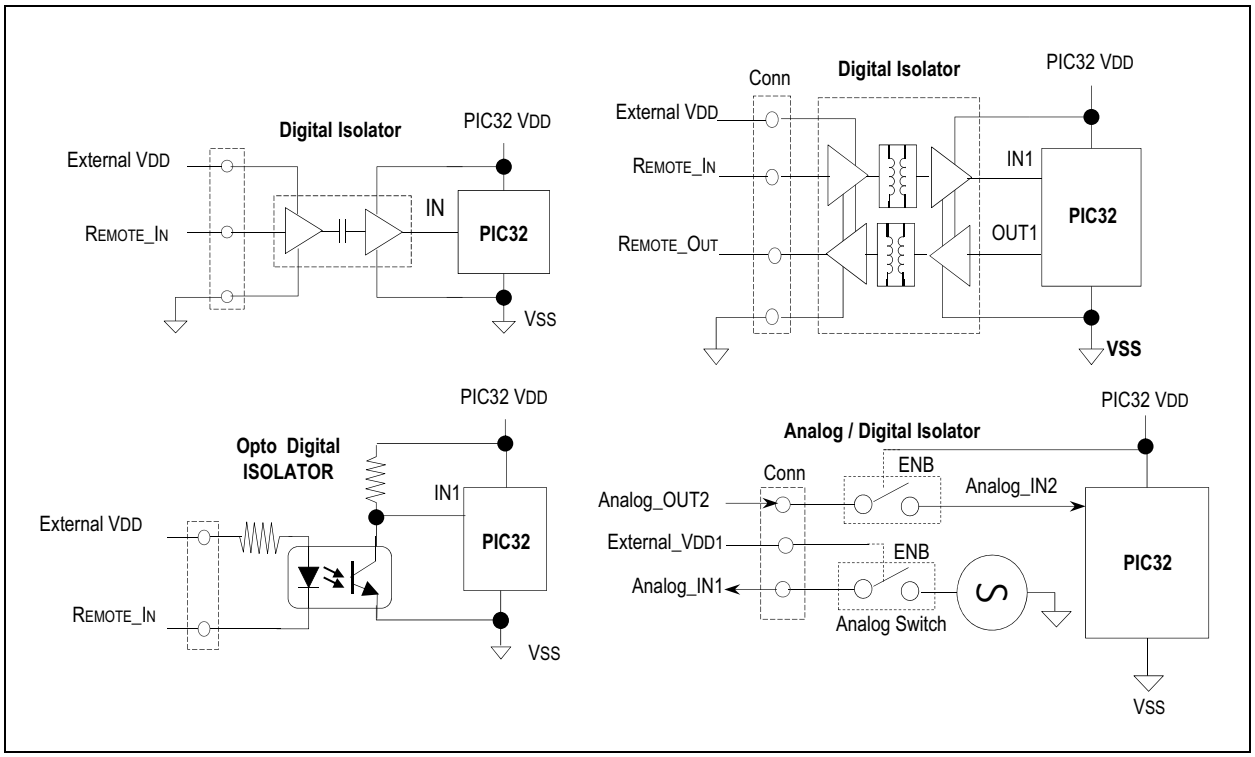
**4:** This pin is only available on 100-pin devices without a USB module.

Without proper signal isolation, on non-5V tolerant pins, the remote signal can power the PIC32 device through the high side ESD protection diodes. Besides violating the absolute maximum rating specification when VDD of the PIC32 device is restored and ramping up or ramping down, it can also negatively affect the internal Power-on Reset (POR) and Brown-out Reset (BOR) circuits, which can lead to improper initialization of internal PIC32 logic circuits. In these cases, it is recommended to implement digital or analog signal isolation as depicted in Figure 2-6, as appropriate. This is indicative of all industry microcontrollers and not just Microchip products.

**TABLE 2-1: EXAMPLES OF DIGITAL/ ANALOG ISOLATORS WITH OPTIONAL LEVEL TRANSLATION**

| Example Digital/Analog Signal Isolation Circuits | Inductive Coupling | Capacitive Coupling | Opto Coupling | Analog/Digital Switch |
|---|---|---|---|---|
| ADuM7241 / 40 ARZ (1 Mbps) | X | — | — | — |
| ADuM7241 / 40 CRZ (25 Mbps) | X | — | — | — |
| ISO721 | — | X | — | — |
| LTV-829S (2 Channel) | — | — | X | — |
| LTV-849S (4 Channel) | — | — | X | — |
| FSA266 / NC7WB66 | — | — | — | X |

**FIGURE 2-6: DIGITAL/ANALOG SIGNAL ISOLATION CIRCUITS**



**REGISTER 5-4: IFSx: INTERRUPT FLAG STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS31 | IFS30 | IFS29 | IFS28 | IFS27 | IFS26 | IFS25 | IFS24 |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS23 | IFS22 | IFS21 | IFS20 | IFS19 | IFS18 | IFS17 | IFS16 |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS15 | IFS14 | IFS13 | IFS12 | IFS11 | IFS10 | IFS9 | IFS8 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS7 | IFS6 | IFS5 | IFS4 | IFS3 | IFS2 | IFS1 | IFS0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **IFS31-IFS0:** Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = No interrupt request has occurred

**Note:** This register represents a generic definition of the IFSx register. Refer to Table 5-1 for the exact bit definitions.

**REGISTER 5-5: IECx: INTERRUPT ENABLE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC31 | IEC30 | IEC29 | IEC28 | IEC27 | IEC26 | IEC25 | IEC24 |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC23 | IEC22 | IEC21 | IEC20 | IEC19 | IEC18 | IEC17 | IEC16 |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC15 | IEC14 | IEC13 | IEC12 | IEC11 | IEC10 | IEC9 | IEC8 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC7 | IEC6 | IEC5 | IEC4 | IEC3 | IEC2 | IEC1 | IEC0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **IEC31-IEC0:** Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

**Note:** This register represents a generic definition of the IECx register. Refer to Table 5-1 for the exact bit definitions.

## 7.1 Control Registers

**TABLE 7-1: RESET SFR SUMMARY**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F600 | RCON | 31:16 | — | — | HVDR | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CMR | VREGS | EXTR | SWR | — | WDTO | SLEEP | IDLE | BOR | POR | xxxx(1) |
| F610 | RSWRST | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SWRST | 0000 |

**Legend:** — = unimplemented, read as '0'. Address offset values are shown in hexadecimal.

**Note 1:** The Reset value is dependent on the DEVCFGx Configuration bits and the type of reset.

**REGISTER 7-2: RSWRST: SOFTWARE RESET REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | W-0, HC |
| | — | — | — | — | — | — | — | SWRST(1) |

| Legend: | HC = Cleared by hardware | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit(1)
- 1 = Enable software Reset event
- 0 = No effect

**Note 1:** The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

**REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit
- 1 = Interrupt is enabled
- 0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit
- 1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)
- 0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit
- 1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)
- 0 = No interrupt is pending

bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
- 1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
- 0 = No interrupt is pending

## 11.0 I/O PORTS

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX/5XX 64/100-pin family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

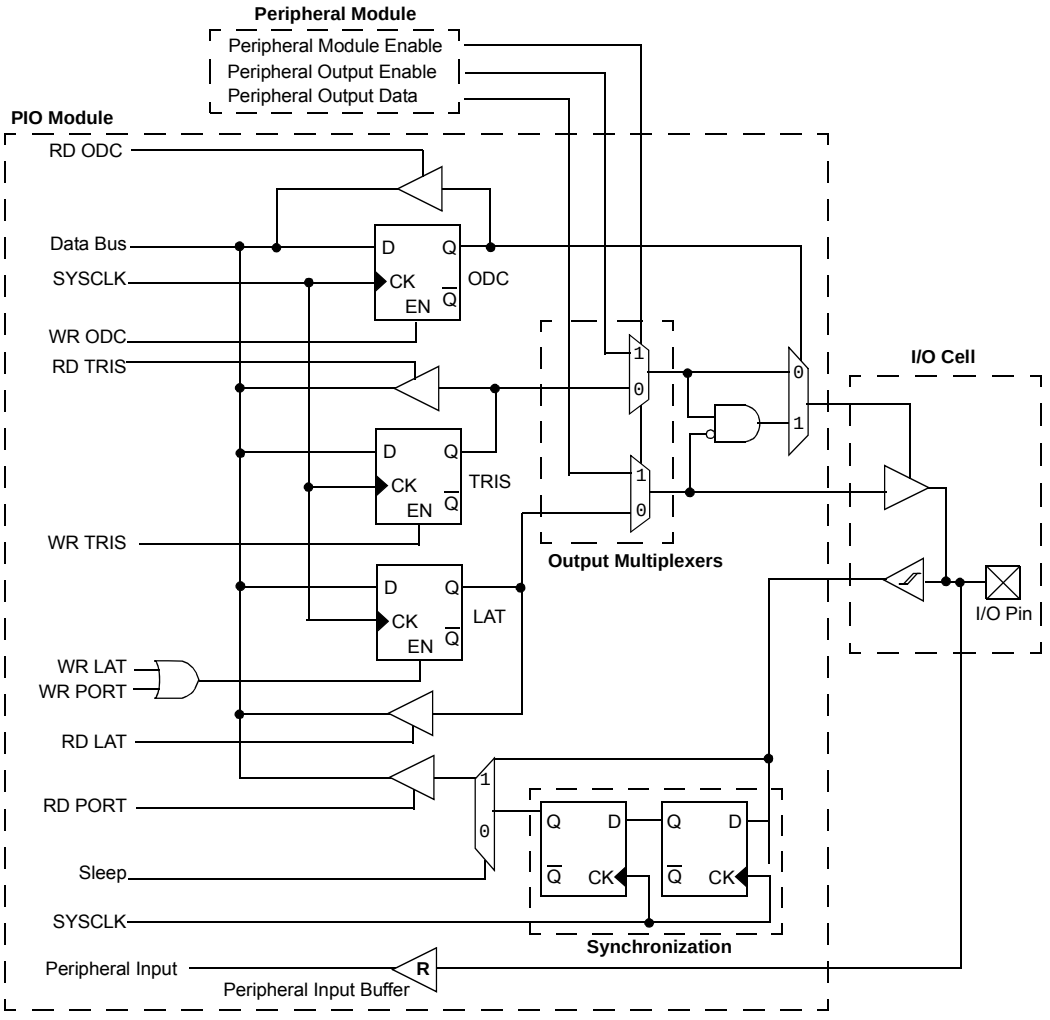
General purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate functions. These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

The following are the key features of this module:

- Individual output pin open-drain enable or disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

Figure 11-1 illustrates a block diagram of a typical multiplexed I/O port.

**FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE**




**Legend:** R = Peripheral input buffer types may vary. Refer to Table 1-1 for peripheral details.

**Note:** This block diagram is a general representation of a shared port/peripheral structure for illustration purposes only. The actual structure for any specific port/peripheral combination may be different than shown here.

**TABLE 11-1: INPUT PIN SELECTION (CONTINUED)**

| Peripheral Pin | [*pin name*]R SFR | [*pin name*]R bits | [*pin name*]R Value to RPn Pin Selection |
|---|---|---|---|
| INT1 | INT1R | INT1R<3:0> | 0000 = RPD1<br>0001 = RPG9<br>0010 = RPB14<br>0011 = RPD0<br>0100 = RPD8<br>0101 = RPB6<br>0110 = RPD5<br>0111 = RPB2<br>1000 = RPF3(4)<br>1001 = RPF13(3)<br>1010 = Reserved<br>1011 = RPF2(1)<br>1100 = RPC2(3)<br>1101 = RPE8(3)<br>1110 = Reserved<br>1111 = Reserved |
| T3CK | T3CKR | T3CKR<3:0> | |
| IC1 | IC1R | IC1R<3:0> | |
| $\overline{\text{U3CTS}}$ | U3CTSR | U3CTSR<3:0> | |
| U4RX | U4RXR | U4RXR<3:0> | |
| U5RX | U5RXR | U5RXR<3:0> | |
| $\overline{\text{SS2}}$ | SS2R | SS2R<3:0> | |
| OCFA | OCFAR | OCFAR<3:0> | |

**Note 1:** This selection is not available on 64-pin USB devices.

**2:** This selection is only available on 100-pin General Purpose devices.

**3:** This selection is not available on 64-pin devices.

**4:** This selection is not available when USBID functionality is used on USB devices.

**5:** This selection is not available on devices without a CAN module.

**6:** This selection is not available on USB devices.

**7:** This selection is not available when VBUSON functionality is used on USB devices.

**TABLE 11-2: OUTPUT PIN SELECTION**

| RPn Port Pin | RPnR SFR | RPnR bits | RPnR Value to Peripheral Selection |
|---|---|---|---|
| RPD2 | RPD2R | RPD2R<3:0> | 0000 = No Connect<br>0001 = U3TX<br>0010 = U4RTS<br>0011 = Reserved<br>0100 = Reserved<br>0101 = Reserved<br>0110 = SDO2<br>0111 = Reserved<br>1000 = Reserved<br>1001 = Reserved<br>1010 = Reserved<br>1011 = OC3<br>1100 = C1TX(5)<br>1101 = C2OUT<br>1110 = SDO3<br>1111 = SDO4(3) |
| RPG8 | RPG8R | RPG8R<3:0> | |
| RPF4 | RPF4R | RPF4R<3:0> | |
| RPD10 | RPD10R | RPD10R<3:0> | |
| RPF1 | RPF1R | RPF1R<3:0> | |
| RPB9 | RPB9R | RPB9R<3:0> | |
| RPB10 | RPB10R | RPB10R<3:0> | |
| RPC14 | RPC14R | RPC14R<3:0> | |
| RPB5(7) | RPB5R | RPB5R<3:0> | |
| RPC1(3) | RPC1R | RPC1R<3:0> | |
| RPD14(3) | RPD14R | RPD14R<3:0> | |
| RPG1(3) | RPG1R | RPG1R<3:0> | |
| RPA14(3) | RPA14R | RPA14R<3:0> | |
| RPD3 | RPD3R | RPD3R<3:0> | 0000 = No Connect<br>0001 = U2TX<br>0010 = Reserved<br>0011 = U1TX<br>0100 = U5RTS(3)<br>0101 = Reserved<br>0110 = SDO2<br>0111 = Reserved<br>1000 = SDO1<br>1001 = Reserved<br>1010 = Reserved<br>1011 = OC4<br>1100 = Reserved<br>1101 = C3OUT<br>1110 = SDO3<br>1111 = SDO4(3) |
| RPG7 | RPG7R | RPG7R<3:0> | |
| RPF5 | RPF5R | RPF5R<3:0> | |
| RPD11 | RPD11R | RPD11R<3:0> | |
| RPF0 | RPF0R | RPF0R<3:0> | |
| RPB1 | RPB1R | RPB1R<3:0> | |
| RPE5 | RPE5R | RPE5R<3:0> | |
| RPC13 | RPC13R | RPC13R<3:0> | |
| RPB3 | RPB3R | RPB3R<3:0> | |
| RPF3(4) | RPF3R | RPF3R<3:0> | |
| RPC4(3) | RPC4R | RPC4R<3:0> | |
| RPD15(3) | RPD15R | RPD15R<3:0> | |
| RPG0(3) | RPG0R | RPG0R<3:0> | |
| RPA15(3) | RPA15R | RPA15R<3:0> | |

**Note 1:** This selection is not available on 64-pin USB devices.

**2:** This selection is only available on 100-pin General Purpose devices.

**3:** This selection is not available on 64-pin devices.

**4:** This selection is not available when USBID functionality is used on USB devices.

**5:** This selection is not available on devices without a CAN module.

**6:** This selection is not available on USB devices.

**7:** This selection is not available when VBUSON functionality is used on USB devices.

**TABLE 11-5: PORTC REGISTER MAP FOR 100-PIN DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6200 | ANSELC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | ANSELC3 | ANSELC2 | ANSELC1 | — | 000E |
| 6210 | TRISC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISC15 | TRISC14 | TRISC13 | TRISC12 | — | — | — | — | — | — | — | TRISC4 | TRISC3 | TRISC2 | TRISC1 | — | FFFF |
| 6220 | PORTC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RC15 | RC14 | RC13 | RC12 | — | — | — | — | — | — | — | RC4 | RC3 | RC2 | RC1 | — | xxxx |
| 6230 | LATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATC15 | LATC14 | LATC13 | LATC12 | — | — | — | — | — | — | — | LATC4 | LATC3 | LATC2 | LATC1 | — | xxxx |
| 6240 | ODCC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCC15 | ODCC14 | ODCC13 | ODCC12 | — | — | — | — | — | — | — | ODCC4 | ODCC3 | ODCC2 | ODCC1 | — | 0000 |
| 6250 | CNPUC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUC15 | CNPUC14 | CNPUC13 | CNPUC12 | — | — | — | — | — | — | — | CNPUC4 | CNPUC3 | CNPUC2 | CNPUC1 | — | 0000 |
| 6260 | CNPDC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDC15 | CNPDC14 | CNPDC13 | CNPDC12 | — | — | — | — | — | — | — | CNPDC4 | CNPDC3 | CNPDC2 | CNPDC1 | — | 0000 |
| 6270 | CNCONC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6280 | CNENC | 31:16 | — | — | | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIEC15 | CNIEC14 | CNIEC13 | CNIEC12 | — | — | — | — | — | — | — | CNIEC4 | CNIEC3 | CNIEC2 | CNIEC1 | — | 0000 |
| 6290 | CNSTATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNSTATC15 | CNSTATC14 | CNSTATC13 | CNSTATC12 | — | — | — | — | — | — | — | CNSTATC4 | CNSTATC3 | CNSTATC2 | CNSTATC1 | — | 0000 |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET, and INV Registers"** for more information.

**REGISTER 18-2: I2CxSTAT: I$^2$C STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0, HSC | R-0, HSC | U-0 | U-0 | U-0 | R/C-0, HS | R-0, HSC | R-0, HSC |
| | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 |
| 7:0 | R/C-0, HS | R/C-0, HS | R-0, HSC | R/C-0, HSC | R/C-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |

| Legend: | HS = Set in hardware | HSC = Hardware set/cleared | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | C = Clearable bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I$^2$C master, applicable to master transmit operation)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I$^2$C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision. This condition can only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I$^2$C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as I$^2$C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of slave byte.

**REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ALRMEN(1,2) | CHIME(2) | PIV(2) | ALRMSYNC(3) | AMASK<3:0>(3) | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ARPT<7:0>(3) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit(1,2)
- 1 = Alarm is enabled
- 0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit(2)
- 1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit(2)

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.
When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit(3)
- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits(3)
- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved; do not use
- 1011 = Reserved; do not use
- 11xx = Reserved; do not use

**Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

**2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

**3:** This assumes a CPU read will execute in less than 32 PBCLKs.

**Note:** This register is reset only on a Power-on Reset (POR).

**REGISTER 23-12: C1FLTCON2: CAN FILTER CONTROL REGISTER 2 (CONTINUED)**

bit 20-16 **FSEL10<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 15 **FLTEN9:** Filter 9 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL9<1:0>:** Filter 9 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL9<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN8:** Filter 8 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL8<1:0>:** Filter 8 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL8<4:0>:** FIFO Selection bits
11111 = Reserved
.
.
.
10000 = Reserved
01111 = Message matching filter is stored in FIFO buffer 15
.
.
.
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 24-2: CMSTAT: COMPARATOR STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | SIDL | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | — | C3OUT | C2OUT | C1OUT |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in IDLE Control bit
- 1 = All Comparator modules are disabled in IDLE mode
- 0 = All Comparator modules continue to operate in the IDLE mode

bit 12-3 **Unimplemented:** Read as '0'

bit 2 **C3OUT:** Comparator Output bit
- 1 = Output of Comparator 3 is a '1'
- 0 = Output of Comparator 3 is a '0'

bit 1 **C2OUT:** Comparator Output bit
- 1 = Output of Comparator 2 is a '1'
- 0 = Output of Comparator 2 is a '0'

bit 0 **C1OUT:** Comparator Output bit
- 1 = Output of Comparator 1 is a '1'
- 0 = Output of Comparator 1 is a '0'

## 27.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 27-1 for more information.

| **Note:** | Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits. |
|---|---|

**TABLE 27-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS**

| Peripheral(1) | PMDx bit Name(1) | Register Name and Bit Location |
|---|---|---|
| ADC1 | AD1MD | PMD1<0> |
| CTMU | CTMUMD | PMD1<8> |
| Comparator Voltage Reference | CVRMD | PMD1<12> |
| Comparator 1 | CMP1MD | PMD2<0> |
| Comparator 2 | CMP2MD | PMD2<1> |
| Comparator 3 | CMP3MD | PMD2<2> |
| Input Capture 1 | IC1MD | PMD3<0> |
| Input Capture 2 | IC2MD | PMD3<1> |
| Input Capture 3 | IC3MD | PMD3<2> |
| Input Capture 4 | IC4MD | PMD3<3> |
| Input Capture 5 | IC5MD | PMD3<4> |
| Output Compare 1 | OC1MD | PMD3<16> |
| Output Compare 2 | OC2MD | PMD3<17> |
| Output Compare 3 | OC3MD | PMD3<18> |
| Output Compare 4 | OC4MD | PMD3<19> |
| Output Compare 5 | OC5MD | PMD3<20> |
| Timer1 | T1MD | PMD4<0> |
| Timer2 | T2MD | PMD4<1> |
| Timer3 | T3MD | PMD4<2> |
| Timer4 | T4MD | PMD4<3> |
| Timer5 | T5MD | PMD4<4> |
| UART1 | U1MD | PMD5<0> |
| UART2 | U2MD | PMD5<1> |
| UART3 | U3MD | PMD5<2> |
| UART4 | U4MD | PMD5<3> |
| UART5 | U5MD | PMD5<4> |
| SPI1 | SPI1MD | PMD5<8> |
| SPI2 | SPI2MD | PMD5<9> |
| SPI3 | SPI3MD | PMD5<10> |
| SPI4 | SPI4MD | PMD5<11> |
| I2C1 | I2C1MD | PMD5<16> |
| I2C2 | I2C2MD | PMD5<17> |
| USB(2) | USBMD | PMD5<24> |
| CAN | CAN1MD | PMD5<28> |
| RTCC | RTCCMD | PMD6<0> |
| Reference Clock Output | REFOMD | PMD6<1> |
| PMP | PMPMD | PMD6<16> |

**Note 1:** Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: "PIC32MX1XX/2XX/5XX 64/100-pin Controller Family Features"** for the list of available peripherals.

**2:** Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

**NOTES:**

**REGISTER 28-2: DEVCFG1: DEVICE CONFIGURATION WORD 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | R/P | R/P |
| | — | — | — | — | — | — | FWDTWINSZ<1:0> | |
| 23:16 | R/P | R/P | r-1 | R/P | R/P | R/P | R/P | R/P |
| | FWDTEN | WINDIS | — | WDTPS<4:0> | | | | |
| 15:8 | R/P | R/P | R/P | R/P | r-1 | R/P | R/P | R/P |
| | FCKSM<1:0> | | FPBDIV<1:0> | | — | OSCIOFNC | POSCMOD<1:0> | |
| 7:0 | R/P | r-1 | R/P | r-1 | r-1 | R/P | R/P | R/P |
| | IESO | — | FSOSCEN | — | — | FNOSC<2:0> | | |

| **Legend:** | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-26 **Reserved:** Write '1'

bit 25-24 **FWDTWINSZ:** Watchdog Timer Window Size bits
11 = Window size is 25%
10 = Window size is 37.5%
01 = Window size is 50%
00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled and cannot be disabled by software
0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit
1 = Watchdog Timer is in non-Window mode
0 = Watchdog Timer is in Window mode

bit 21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits
10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

**Note 1:** Do not disable the POSC (POSCMOD = 11) when using this oscillator source.

**TABLE 31-18: PLL CLOCK TIMING SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range | 3.92 | — | 5 | MHz | ECPLL, HSPLL, XTPLL, FRCPLL modes |
| OS51 | FSYS | On-Chip VCO System Frequency | 60 | — | 120 | MHz | — |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | — | — | 2 | ms | — |
| OS53 | DCLK | CLKO Stability(2) (Period Jitter or Cumulative) | -0.25 | — | +0.25 | % | Measured over 100 ms period |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 40 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{40}{20}}} = \frac{D_{CLK}}{1.41}$$

**TABLE 31-19: INTERNAL FRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **Internal FRC Accuracy @ 8.00 MHz(1)** | | | | | | |
| F20a | FRC | -0.9 | — | +0.9 | % | -40°C ≤ TA ≤ +85°C |
| F20b | FRC | -2 | — | +2 | % | -40°C ≤ TA ≤ +105°C |

**Note 1:** Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

**TABLE 31-20: INTERNAL LPRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **LPRC @ 31.25 kHz(1)** | | | | | | |
| F21 | LPRC | -15 | — | +15 | % | — |

**Note 1:** Change of LPRC frequency as VDD changes.

# Worldwide Sales and Service

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