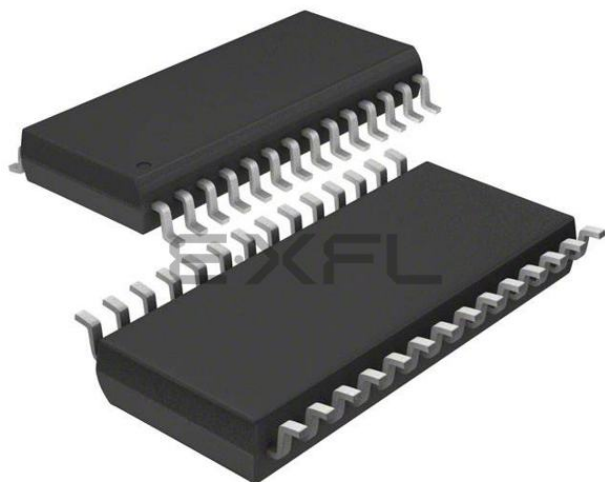




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 12x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c29466-24pvxi

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article “How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292”. Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
 - [Getting Started with PSoC® 1 – AN75320](#)
 - [PSoC® 1 - Getting Started with GPIO – AN2094](#)
 - [PSoC® 1 Analog Structure and Configuration – AN74170](#)
 - [PSoC® 1 Switched Capacitor Analog Blocks – AN2041](#)
 - [Selecting Analog Ground and Reference – AN2219](#)

Note: For CY8C29X66 devices related Application note please click [here](#).

- Development Kits:
 - [CY3210-PSoCEval1](#) supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
 - [CY3214-PSoCEvalUSB](#) features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C29X66 devices related Development Kits please click [here](#).

The [MiniProg1](#) and [MiniProg3](#) devices provide interfaces for flash programming and debug.

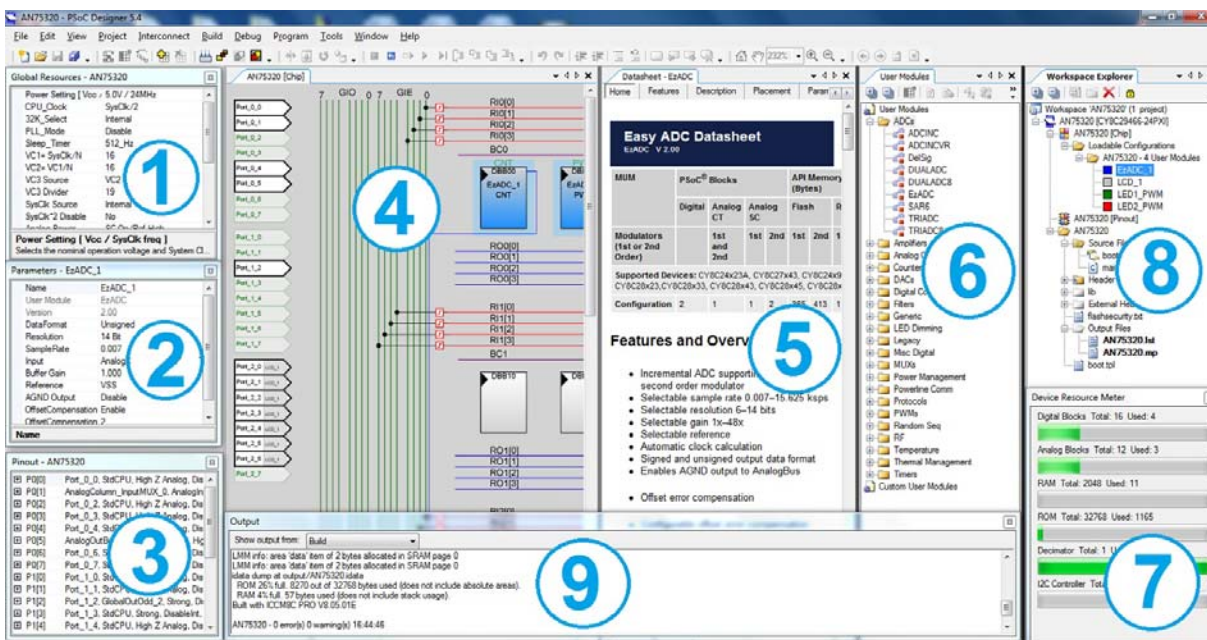
PSoC Designer

[PSoC Designer](#) is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. [Figure 1](#) shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources** – all device hardware settings.
2. **Parameters** – the parameters of the currently selected User Modules.
3. **Pinout** – information related to device pins.
4. **Chip-Level Editor** – a diagram of the resources available on the selected chip.
5. **Datasheet** – the datasheet for the currently selected UM
6. **User Modules** – all available User Modules for the selected device.
7. **Device Resource Meter** – device resource usage for the current project configuration.
8. **Workspace** – a tree level diagram of files associated with the project.
9. **Output** – output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout



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Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

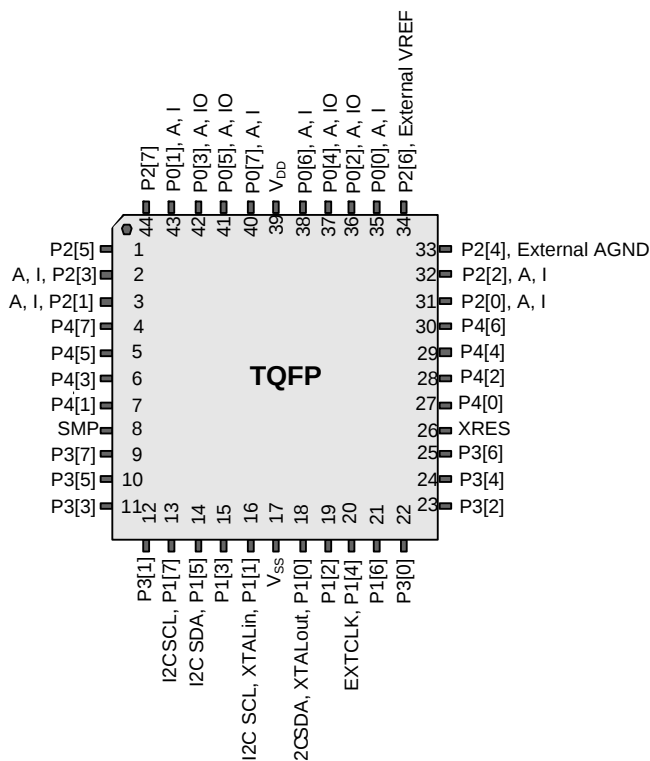
A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Table 3. 44-Pin Part Pinout (TQFP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O		P2[5]	
2	I/O	I	P2[3]	Direct switched capacitor block input
3	I/O	I	P2[1]	Direct switched capacitor block input
4	I/O		P4[7]	
5	I/O		P4[5]	
6	I/O		P4[3]	
7	I/O		P4[1]	
8	Power		SMP	Switch mode pump (SMP) connection to external components required
9	I/O		P3[7]	
10	I/O		P3[5]	
11	I/O		P3[3]	
12	I/O		P3[1]	
13	I/O		P1[7]	I ² C SCL
14	I/O		P1[5]	I ² C SDA
15	I/O		P1[3]	
16	I/O		P1[1]	Crystal (XTALin), I ² C SCL, ISSP-SCLK ^[6]
17	Power		V _{SS}	Ground connection
18	I/O		P1[0]	Crystal (XTALout), I ² C SDA, ISSP-SDATA ^[6]
19	I/O		P1[2]	
20	I/O		P1[4]	Optional EXTCLK
21	I/O		P1[6]	
22	I/O		P3[0]	
23	I/O		P3[2]	
24	I/O		P3[4]	
25	I/O		P3[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O		P4[0]	
28	I/O		P4[2]	
29	I/O		P4[4]	
30	I/O		P4[6]	
31	I/O	I	P2[0]	Direct switched capacitor block input
32	I/O	I	P2[2]	Direct switched capacitor block input
33	I/O		P2[4]	External analog ground (AGND)
34	I/O		P2[6]	External voltage reference (VREF)
35	I/O	I	P0[0]	Analog column mux input
36	I/O	I/O	P0[2]	Analog column mux input and column output
37	I/O	I/O	P0[4]	Analog column mux input and column output
38	I/O	I	P0[6]	Analog column mux input
39	Power		V _{DD}	Supply voltage
40	I/O	I	P0[7]	Analog column mux input
41	I/O	I/O	P0[5]	Analog column mux input and column output
42	I/O	I/O	P0[3]	Analog column mux input and column output
43	I/O	I	P0[1]	Analog column mux input
44	I/O		P2[7]	

Figure 5. CY8C29566 44-Pin PSoC Device



6. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

48-Pin Part Pinout

Table 4. 48-Pin Part Pinout (SSOP)

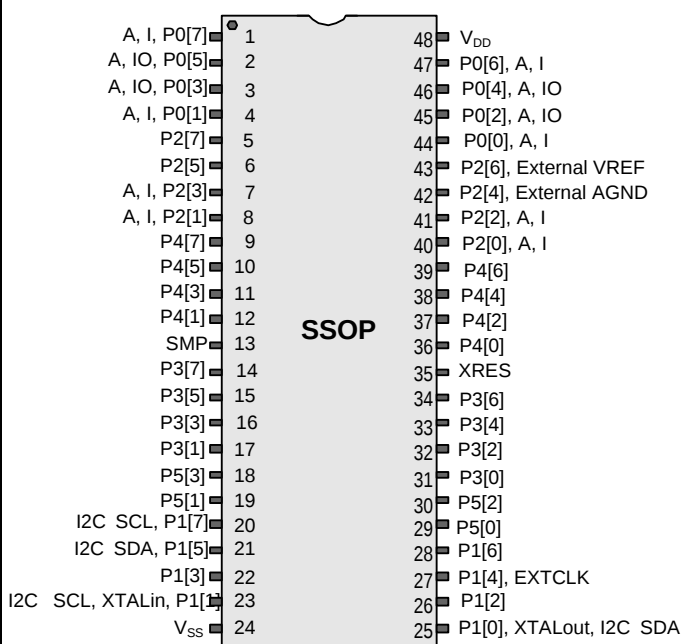
Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	I/O		P4[7]	
10	I/O		P4[5]	
11	I/O		P4[3]	
12	I/O		P4[1]	
13	Power		SMP	Switch mode pump (SMP) connection to external components required
14	I/O		P3[7]	
15	I/O		P3[5]	
16	I/O		P3[3]	
17	I/O		P3[1]	
18	I/O		P5[3]	
19	I/O		P5[1]	
20	I/O		P1[7]	I ² C SCL
21	I/O		P1[5]	I ² C SDA
22	I/O		P1[3]	
23	I/O		P1[1]	Crystal (XTALin), I ² C SCL, ISSP-SCLK ^[7]
24	Power		V _{SS}	Ground connection
25	I/O		P1[0]	Crystal (XTALout), I ² C SDA, ISSP-SDATA ^[7]
26	I/O		P1[2]	
27	I/O		P1[4]	Optional EXTCLK
28	I/O		P1[6]	
29	I/O		P5[0]	
30	I/O		P5[2]	
31	I/O		P3[0]	
32	I/O		P3[2]	
33	I/O		P3[4]	
34	I/O		P3[6]	
35	Input		XRES	Active high external reset with internal pull-down
36	I/O		P4[0]	
37	I/O		P4[2]	
38	I/O		P4[4]	
39	I/O		P4[6]	
40	I/O	I	P2[0]	Direct switched capacitor block input
41	I/O	I	P2[2]	Direct switched capacitor block input
42	I/O		P2[4]	External Analog Ground (AGND)
43	I/O		P2[6]	External Voltage Reference (VREF)
44	I/O	I	P0[0]	Analog column mux input
45	I/O	I/O	P0[2]	Analog column mux input and column output
46	I/O	I/O	P0[4]	Analog column mux input and column output
47	I/O	I	P0[6]	Analog column mux input
48	Power		V _{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Note

7. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

Figure 6. CY8C29666 48-Pin PSoC Device



100-Pin Part Pinout (On-Chip Debug)

The 100-pin TQFP part is for the CY8C29000 On-Chip Debug (OCD) PSoC device.

Note OCD parts are only used for in-circuit debugging. OCD parts are NOT available for production.

Table 7. 100-Pin OCD Part Pinout (TQFP)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No internal connection	51			NC	No internal connection
2			NC	No internal connection	52	I/O		P5[0]	
3	I/O	I	P0[1]	Analog column mux input	53	I/O		P5[2]	
4	I/O		P2[7]		54	I/O		P5[4]	
5	I/O		P2[5]		55	I/O		P5[6]	
6	I/O	I	P2[3]	Direct switched capacitor block input	56	I/O		P3[0]	
7	I/O	I	P2[1]	Direct switched capacitor block input	57	I/O		P3[2]	
8	I/O		P4[7]		58	I/O		P3[4]	
9	I/O		P4[5]		59	I/O		P3[6]	
10	I/O		P4[3]		60			HCLK	OCD high speed clock output
11	I/O		P4[1]		61			CCLK	OCD CPU clock output
12			OCDE	OCD even data I/O	62	Input		XRES	Active high pin reset with internal pull-down
13			OCDO	OCD odd data output	63	I/O		P4[0]	
14	Power		SMP	Switch Mode Pump (SMP) connection to required external components	64	I/O		P4[2]	
15	Power		V _{SS}	Ground connection ^[12]	65	Power		V _{SS}	Ground connection ^[12]
16	I/O		P3[7]		66	I/O		P4[4]	
17	I/O		P3[5]		67	I/O		P4[6]	
18	I/O		P3[3]		68	I/O	I	P2[0]	Direct switched capacitor block input
19	I/O		P3[1]		69	I/O	I	P2[2]	Direct switched capacitor block input
20	I/O		P5[7]		70	I/O		P2[4]	External Analog Ground (AGND) input
21	I/O		P5[5]		71			NC	No internal connection
22	I/O		P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF) input
23	I/O		P5[1]		73			NC	No internal connection
24	I/O		P1[7]	I ² C SCL	74	I/O	I	P0[0]	Analog column mux input
25			NC	No internal connection	75			NC	No internal connection
26			NC	No internal connection	76			NC	No internal connection
27			NC	No internal connection	77	I/O	I/O	P0[2]	Analog column mux input and column output
28	I/O		P1[5]	I ² C SDA	78			NC	No internal connection
29	I/O		P1[3]	I _{FTEST}	79	I/O	I/O	P0[4]	Analog column mux input and column output, V _{REF}
30	I/O		P1[1] ^[13]	Crystal (XTALin), I ² C SCL, TC SCLK.	80			NC	No internal connection
31			NC	No internal connection	81	I/O	I	P0[6]	Analog column mux input
32	Power		V _{DD}	Supply voltage	82	Power		V _{DD}	Supply voltage
33			NC	No internal connection	83	Power		V _{DD}	Supply voltage
34	Power		V _{SS}	Ground connection ^[12]	84	Power		V _{SS}	Ground connection ^[12]
35			NC	No internal connection	85	Power		V _{SS}	Ground connection ^[12]
36	I/O		P7[7]		86	I/O		P6[0]	
37	I/O		P7[6]		87	I/O		P6[1]	
38	I/O		P7[5]		88	I/O		P6[2]	
39	I/O		P7[4]		89	I/O		P6[3]	
40	I/O		P7[3]		90	I/O		P6[4]	
41	I/O		P7[2]		91	I/O		P6[5]	
42	I/O		P7[1]		92	I/O		P6[6]	
43	I/O		P7[0]		93	I/O		P6[7]	
44	I/O		P1[0]*	Crystal (XTALout), I ² C SDA, TC SDA	94			NC	No internal connection
45	I/O		P1[2]	V _{FTEST}	95	I/O	I	P0[7]	Analog column mux input
46	I/O		P1[4]	Optional External Clock Input (EXTCLK)	96			NC	No internal connection
47	I/O		P1[6]		97	I/O	I/O	P0[5]	Analog column mux input and column output
48			NC	No internal connection	98			NC	No internal connection
49			NC	No internal connection	99	I/O	I/O	P0[3]	Analog column mux input and column output
50			NC	No internal connection	100			NC	No internal connection

LEGEND A = Analog, I = Input, O = Output, NC = No connection. Pin must be left floating, TC/TM: Test.

Notes

12. All V_{SS} pins should be brought out to one common GND plane.

13. ISSP pin which is not High-Z at POR.

Table 9. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBB20DR0	40	#	ASC10CR0	80	RW	RD12RI	C0	RW
PRT0IE	01	RW	DBB20DR1	41	W	ASC10CR1	81	RW	RD12SYN	C1	RW
PRT0GS	02	RW	DBB20DR2	42	RW	ASC10CR2	82	RW	RD12IS	C2	RW
PRT0DM2	03	RW	DBB20CR0	43	#	ASC10CR3	83	RW	RD12LT0	C3	RW
PRT1DR	04	RW	DBB21DR0	44	#	ASD11CR0	84	RW	RD12LT1	C4	RW
PRT1IE	05	RW	DBB21DR1	45	W	ASD11CR1	85	RW	RD12RO0	C5	RW
PRT1GS	06	RW	DBB21DR2	46	RW	ASD11CR2	86	RW	RD12RO1	C6	RW
PRT1DM2	07	RW	DBB21CR0	47	#	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DCB22DR0	48	#	ASC12CR0	88	RW	RD13RI	C8	RW
PRT2IE	09	RW	DCB22DR1	49	W	ASC12CR1	89	RW	RD13SYN	C9	RW
PRT2GS	0A	RW	DCB22DR2	4A	RW	ASC12CR2	8A	RW	RD13IS	CA	RW
PRT2DM2	0B	RW	DCB22CR0	4B	#	ASC12CR3	8B	RW	RD13LT0	CB	RW
PRT3DR	0C	RW	DCB23DR0	4C	#	ASD13CR0	8C	RW	RD13LT1	CC	RW
PRT3IE	0D	RW	DCB23DR1	4D	W	ASD13CR1	8D	RW	RD13RO0	CD	RW
PRT3GS	0E	RW	DCB23DR2	4E	RW	ASD13CR2	8E	RW	RD13RO1	CE	RW
PRT3DM2	0F	RW	DCB23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW	DBB30DR0	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	DBB30DR1	51	W	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	DBB30DR2	52	RW	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	DBB30CR0	53	#	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	DBB31DR0	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	DBB31DR1	55	W	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	DBB31DR2	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	DBB31CR0	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
PRT6DR	18	RW	DCB32DR0	58	#	ASD22CR0	98	RW	I2C_DR	D8	RW
PRT6IE	19	RW	DCB32DR1	59	W	ASD22CR1	99	RW	I2C_MSCR	D9	#
PRT6GS	1A	RW	DCB32DR2	5A	RW	ASD22CR2	9A	RW	INT_CLR0	DA	RW
PRT6DM2	1B	RW	DCB32CR0	5B	#	ASD22CR3	9B	RW	INT_CLR1	DB	RW
PRT7DR	1C	RW	DCB33DR0	5C	#	ASC23CR0	9C	RW	INT_CLR2	DC	RW
PRT7IE	1D	RW	DCB33DR1	5D	W	ASC23CR1	9D	RW	INT_CLR3	DD	RW
PRT7GS	1E	RW	DCB33DR2	5E	RW	ASC23CR2	9E	RW	INT_MSK3	DE	RW
PRT7DM2	1F	RW	DCB33CR0	5F	#	ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RD10RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RD10SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RD10IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RD10LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RD10LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RD10RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RD10RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RD11RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RD11SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RD11IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RD11LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RD11LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RD11RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C29x66 PSoC device. For the most up-to-date electrical specifications, confirm that you have the most recent datasheet by going to the web at <http://www.cypress.com>.

Specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $T_J \leq 100^{\circ}\text{C}$, except where noted. Refer to Table 29 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 10. Voltage versus CPU Frequency

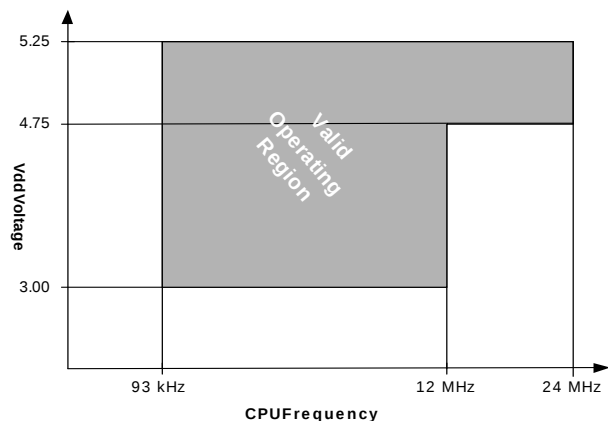
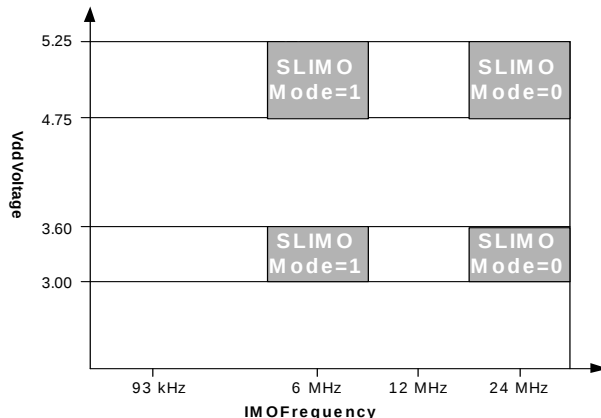


Figure 11. IMO Frequency Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	-55	25	+100	$^{\circ}\text{C}$	Higher storage temperatures reduce data retention time. Recommended storage temperature is $+25^{\circ}\text{C} \pm 25^{\circ}\text{C}$. Extended duration storage temperatures higher than 65°C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	—	125	See package label	$^{\circ}\text{C}$	
$T_{BAKETIME}$	Bake time	See package label	—	72	Hours	
T_A	Ambient temperature with power applied	-40	—	+85	$^{\circ}\text{C}$	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	-0.5	—	+6.0	V	
V_{IO}	DC input voltage	$V_{SS} - 0.5$	—	$V_{DD} + 0.5$	V	
V_{IOZ}	DC voltage applied to tristate	$V_{SS} - 0.5$	—	$V_{DD} + 0.5$	V	
I_{MIO}	Maximum current into any port pin	-25	—	+50	mA	
I_{MAIO}	Maximum current into any port pin configured as analog driver	-50	—	+50	mA	
ESD	Electrostatic discharge voltage	2000	—	—	V	Human body model ESD.
LU	Latch-up current	—	—	200	mA	

DC GPIO Specifications

Table 14 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 14. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull-up resistor	4	5.6	8	$k\Omega$	
R_{PD}	Pull-down resistor	4	5.6	8	$k\Omega$	
V_{OH}	High output level	$V_{DD} - 1.0$	–	–	V	$I_{OH} = 10\text{ mA}$, $V_{DD} = 4.75\text{ V to }5.25\text{ V}$ (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	$I_{OL} = 25\text{ mA}$, $V_{DD} = 4.75\text{ V to }5.25\text{ V}$ (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High level source current	10	–	–	mA	$V_{OH} = V_{DD} - 1.0\text{ V}$, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low level sink current	25	–	–	mA	$V_{OL} = 0.75\text{ V}$, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.8	V	$V_{DD} = 3.0\text{ to }5.25$
V_{IH}	Input high level	2.1	–	–	V	$V_{DD} = 3.0\text{ to }5.25$
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to $1\text{ }\mu\text{A}$.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C .
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C .

Table 16. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	1.4	10	mV	Power = High, Opamp bias = High setting is not allowed for 3.3 V V_{DD} operation.
	Power = Low, Opamp bias = Low	–	1.4	10	mV	
	Power = Low, Opamp bias = High	–	1.4	10	mV	
	Power = Medium, Opamp bias = Low	–	1.4	10	mV	
	Power = Medium, Opamp bias = High	–	1.4	10	mV	
	Power = High, Opamp bias = Low	–	1.4	10	mV	
	Power = High, Opamp bias = High	–	–	–	mV	
TCV_{OSOA}	Average input offset voltage drift	–	7	40	$\mu V/^{\circ}C$	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	200	–	pA	Gross tested to 1 μA .
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 $^{\circ}C$
V_{CMOA}	Common mode voltage range	0	–	V_{DD}	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common mode rejection ratio	60	–	–	dB	
G_{OLOA}	Open loop gain	80	–	–	dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals)	$V_{DD} - 0.01$	–	–	V	
V_{OLOWOA}	Low output voltage swing (internal signals)	–	–	0.01	V	
I_{SOA}	Supply current (including associated AGND buffer)					Power = High, Opamp bias = High setting is not allowed for 3.3 V V_{DD} operation.
	Power = Low, Opamp bias = Low	–	150	200	μA	
	Power = Low, Opamp bias = High	–	300	400	μA	
	Power = Medium, Opamp bias = Low	–	600	800	μA	
	Power = Medium, Opamp bias = High	–	1200	1600	μA	
	Power = High, Opamp bias = Low	–	2400	3200	μA	
	Power = High, Opamp bias = High	–	–	–	μA	
$PSRR_{OA}$	Supply voltage rejection ratio	54	80	–	dB	$V_{SS} \leq V_{IN} \leq (V_{DD} - 2.25)$ or $(V_{DD} - 1.25 V) \leq V_{IN} \leq V_{DD}$

DC Low-Power Comparator Specifications

Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, 3.0 V to 3.6 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, or 2.4 V to 3.0 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, respectively. Typical parameters apply to 5 V at 25 $^{\circ}C$ and are for design guidance only.

Table 17. DC Low-Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Unit
V_{REFLPC}	Low-power comparator (LPC) reference voltage range	0.2	–	$V_{DD} - 1$	V
I_{SLPC}	LPC supply current	–	10	40	μA
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV

DC Analog Output Buffer Specifications

Table 18 and Table 19 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 18. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOB}	Input offset voltage (absolute value)					
	Power = Low, Opamp bias = Low	–	3.2	18	mV	
	Power = Low, Opamp bias = High	–	3.2	18	mV	
	Power = High, Opamp bias = Low	–	3.2	18	mV	
	Power = High, Opamp bias = High	–	3.2	18	mV	
TCV_{OSOB}	Average input offset voltage drift	–	5.5	26	$\mu\text{V}/^{\circ}\text{C}$	
V_{CMOB}	Common-mode input voltage range	0.5	–	$V_{\text{DD}} - 1.0$	V	
R_{OUTOB}	Output resistance					
	Power = Low	–	–	1	Ω	
	Power = High	–	–	1	Ω	
V_{OHIGHOB}	High output voltage swing (Load = 32 ohms to $V_{\text{DD}}/2$)					
	Power = Low	$0.5 \times V_{\text{DD}} + 1.3$	–	–	V	
	Power = High	$0.5 \times V_{\text{DD}} + 1.3$	–	–	V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to $V_{\text{DD}}/2$)					
	Power = Low	–	–	$0.5 \times V_{\text{DD}} - 1.3$	V	
	Power = High	–	–	$0.5 \times V_{\text{DD}} - 1.3$	V	
I_{SOB}	Supply current including bias cell (no load)					
	Power = Low	–	1.1	2	mA	
	Power = High	–	2.6	5	mA	
PSRR_{OB}	Supply voltage rejection ratio	40	64		dB	
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.

DC Switch Mode Pump Specifications

Table 20 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 20. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
$V_{\text{PUMP } 5\text{ V}}$	5 V output voltage at V_{DD} from pump	4.75	5.0	5.25	V	Configured as in Note 15. Average, neglecting ripple. SMP trip voltage is set to 5.0 V
$V_{\text{PUMP } 3\text{ V}}$	3 V output voltage at V_{DD} from pump	3.00	3.25	3.60	V	Configured as in Note 15. Average, neglecting ripple. SMP trip voltage is set to 3.25 V
I_{PUMP}	Available output current $V_{\text{BAT}} = 1.5\text{ V}$, $V_{\text{PUMP}} = 3.25\text{ V}$ $V_{\text{BAT}} = 1.8\text{ V}$, $V_{\text{PUMP}} = 5.0\text{ V}$	8 5	— —	— —	mA mA	Configured as in Note 15 SMP trip voltage is set to 3.25 V SMP trip voltage is set to 5.0 V
$V_{\text{BAT } 5\text{ V}}$	Input voltage range from battery	1.8	—	5.0	V	Configured as in Note 15. SMP trip voltage is set to 5.0 V
$V_{\text{BAT } 3\text{ V}}$	Input voltage range from battery	1.0	—	3.3	V	Configured as in Note 15. SMP trip voltage is set to 3.25 V
V_{BATSTART}	Minimum input voltage from battery to start pump	1.2	—	—	V	Configured as in Note 15. $0^{\circ}\text{C} \leq T_A \leq 100^{\circ}\text{C}$. 1.25 V at $T_A = -40^{\circ}\text{C}$
$\Delta V_{\text{PUMP_Line}}$	Line regulation (over V_{BAT} range)	—	5	—	% V_{O}	Configured as in Note 15. V_{O} is the " V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 26, "DC POR, SMP, and LVD Specifications," on page 38
$\Delta V_{\text{PUMP_Load}}$	Load regulation	—	5	—	% V_{O}	Configured as in Note 15. V_{O} is the " V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in Table 26, "DC POR, SMP, and LVD Specifications," on page 38
$\Delta V_{\text{PUMP_Ripple}}$	Output voltage ripple (depends on capacitor/load)	—	100	—	mVpp	Configured as in Note 15. Load is 5 mA
E_3	Efficiency	35	50	—	%	Configured as in Note 15. Load is 5 mA. SMP trip voltage is set to 3.25 V
F_{PUMP}	Switching frequency	—	1.4	—	MHz	
DC_{PUMP}	Switching duty cycle	—	50	—	%	

Note

15. $L_1 = 2\text{ }\mu\text{H}$ inductor, $C_1 = 10\text{ }\mu\text{F}$ capacitor, $D_1 = \text{Schottky diode}$. See Figure 12.

Table 22. 3.3-V DC Analog Reference Specifications

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = High Opamp bias = High	V _{REFHI}	Ref High	V _{DD} /2 + Band-Gap	V _{DD} /2 + 1.225	V _{DD} /2 + 1.292	V _{DD} /2 + 1.361	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.067	V _{DD} /2 – 0.002	V _{DD} /2 + 0.063	V
		V _{REFLO}	Ref Low	V _{DD} /2 – Band-Gap	V _{DD} /2 – 1.35	V _{DD} /2 – 1.293	V _{DD} /2 – 1.210	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref High	V _{DD} /2 + Band-Gap	V _{DD} /2 + 1.218	V _{DD} /2 + 1.294	V _{DD} /2 + 1.370	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.038	V _{DD} /2 – 0.001	V _{DD} /2 + 0.035	V
		V _{REFLO}	Ref Low	V _{DD} /2 – Band-Gap	V _{DD} /2 – 1.329	V _{DD} /2 – 1.296	V _{DD} /2 – 1.259	V
	RefPower = Med Opamp bias = High	V _{REFHI}	Ref High	V _{DD} /2 + Band-Gap	V _{DD} /2 + 1.221	V _{DD} /2 + 1.294	V _{DD} /2 + 1.366	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.050	V _{DD} /2 – 0.002	V _{DD} /2 + 0.046	V
		V _{REFLO}	Ref Low	V _{DD} /2 – Band-Gap	V _{DD} /2 – 1.331	V _{DD} /2 – 1.296	V _{DD} /2 – 1.260	V
	RefPower = Med Opamp bias = Low	V _{REFHI}	Ref High	V _{DD} /2 + Band-Gap	V _{DD} /2 + 1.226	V _{DD} /2 + 1.295	V _{DD} /2 + 1.365	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.028	V _{DD} /2 – 0.001	V _{DD} /2 + 0.025	V
		V _{REFLO}	Ref Low	V _{DD} /2 – Band-Gap	V _{DD} /2 – 1.329	V _{DD} /2 – 1.297	V _{DD} /2 – 1.262	V

Table 22. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b010	RefPower = High Opamp bias = High	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.06	V _{DD} – 0.010	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.05	V _{DD} /2 – 0.002	V _{DD} /2 + 0.040	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.009	V _{SS} + 0.056	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.060	V _{DD} – 0.006	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.028	V _{DD} /2 – 0.001	V _{DD} /2 + 0.025	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.005	V _{SS} + 0.034	V
	RefPower = Med Opamp bias = High	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.058	V _{DD} – 0.008	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.037	V _{DD} /2 – 0.002	V _{DD} /2 + 0.033	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.007	V _{SS} + 0.046	V
	RefPower = Med Opamp bias = Low	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.057	V _{DD} – 0.006	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.025	V _{DD} /2 – 0.001	V _{DD} /2 + 0.022	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.004	V _{SS} + 0.030	V
0b011	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–

DC POR, SMP, and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0

V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 26. DC POR, SMP, and LVD Specifications

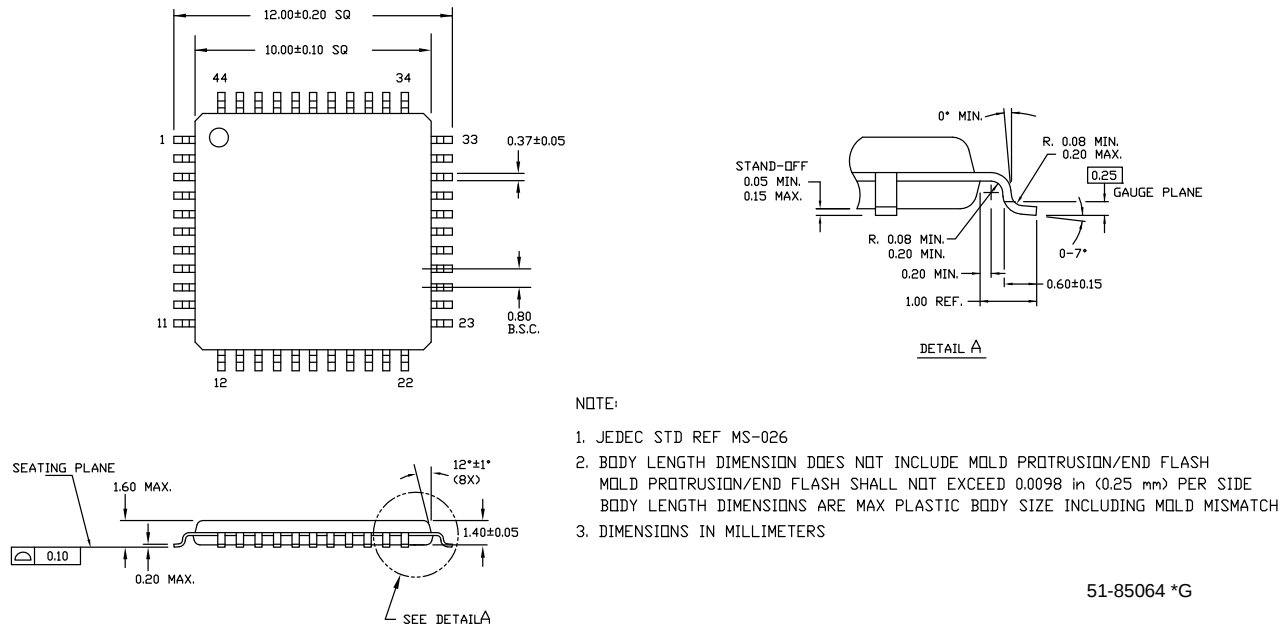
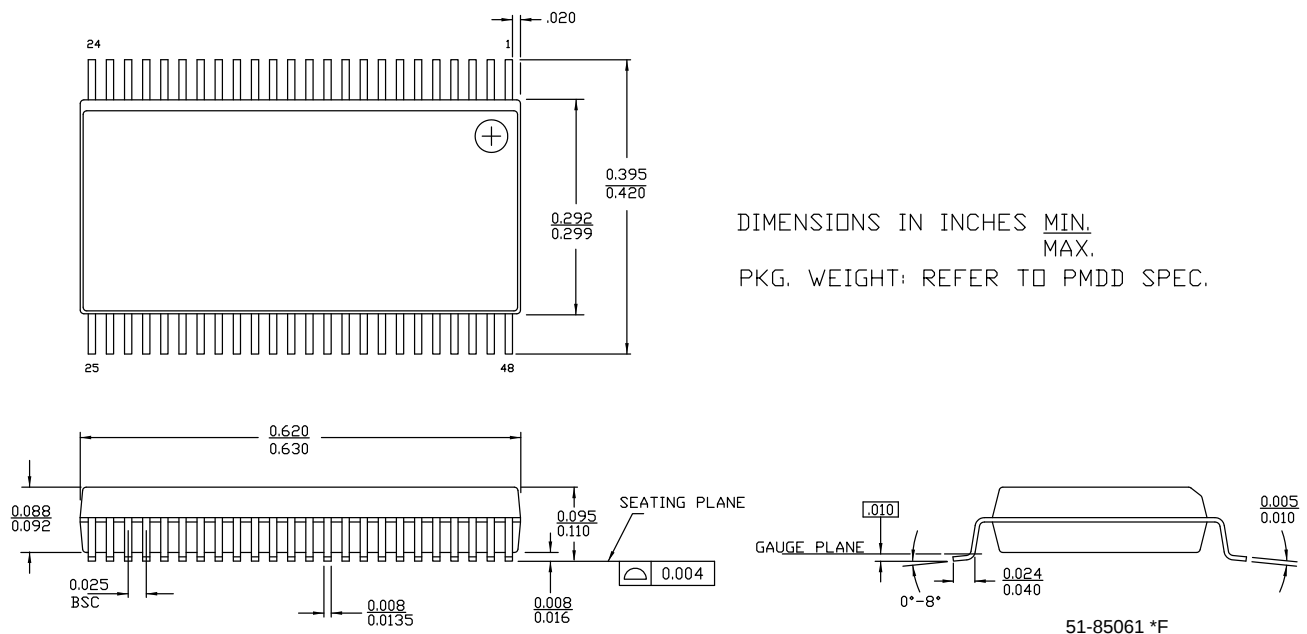
Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR0R} V_{PPOR1R} V_{PPOR2R}	V_{DD} value for PPOR trip (positive ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	—	2.91 4.39 4.55	—	V V V	
V_{PPOR0} V_{PPOR1} V_{PPOR2}	V_{DD} value for PPOR trip (negative ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	—	2.82 4.39 4.55	—	V V V	
V_{PH0} V_{PH1} V_{PH2}	PPOR hysteresis PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	— — —	92 0 0	— — —	mV mV mV	
V_{LVD0} V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	V_{DD} value for LVD trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.86 2.96 3.07 3.92 4.39 4.55 4.63 4.72	2.92 3.02 3.13 4.00 4.48 4.64 4.73 4.81	2.98 ^[16] 3.08 3.20 4.08 4.57 4.74 ^[17] 4.82 4.91	V V V V V V V V	
V_{PUMP0} V_{PUMP1} V_{PUMP2} V_{PUMP3} V_{PUMP4} V_{PUMP5} V_{PUMP6} V_{PUMP7}	V_{DD} value for SMP trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.96 3.03 3.18 4.11 4.55 4.63 4.72 4.90	3.02 3.10 3.25 4.19 4.64 4.73 4.82 5.00	3.08 3.16 3.32 4.28 4.74 4.82 4.91 5.10	V V V V V V V V	

Notes

16. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
17. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

Figure 23. 44-pin TQFP (10 × 10 × 1.4 mm) Package Outline, 51-85064

44 Lead Thin Plastic Quad Flatpack 10 X 10 X 1.4mm


Figure 24. 48-pin SSOP (300 Mils) Package Outline, 51-85061


Ordering Information

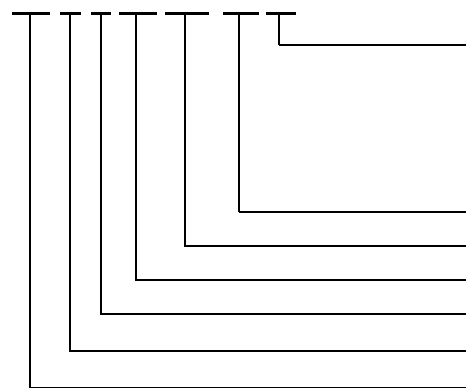
The following table lists the CY8C29x66 PSoC device's key package features and ordering codes.

Package	Ordering Code	Flash (KB)	RAM (KB)	Switch Mode Pump	Temperature Range	Digital PSoC Blocks	Analog PSoC Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-pin (300-mil) DIP	CY8C29466-24PXI	32	2	Yes	-40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (210-mil) SSOP	CY8C29466-24PVXI	32	2	Yes	-40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (210-mil) SSOP (Tape and Reel)	CY8C29466-24PVXIT	32	2	Yes	-40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (300-mil) SOIC	CY8C29466-24SXI	32	2	Yes	-40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (300-mil) SOIC (Tape and Reel)	CY8C29466-24SXIT	32	2	Yes	-40 °C to +85 °C	16	12	24	12	4	Yes
44-pin TQFP	CY8C29566-24AXI	32	2	Yes	-40 °C to +85 °C	16	12	40	12	4	Yes
44-pin TQFP (Tape and Reel)	CY8C29566-24AXIT	32	2	Yes	-40 °C to +85 °C	16	12	40	12	4	Yes
48-pin (300-mil) SSOP	CY8C29666-24PVXI	32	2	Yes	-40 °C to +85 °C	16	12	44	12	4	Yes
48-pin (300-mil) SSOP (Tape and Reel)	CY8C29666-24PVXIT	32	2	Yes	-40 °C to +85 °C	16	12	44	12	4	Yes
100-Pin TQFP	CY8C29866-24AXI	32	2	Yes	-40 °C to +85 °C	16	12	64	12	4	Yes
100-Pin OCD TQFP ^[35]	CY8C29000-24AXI	32	2	Yes	-40 °C to +85 °C	16	12	64	12	4	Yes
48-Pin (7 × 7 × 1.0 mm) QFN (Sawn)	CY8C29666-24LTXI	32	2	Yes	-40 °C to +85 °C	16	12	44	12	4	Yes
48-Pin (7 × 7 × 1.0 mm) QFN (Sawn)	CY8C29666-24LTXIT	32	2	Yes	-40 °C to +85 °C	16	12	44	12	4	Yes

Note For Die sales information, contact a local Cypress sales office or field applications engineer (FAE).

Ordering Code Definitions

CY 8 C 29 xxx-SPxx



Package Type: Thermal Rating:
 PX = PDIP Pb-free C = Commercial
 SX = SOIC Pb-free I = Industrial
 PVX = SSOP Pb-free E = Extended
 LFX/LKX/LTX/LQX/LCX = QFN Pb-free
 AX = TQFP Pb-free
 Speed: 24 MHz
 Part Number
 Family Code
 Technology Code: C = CMOS
 Marketing Code: 8 = Cypress PSoC
 Company ID: CY = Cypress

Note

35. This part may be used for in-circuit debugging. It is NOT available for production.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level API (Application Programming Interface) for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V _{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V _{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Document Title: CY8C29466/CY8C29566/CY8C29666/CY8C29866, PSoC® Programmable System-on-Chip™ Document Number: 38-12013				
Revision	ECN	Origin of Change	Submission Date	Description of Change
**	131151	New Silicon	11/13/2003	New document (Revision **).
*A	132848	NWJ	01/21/2004	New information. First edition of preliminary datasheet.
*B	133205	NWJ	01/27/2004	Changed part numbers, increased SRAM data storage to 2 K bytes.
*C	133656	SFV	02/09/2004	Changed part numbers and removed a 28-pin SOIC.
*D	227240	SFV	06/12/2004	Changes to Overview section, 48-pin MLF pinout, and significant changes to the Electrical Specs.
*E	240108	SFV	See ECN	Added a 28-lead (300 mil) SOIC part.
*F	247492	SFV	See ECN	New information added to the Electrical Specifications chapter.
*G	288849	HMT	See ECN	Add DS standards, update device table, fine-tune pinouts, add Reflow Peak Temp. table. Finalize.
*H	722736	HMT	See ECN	Add QFN package clarifications. Add new QFN diagram. Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add CY8C20x34 to PSoC Device Characteristics table. Update emulation pod/feet kit part numbers. Add OCD non-production pinouts and package diagrams. Add ISSP note to pinout tables. Update package diagram revisions. Update typical and recommended Storage Temperature per industrial specs. Update CY branding and QFN convention. Add new Dev. Tool section. Update copyright and trademarks.
*I	2503350	DFK / PYRS	See ECN	Pinout for CY8C29000 OCD wrongly included details of CY8C24X94. The correct pinout for CY8C29000 is included in this version. Added note on digital signaling in "DC Analog Reference Specifications" section.
*J	2545030	YARA	07/29/08	Added note to Ordering Information
*K	2708295	JVY	04/22/2009	Changed title from "CY8C29466, CY8C29566, CY8C29666, and CY8C29866 PSoC Mixed Signal Array Final datasheet" to "CY8C29466, CY8C29566, CY8C29666, and CY8C29866 PSoC® Programmable System-on-Chip™" Updated to datasheet template Added 48-Pin QFN (Sawn) package diagram and CY8C29666-24LTXI and CY8C29666-24LTXIT part details in the Ordering Information table Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified F _{IMO6} (page 27), T _{WRITE} specifications (page 34) Added I _{OH} (page 21), I _{OL} (page 21), DC _{ILO} (page 28), F _{32K_U} (page 27), T _{POWERUP} (page 28), T _{ERASEALL} (page 34), T _{PROGRAM_HOT} (page 34), and T _{PROGRAM_COLD} (page 34) specifications
*L	2761941	DRSW / AESA	09/10/2009	Added SR _{POWER_UP} parameter in AC specs table.
*M	2842762	DRSW	01/08/2010	Corrected Notes for V _{DD} parameter in Table 13, "DC Chip-Level Specifications," on page 22. Added " Contents " on page 3. Updated links in Sales , Solutions , and Legal Information .

Document History Page (continued)

Document Title: CY8C29466/CY8C29566/CY8C29666/CY8C29866, PSoC [®] Programmable System-on-Chip™ Document Number: 38-12013				
Revision	ECN	Origin of Change	Submission Date	Description of Change
*V	3991993	PMAD	05/08/2013	Updated Packaging Information : spec 51-85014 – Changed revision from *F to *G. spec 51-85061 – Changed revision from *E to *F. spec 001-13191 – Changed revision from *F to *G. Updated Reference Documents (Removed 001-17397 spec, 001-14503 spec related information). Added Errata .
*W	4081641	PMAD	07/31/2013	Added Errata footnotes (Note 1, 2, 14, 21, 25). Updated Features : Replaced “±2.5%” with “±5%”. Added Note 1 and referred the same note in ±5% under “Precision, programmable clocking”. Updated PSoC Functional Overview : Updated PSoC Core : Replaced “2.5%” with “5%” in 4th paragraph. Added Note 2 and referred the same note in 5%. Updated Electrical Specifications : Updated DC Electrical Characteristics : Updated DC Chip-Level Specifications : Added Note 14 and referred the same note in V _{DD} parameter. Updated AC Electrical Characteristics : Updated AC Chip-Level Specifications : Added Note 21 and referred the same note in F _{IMO24} parameter in Table 29 . Replaced all instances of “24.6” with “25.2” in Table 29 . Replaced all instances of “23.4” with “22.8” in Table 29 . Replaced all instances of “49.2” with “50.4” in Table 29 . Replaced “12.3” with “12.6” for maximum value of F _{CPU2} parameter in Table 29 . Replaced “46.8” with “45.6” for minimum value of F _{out48M} parameter in Table 29 . Added Note 25 and referred the same note in T _{POWERUP} parameter in Table 29 . Updated AC Digital Block Specifications : Replaced all instances of “49.2” with “50.4” in Table 34 . Replaced all instances of “24.6” with “25.2” in Table 34 . Updated Packaging Information : spec 51-85026 – Changed revision from *F to *G. spec 51-85048 – Changed revision from *G to *H. Updated Errata . Updated in new template.
*X	4378144	PMAD	05/13/2014	Updated Electrical Specifications : Updated AC Electrical Characteristics : Updated AC External Clock Specifications : Updated Table 37 : Changed unit from “ms” to “μs” corresponding to “Power-up IMO to switch”. Updated Packaging Information : spec 51-85026 – Changed revision from *G to *H. spec 51-85064 – Changed revision from *E to *F. spec 51-85048 – Changed revision from *H to *I. Completing Sunset Review.